

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-20	0.065 @ V _{GS} = -4.5 V	-4.9
	0.095 @ V _{GS} = -2.5 V	-4.1

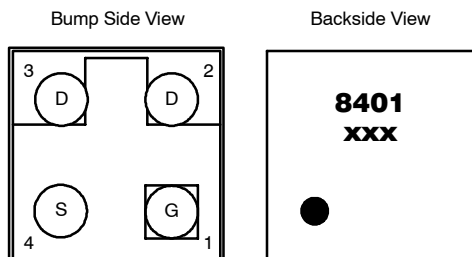
FEATURES

- TrenchFET® Power MOSFET
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Pin Compatible to Industry Standard Si3443DV

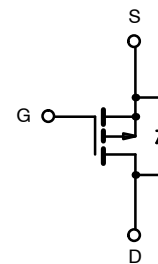
APPLICATIONS

- PA, Battery and Load Switch
- Battery Charger Switch
- PA Switch

MICRO FOOT



Device Marking: 8401
xxx = Date/Lot Traceability Code



P-Channel MOSFET

Ordering Information: Si8401DB-T1
Si8401DB-T1—E3 (Lead Free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	-4.9	-3.6	A
		T _A = 70 °C	-3.9	-2.8	
Pulsed Drain Current	I _{DM}	-10			
continuous Source Current (Diode Conduction) ^a	I _S	-2.5	-2.5		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.77	1.47	W
		T _A = 70 °C	1.77	0.94	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C
Package Reflow Conditions ^b	VPR	215/245°			
	IR/Convection	220/250°			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 sec	35	45	°C/W
		Steady State	72	85	
Maximum Junction-to-Foot (drain)	R _{thJF}	16	20		

Notes

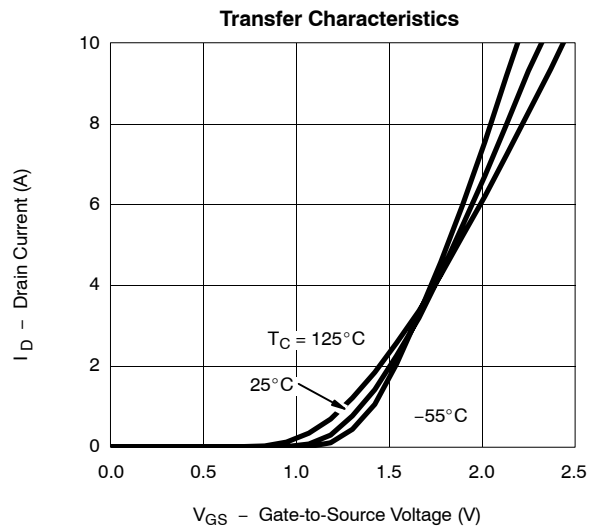
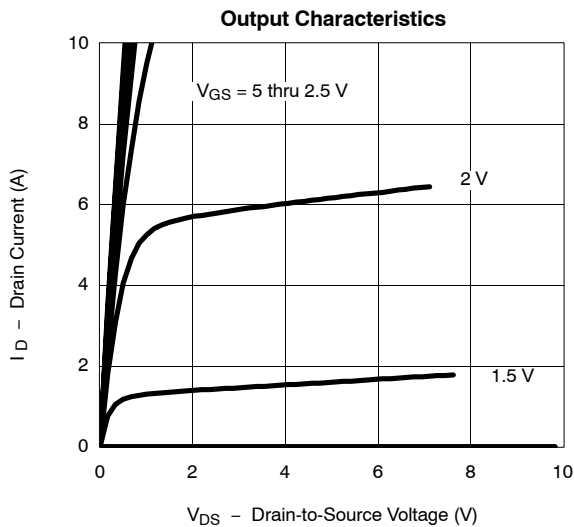
- Surface Mounted on 1" x 1" FR4 Board.
- Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.
- Package reflow conditions for lead-free.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45	-0.9		V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-5			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -1 A		0.057	0.065	Ω
		V _{GS} = -2.5 V, I _D = -1 A		0.080	0.095	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -1 A		6		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1 A, V _{GS} = 0 V		-0.73	-1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -1 A		11	17	nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			2.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		17	25	ns
Rise Time	t _r			28	45	
Turn-Off Delay Time	t _{d(off)}			88	135	
Fall Time	t _f			60	90	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -A, di/dt = 100 A/μs			

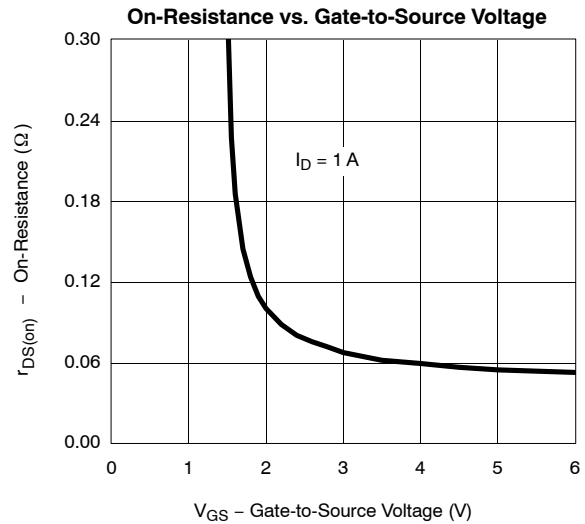
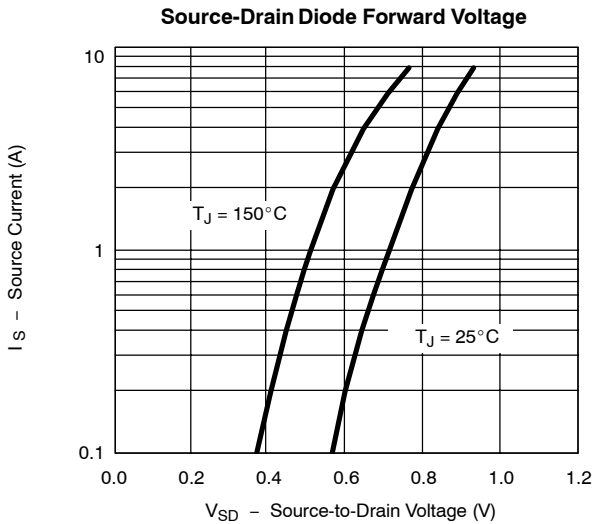
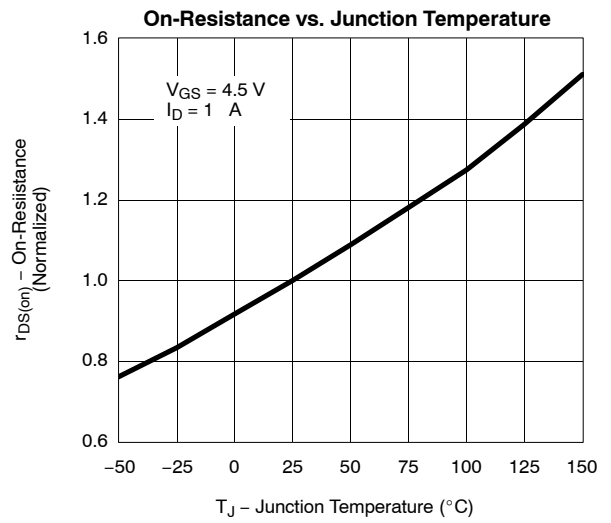
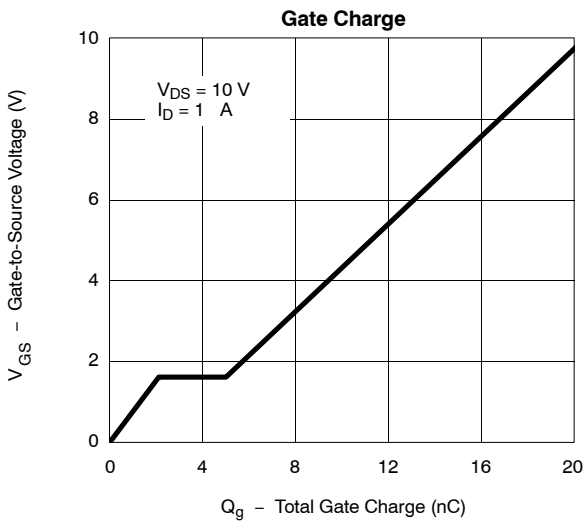
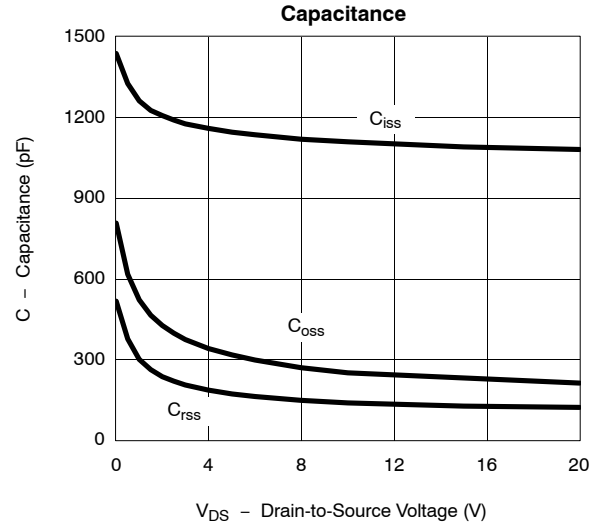
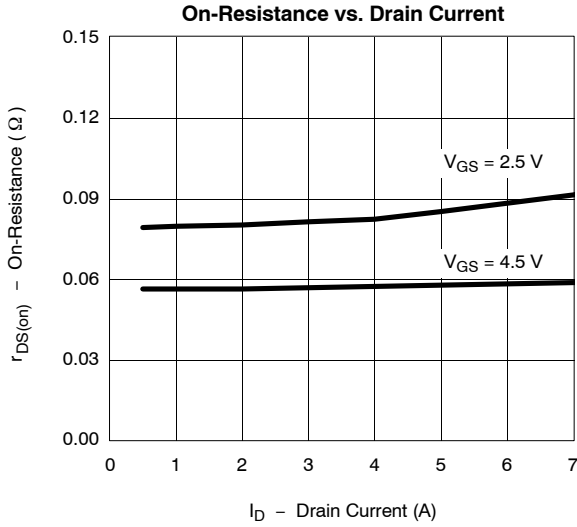
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

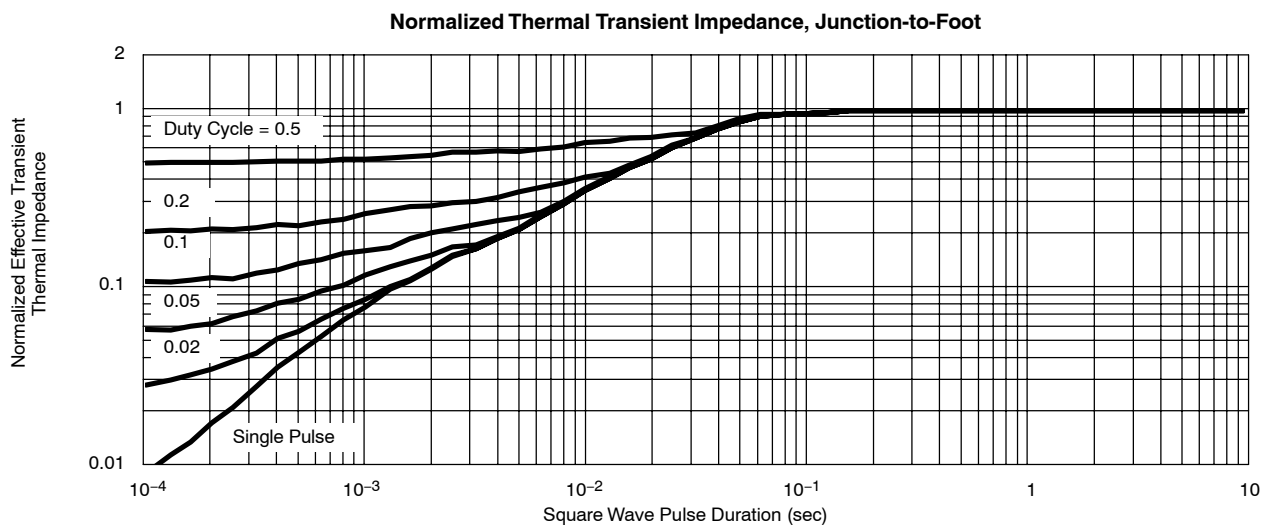
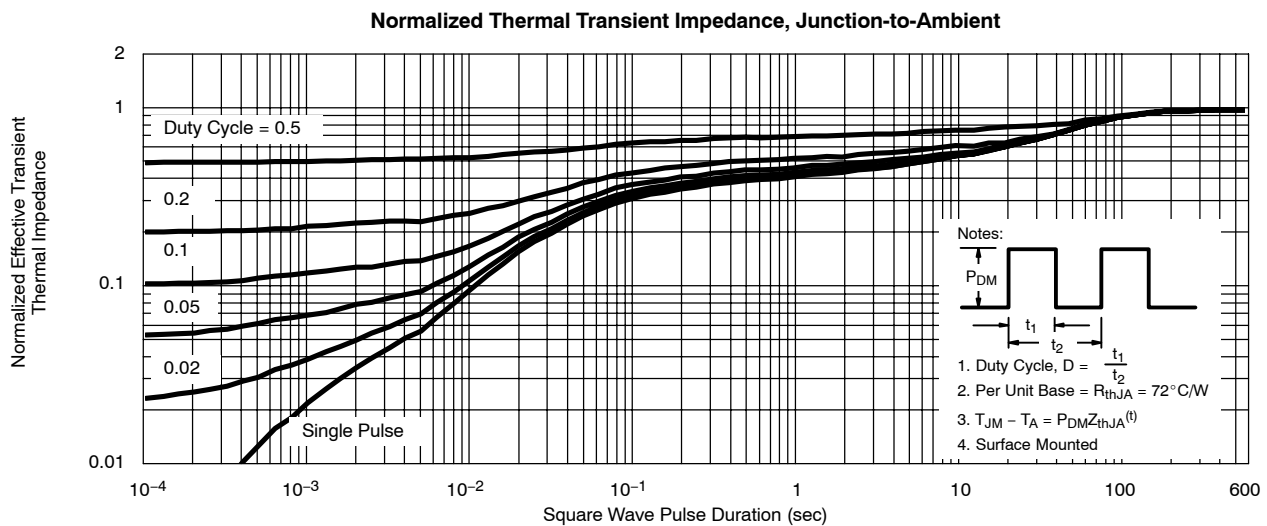
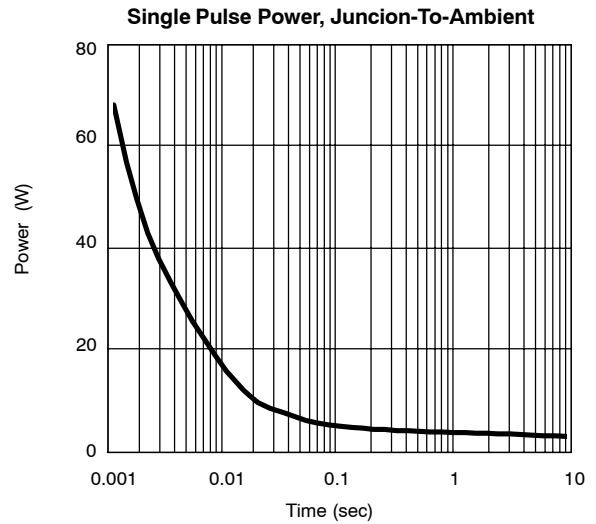
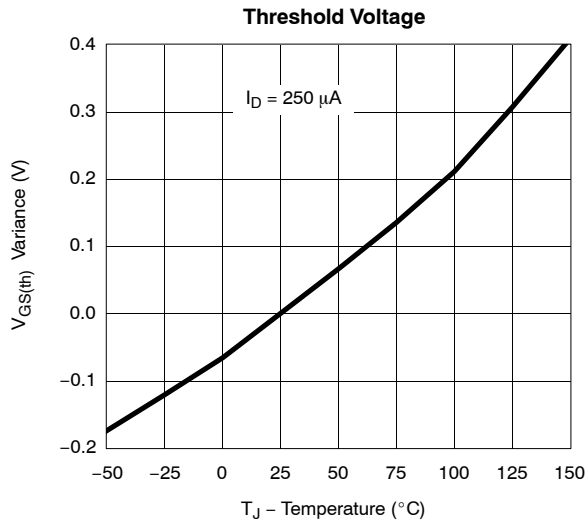
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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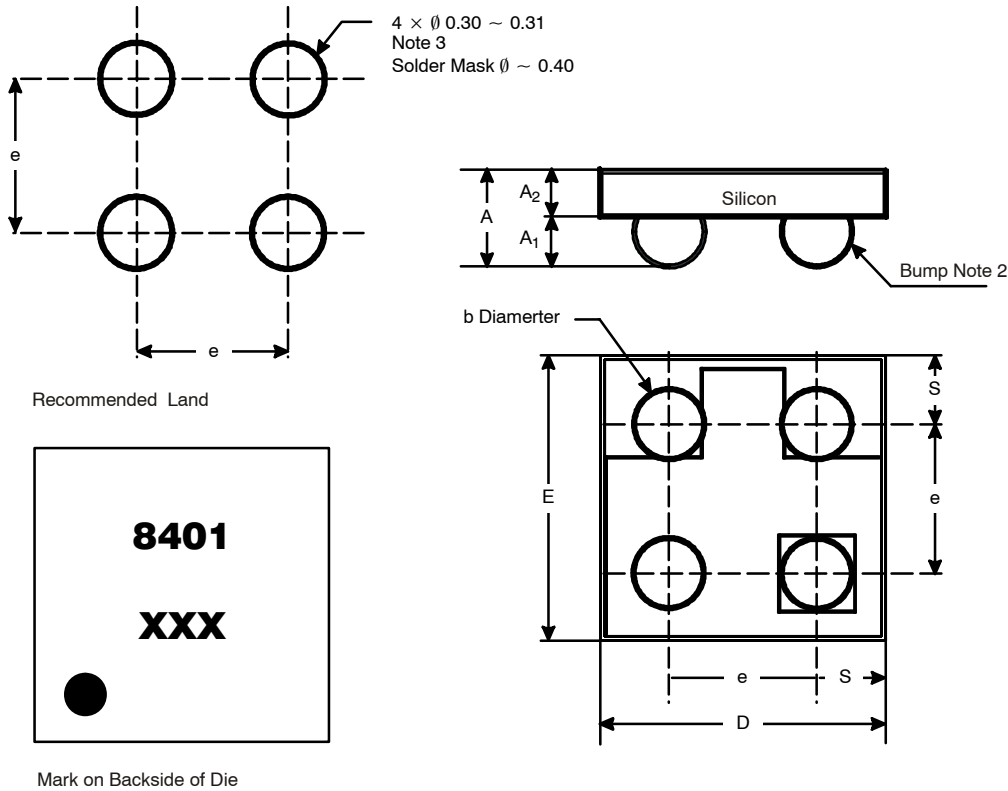


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 X 2, 0.8-mm PITCH)



NOTES (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Eutectic solder 63/57 Sn/Pb. (Sn 3.8 Ag, 0.7 Cu for Pb-free bumps)
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A₁	0.260	0.290	0.0102	0.0114
A₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

* Use millimeters as the primary measurement.