Technical Reference Note

Embedded Power for
Business-Critical Continuity

LGA C Series
3/6/10/20 A

Total Power: 15-100 Watts
No. of Outputs: Single

RoHS 2002/95/EC

Special Features

- 3,6,10 and 20 A output current rating
- Wide input voltage range: up to 14 Vdc
- Adjustable output voltage: 0.59-5.1 V
- Excellent transient response
- High efficiency
- Output margining
- Power enable
- Minimal airflow requirement
- Termination voltage capability
- Ultra compact profile and footprint
- RoHS compliant
- Remote sense

Product Family: **LGA C Series**
Function: **Embedded Power Device**
Usage: **ASIC, Memory, FPGAs, Telecom and Networking Equipment, Servers, Industrial Equipment, POL Regulation**

Definition:

The LGA C Series is a new high density, non-isolated converter for space sensitive applications. This Embedded Power Device (EPD) has a wide input range up to14.0 V and offers a 0.59-5.1 V adjustable output with 3, 6, 10 and 20 A capability without derating. This EPD offers a complete feature set of of enable, remote sense, and power good inclusive of a wide adjustable output range.

Standards

Designed to meet EN60950 when utilized in end use equipment.
International Standards for Solderability: J-STD-002B
IEC-60068-2-58

EMERSON
Network Power

Electrical Description

Electrical Description

The LGA C Series is implemented using a voltage mode single-phase synchronous buck topology. A block diagram of the converter is shown in Figure 1.

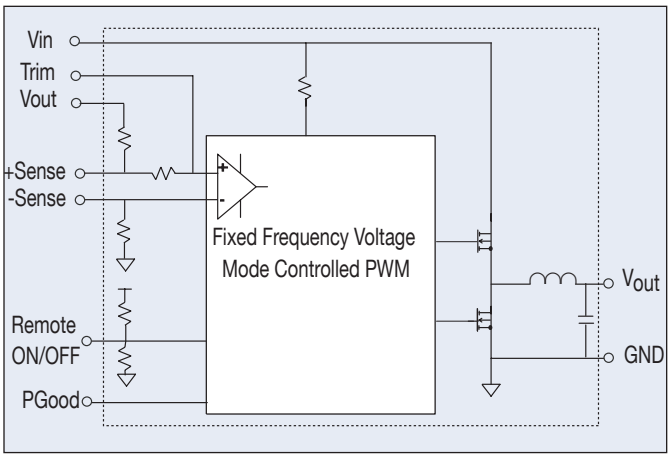


Figure 1 - Electrical Block Diagram

The output voltage is adjustable over a range of 0.59 - 5.1 V by using a resistor or voltage as described on Page 5. (Factory preset is 0.591Vout.)

The converter can be shut down via the remote ON/OFF. The remote ON/OFF operates with positive logic that is compatible with popular logic devices. Positive logic implies that the converter is enabled if the remote ON/OFF input is high (or floating), and disabled if it is low.

The power good signal is an open collector output that is pulled low by the PWM controller when it detects the output is not within ±10% of its set value.

The output is monitored for overcurrent and short-circuit conditions. When the PWM controller detects an overcurrent condition, it forces the module into hiccup mode.

A typical application is shown in Figure 2.

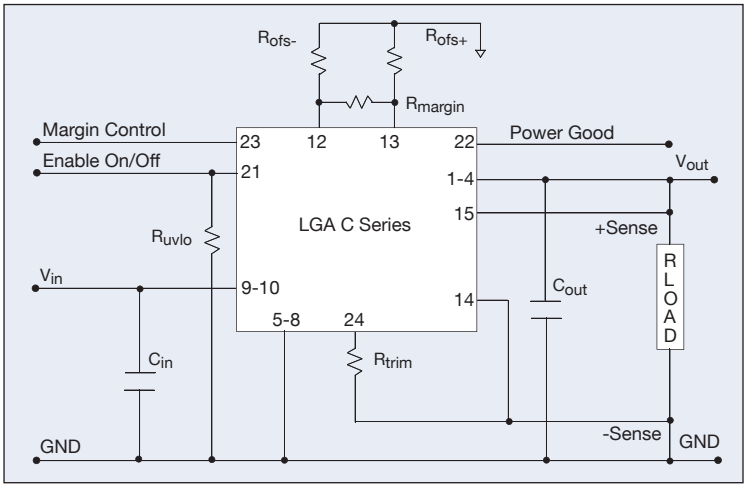


Figure 2 - Standard Application Drawing

Wide Operating Temperature Range

The LGA C Series's ability to accommodate a wide range of ambient temperatures is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the thermally enhanced cover. The maximum output power that the module delivers will depend on a number of parameters, primarily:

- Input voltage range
- Output load current
- Air velocity (forced or natural convection)
- Addition of heatisnk

The LGA C Series module has an operating temperature range of -40 °C to 85 °C with suitable derating.

Features and Functions

Output Voltage Adjustment
The output voltage on all models is adjustable from 0.59 - 5.1 V.

Undervoltage Lockout
The default undervoltage lockout is set as follows:

LGA 03/06/10C: 2.9 V
LGA20C: 4.3 V

Current Limit and Short-Circuit Protection
The LGA C models have a built-in non-latching current limit function and full continuous short-circuit protection. The module monitors current through the top and bottom FET. When an overcurrent condition occurs, the module goes into hiccup mode, where it attempts to power up periodically to determine if the problem persists.

The output current level is sensed through the voltage drop across the top and bottom FETs during their on time. This type of sensing is affected by temperature due to the change in Rdson. At higher temperatures, the Rdson increases, which lowers the overcurrent point.

Note that the module specifications are not guaranteed when the unit is operated in an overcurrent condition.

Remote ON/OFF
The remote ON/OFF input allows external circuitry to put the LGA C Series converter into a low dissipation sleep mode. Positive logic remote ON/OFF is available as standard.

The EPD is turned on if the remote ON/OFF pin is high or floating. Pulling the pin low will turn off the EPD. To guarantee turn-on, the enable voltage must be above 0.50 V. To turn off the enable voltage, it must be pulled below 0.2 V.

Figures illustrating the response of the unit to switching on and off using the remote ON/OFF feature are included on pages 13, 16, 20 and 25. Figures 3 and 4 show various circuits for driving the remote ON/OFF feature. The remote ON/OFF input can be driven through a discrete device (e.g. a bipolar signal transistor) or directly from a logic gate output. The output of the logic gate may be an open-collector (or open-drain) device. Please note the remote ON/OFF pin should only be driven in the following range:

If, $V_{in} \leq 5$ V, $V_{on/off\ (max)} = V_{in}$

If, $V_{in} > 5$ V, $V_{on/off\ (max)} = 5$ V

Features and Functions (cont'd)

Remote ON/OFF (cont'd)

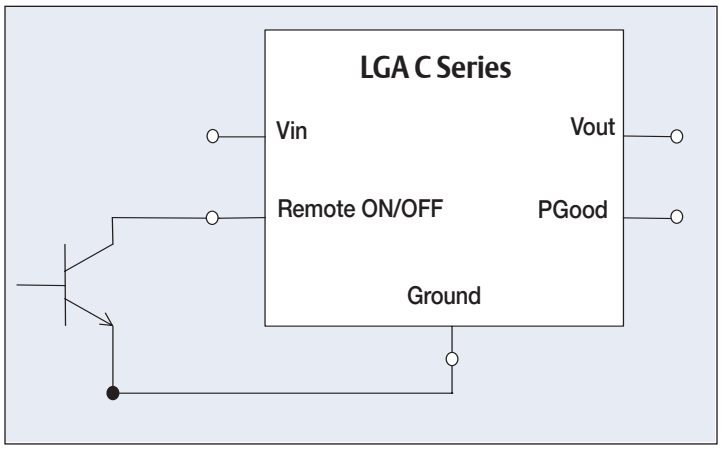


Figure 3 - Remote ON/OFF Input Drive Circuit for Non-Isolated Biopolar

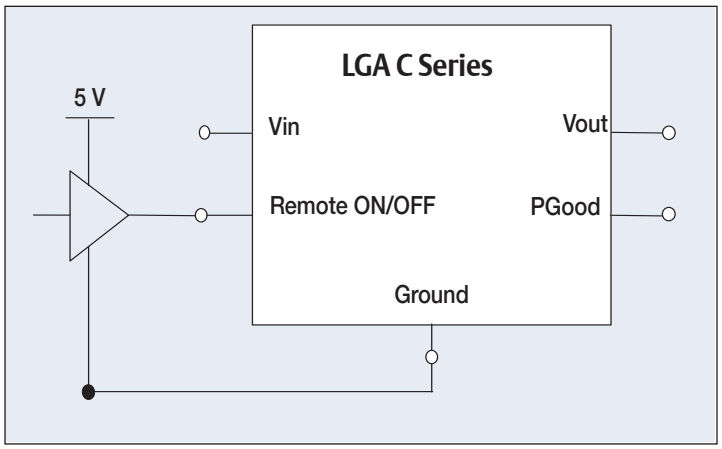


Figure 4 - Remote ON/OFF Input Drive Circuit for Logic Driver

Power Good

The LGA C modules have a power good indicator output. This output pin uses positive logic and is open-collector. Also, the power good output is able to sink 10 mA.

When the output of the module is within ±10% of the nominal set point, the Power Good pin can be pulled high. Note that Power Good should not be pulled higher than the following conditions:

If, $Vin \leq 5\ V$, $V_{pgood}\ (max) = Vin$

If, $Vin > 5\ V$, $V_{pgood}\ (max) = 5\ V$

Current Sink Capabilities

The LGA C series of dc-dc converters is able to current sink as well as current source. The EPD operates over the full output current range at any specified output voltage. This feature allows the LGA C to fit into any voltage termination application.

Setting Output Voltage

The output of the module can be adjusted from 0.59 V to 5.1 V. This is accomplished by connecting an external resistor between Trim and -Sense as shown in Figure 5 and graphed in Figure 8 or by driving the Trim pin with an external voltage as shown in Figure 6. High accuracy setpoints can be achieved with the use of a potentiometer as shown in Figure 7.

Applications

Setting Output Voltage (cont'd)

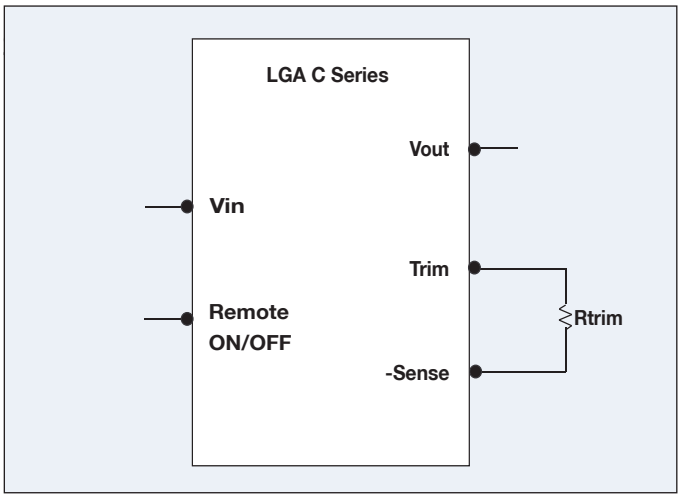


Figure 5 - Output Voltage Trim

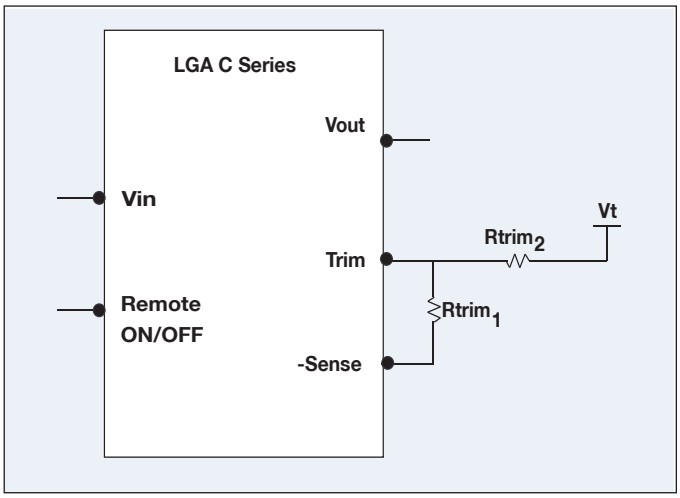


Figure 6 - Output Voltage Trim - with Voltage Source

The trim equation for the basic configuration shown in Figure 5 is:

$$R_{trim}\ (k\Omega) = \frac{1.182}{(Vout - 0.591)}$$

Where Vout is the desired output voltage and Rtrim is the resistance required between the Trim pin and -Sense.

The trim equation for the external voltage configuration shown in Figure 6 is:

$$R_{trim2}\ (k\Omega) = \frac{R_{trim1}\ (1.182 - 2Vt)}{R_{trim1}\ (Vout - 0.591) - 1.182}$$

Where Vout is the desired output voltage, R_{trim1} (kΩ) and R_{trim2} (kΩ) are the resistors in Figure 6 and Vt is the applied external output voltage.

Note: If, Vin ≤ 5 V, V_{pin24} (max) = Vin

If, Vin > 5 V, V_{pin24} (max) = 5 V

Applications (cont'd)

Setting Output Voltage (cont'd)

The trim equation for the potentiometer configuration show in Figure 7.

$$Vout = \frac{0.591}{(Rtrim2 + Rpot)Rtrim1} * (2R_{trim2} + 2R_{pot} + R_{trim1}R_{trim2} + R_{trim1}R_{pot} + 2Rtrim1)$$

Where Vout is the desired output voltage, $R_{trim1}(k\Omega)$ and $R_{trim2}(k\Omega)$ are the resistors in Figure 7 and R_{pot} is the resistance of the potentiometer.

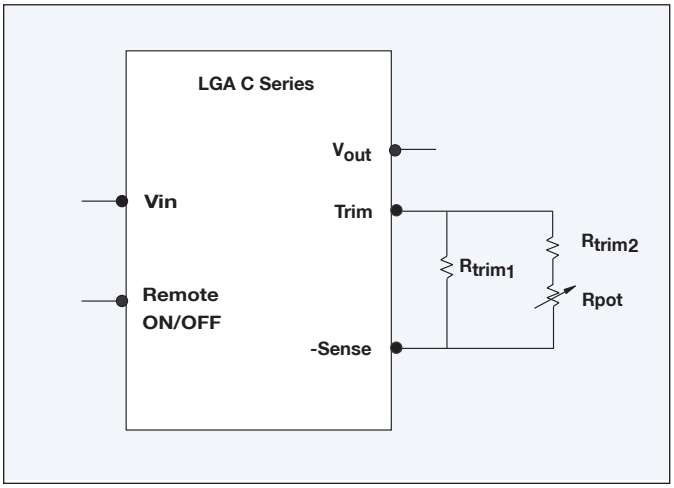


Figure 7 - Output Voltage Trim - with Potentiometer

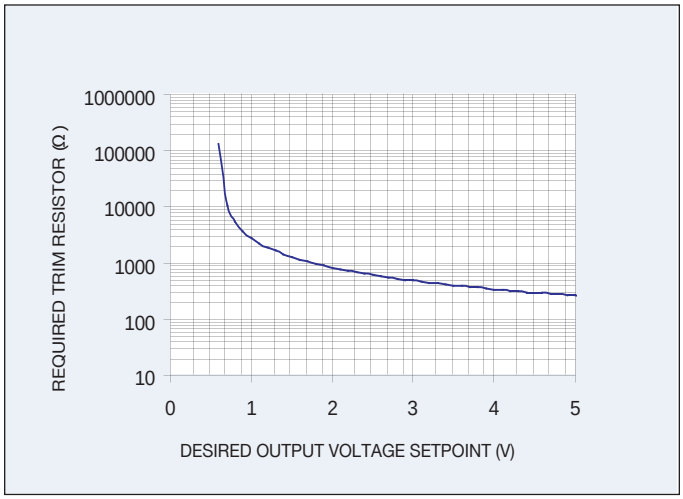


Figure 8 - Typical Trim Curves

Undervoltage Lockout

These EPD's have built-in undervoltage lockout to ensure reliable output power. The lockout prevents the unit from operating when the input voltage is too low. The UVLO for the LGA03/06/10C can be adjusted with the following equation:

$$Ruvlo(k\Omega) = \frac{14.8 * 6.81}{6.81 * V_{turn\_on} - 18.16}$$

The UVLO for the LGA20C can be adjusted with the following equation:

$$Ruvlo(k\Omega) = \frac{30.1 * 4.22}{8.577 * V_{turn\_on} - 34.32}$$

Applications (cont'd)

Output Capacitance

The LGA C Series has output capacitors inside the converter. Limited output capacitance, 10uF for the 3 A/6A/10A and 50 uF for the 20A, is required for stable operation. When powering loads with large dynamic current requirements, improved voltage regulation is obtained by inserting low ESR capacitors as close as possible to the load. Low ESR ceramic capacitors will handle the short duration high frequency components of the dynamic current requirement. In addition, higher values of electrolytic capacitors should be used to handle the mid-frequency components.

It is equally important to use good design practices when configuring the dc distribution system. Low resistance and low inductance PCB layout traces should be utilized, particularly in the high current output section. Remember that the capacitance of the distribution system and the associated ESR are within the feedback loop of the power capabilities, thus affecting the stability and dynamic response of the module. Note that the maximum rated value of output capacitance varies between models and for each output voltage setpoint. A stability vs. Load Capacitance calculator, (see your sales representative), details how an external load capacitance influences the gain and phase margins of the LGA C Series modules.

Setting Margin Control

To margin the output voltage up, pull the margin control pin high. To margin down, pull the margin control pin low. If the pin is left floating, the feature is disabled. The maximum margining range is ±33% of the output voltage setting, with maximum output at 5.5 V. The equations for margining up and down are as follows:

$$V_{margin\_up} = 0.1182 * \frac{R_{margin}}{R_{ofs+}} * \frac{R_{trim} + 2k}{R_{trim}}$$

$$V_{margin\_down} = 0.1182 * \frac{R_{margin}}{R_{ofs-}} * \frac{R_{trim} + 2k}{R_{trim}}$$

Note: The margin control pin cannot be pulled in the following range:

If, Vin ≤ 5V then $V_{margin(max)}$ = Vin
If, Vin > 5V then $V_{margin(max)}$ = 5V

See Table 1 for suggested margining values.

Applications (cont'd)

Setting Margin Control (cont'd)

Margin Up and Down 5%								
Vout_nom (V)	Rtrim (kΩ)	Rmargin (kΩ)	Rofs- (kΩ)	Rofs+ (kΩ)	Vmargin_down (V)	Vout _down (V)	Vmargin_up (V)	Vout_up (V)
0.9	3.83	2.49	10.0	10.0	0.045	0.855	0.045	0.945
1.2	1.96	2.49	10.0	10.0	0.059	1.141	0.059	1.259
1.8	0.976	2.49	10.0	10.0	0.090	1.710	0.090	1.890
2.5	0.619	2.49	10.0	10.0	0.125	2.375	0.125	2.625
3.3	0.432	2.49	10.0	10.0	0.166	3.134	0.166	3.466
5.0	0.267	2.49	10.0	10.0	0.250	4.750	0.250	5.250
Margin Up and Down 10%								
0.9	3.83	4.99	10.0	10.0	0.090	0.810	0.090	0.990
1.2	1.96	4.99	10.0	10.0	0.119	1.081	0.199	1.319
1.8	0.976	4.99	10.0	10.0	0.180	1.620	0.180	1.980
2.5	0.619	4.99	10.0	10.0	0.250	2.250	0.250	2.750
3.3	0.432	4.99	10.0	10.0	0.332	2.968	0.332	3.632
5.0	0.267	4.99	10.0	10.0	0.501	4.499	0.501	5.501

Table 1 - Suggested Margin Values

Water Washing

Water-washing is not recommended.

Interface Finish

Electroless Nickel Immersion Gold (ENIG).

Solder Paste

Solderballs are caused between LGA and substrate due to printing an excessive amount of solderpaste. Stencil apertures should be windowpaned; dividing them into quadrants rather than printing a continuous deposit over the entire pad. This will control the amount of solder available to form a joint between LGA and customer board. Additionally, this will also reduce the formation of voids.

Solder Paste Window Paning

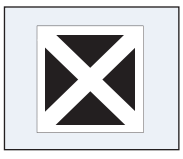


Figure 9: Window Paning

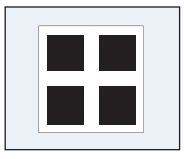


Figure 10: Window Paning

Applications (cont'd)

Recommend Placement Method
Use of a placement machine with front lighting and pad recognition is recommended. For best results, place the LGA based on the centerpoint of the pad array (case silhouetting is not recommended for placement).

Reflow Guidelines
For a SnPb process: pads should be above 183 °C (liquidus) for 90 seconds max (60-75 seconds typical) with a peak temperature of 225 °C. For a leadfree SAC305 process: pads should be above 217 °C (liquidus) for 90 seconds max (60-75 seconds typical) with a peak temperature of 250 °C.

The LGA Series products passed solderability testing per J-STD-002B and IEC-60068-2-58. The test was conducted by Process Sciences, Inc in August, 2007

Thermal Hotspot
The electrical operating conditions of the LGA (shown below) determine how much power is dissipated within the converter.

- Input voltage (Vin)
- Output voltage (Vo)
- Output current (Io)

The following parameters further influence the thermal stresses experienced by the converter:

- Ambient temperature
- Air velocity
- Thermal efficiency of the end system application
- Parts mounted on system PCB that may block airflow
- Real airflow characteristics at the converter location

In order to simplify the thermal design, a number of thermal derating plots are provided in this Technical Reference Note. These derating graphs show the load current of the LGA versus the ambient air temperature and forced air velocity. However, since the thermal performance is heavily dependent upon the final system application, the user needs to ensure the thermal reference point temperatures are kept within the recommended temperature rating. It is recommended that the thermal reference point temperatures are measured using a thermocouple or an IR camera. In order to comply with stringent Emerson Network Power derating criteria the ambient temperature should never exceed 85 °C. The case maximum recommended temperature is 100 °C. Please contact Emerson Network Power for further support.

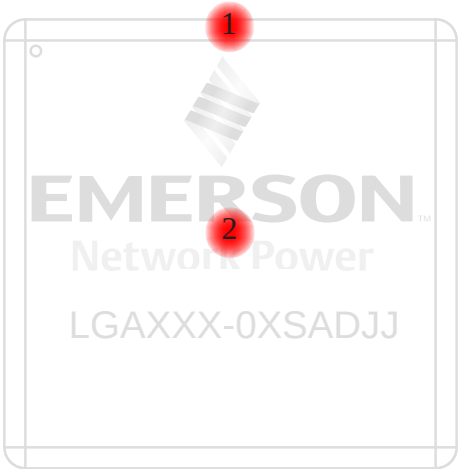


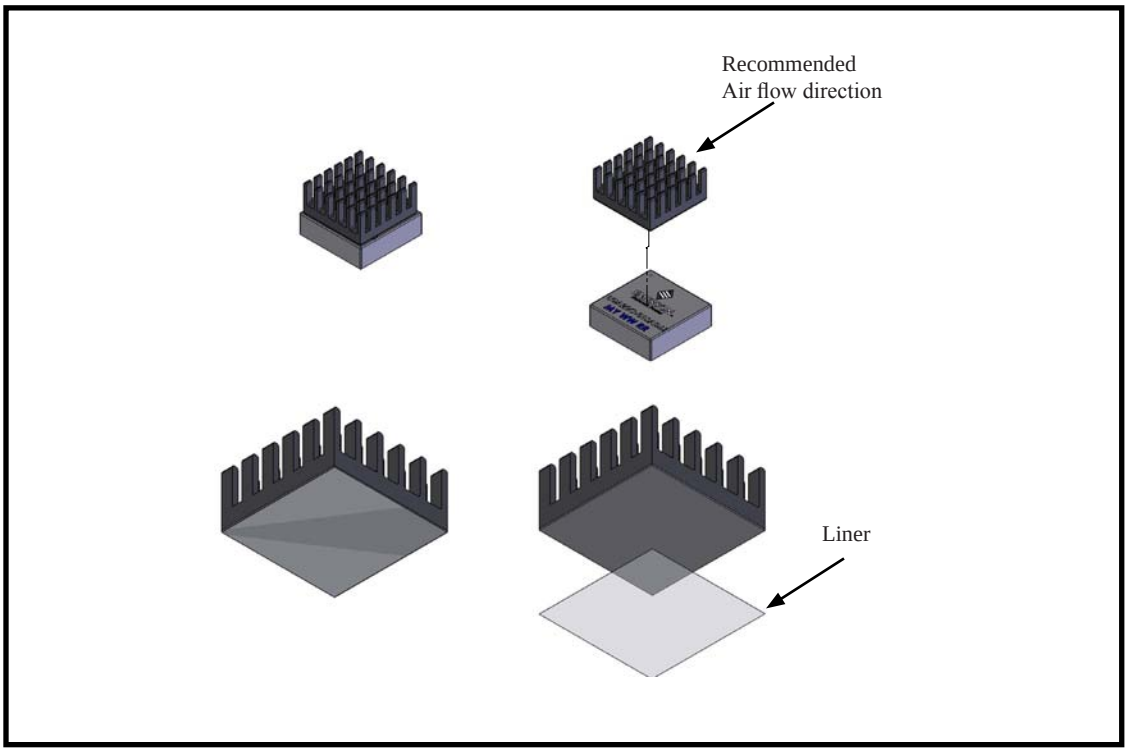
Figure 11: Thermal Hotspots
1: With Heatsink
2: Without Heatsink

Applications (cont'd)

Heatsink Accessory

System should be reflowed before attaching heatsink.

1. Clean the top surface of the case with isopropyl alcohol and ensure the case surface is air-dried.
2. Remove clear plastic liner from bottom of the heatsink to expose the adhesive.
3. Align heatsink with case and apply even pressure (10-15 PSI) for 10-20 seconds.



Heatsink Number System with Options

Product Family		Product		Package		Height*
LGA	-	**HTSK**	-	**KIT**	-	**XXX**
		Product HTSK = Heatsink		**Package** KIT = Heatsink and Adhesive		**LGA20 + Heatsink** 045 = 0.45" 048 = 0.48" 050 = 0.50"

*Height is the total height of the LGA20C-00SADJJ with heatsink attached.

All Models

Parameter	Test Conditions	Min	Typ	Max	Units
Absolute Maximums					
Input Voltage		0		14.0	V
Enable Voltage		0		5	V
Operating Ambient Temperature		-40		85	°C
Non-Operating Ambient Temperature		-40		125	°C
Case Temperature				100	°C
Output Specifications					
Ouput Voltage		0.591		5.1	V
Output Setpoint Accuracy		-1.0		+1.0	%
Output Regulation (Line)		-0.2		+0.2	%
Duty Cycle			90		%
Turn On Specifications					
Turn On Delay (with Vin)			2	3	ms
Turn On Delay (with Enable)			2.0	3	ms
Output Rise TIme	10% - 90%		1.5		ms
Enable Specifications					
Signal Low (Unit Off)		0		0.4	V
Signal Low Current	12 Vin	0	400		uA
Signal High (Unit On)		15			V
Signal High Current			1		uA
Material Ratings					
Flammability			UL94V-0		
Moisture Sensitivity Level			3		
Material Type			FR4 PCB		
International Standards					
Solderability		J-STD-002B IEC-60068-2-58			

LGA03C

Parameter	Test Conditions	Min	Typ	Max	Units
Input Specifications					
Input Voltage	Internal input capacitance rated 16 Vdc max.	3		14.0	V
Input Current (Max)				3	A
Input Current (No Load)	12.0 Vin, 2.5 Vout, 0 Aout		55		mA
Input Current (Standby)	12.0 Vin, Module disabled		14		mA
Input Capacitance (Internal)			10		uF
Input Capacitance (External)	Required for input ripple current		1		uF
Output Specifications					
Output Current		0		3	A
Output Capacitance (Internal)			20		uF
Output Capacitance (External)	12 Vin, 0.9 Vout (Startup capacitance)	10		3,000	uF
	12 Vin, 2.5 Vout (Startup capacitance)	10		1,100	uF
	12 Vin, 5.0 Vout (Startup capacitance)	10		450	uF
Output Ripple/Noise (Peak/Peak)	5 Vin, 0.9 Vout, 10 uF Cout		15		mV
	12 Vin, 2.5 Vout, 10 uF Cout		20		mV
	12 Vin, 5 Vout, 10 uF Cout		30		mV
Efficiency	5 Vin, 0.9 Vout, 3 Aout		79.1		%
	12 Vin, 2.5 Vout, 3 Aout		86.4		%
	12 Vin, 5 Vout, 3 Aout		91.8		%
Dynamic Load Response (Peak Deviation)	12 Vin, 0.9 Vout, 1.5-3 at 5 A/us, 10 uF Cout		85		mV
Dynamic Load Response (Setting Time)	12 Vin, 0.9 Vout, 1.5-3 at 5 A/us, 10 uF Cout		8		us
Dynamic Load Response (Peak Deviation)	12 Vin, 2.5 Vout, 1.5-3 at 5 A/us, 10 uF Cout		95		mV
Dynamic Load Response (Setting Time)	12 Vin, 2.5 Vout, 1.5-3 at 5 A/us, 10 uF Cout		15		us
Protection Specification					
Over Current Protection	Hiccup Mode		6		A
General Specifications					
MTBF	Telcordia SR-332, Method II, Parts Stress, 40 °C Ambient, 400 LFM, 100% Load		28,037,062		Hours
Weight			0.1		oz
Switching Frequency			1,000		kHz
Junction to Case Thermal Resistance			3		°C/W

LGA03C

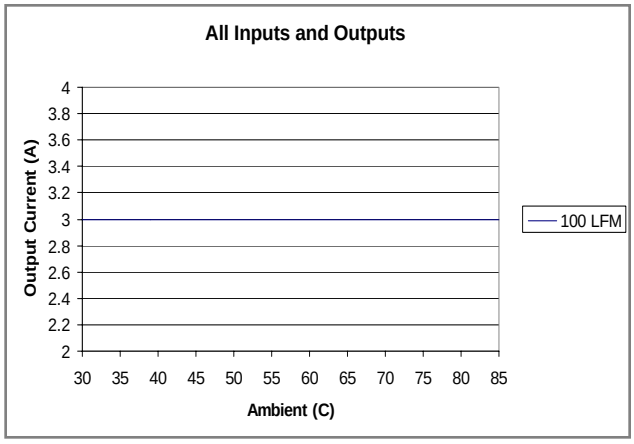


Figure 12: Thermal Derating Curve for All Inputs and Outputs

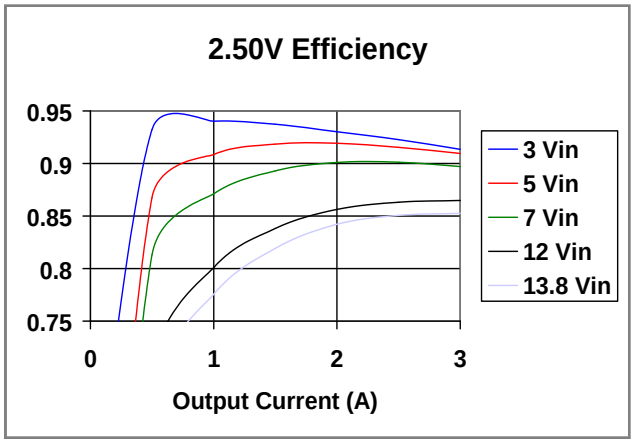


Figure 13: 2.5 V Efficiency vs. Load

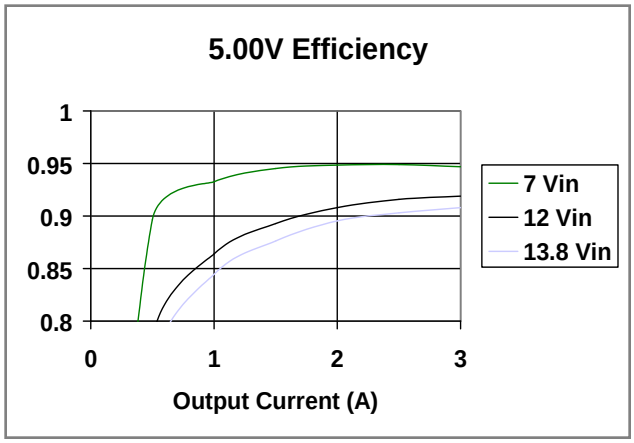


Figure 14: 5 V Efficiency vs. Load

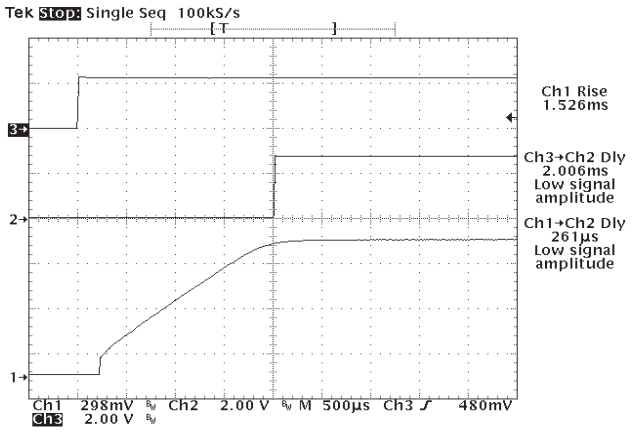


Figure 15: Remote On/Off
(Channel 1: Output Voltage, Channel 2: PGood,
Channel 3: Enable)

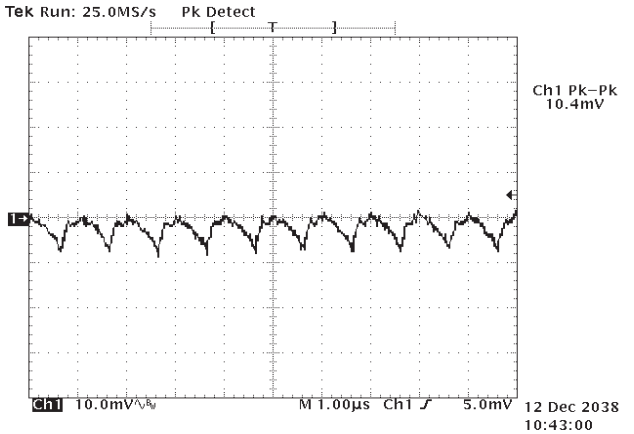


Figure 16: Typical Output Ripple

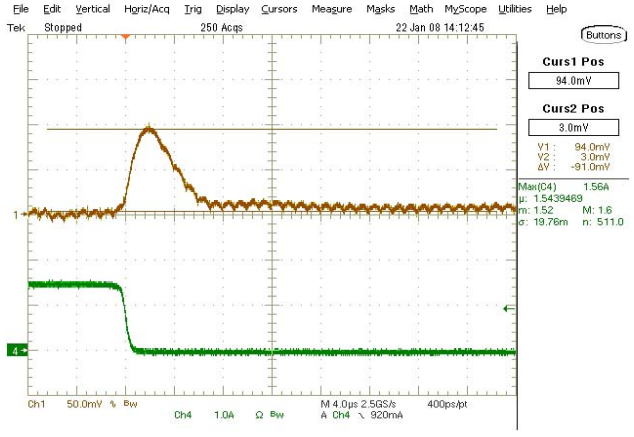


Figure 17: Transient Response 100% - 50%
(Channel 4: Current Step at 1 A/div,
Channel 1: Output Voltage Deviation)

LGA03C

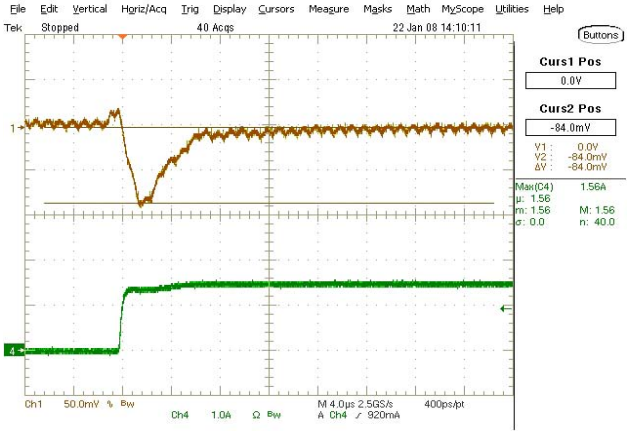


Figure 18: Transient Response 50% - 100%
(Channel 4: Current Step at 1 A/div,
Channel 1: Output Voltage Deviation)

LGA06C

Parameter	Test Conditions	Min	Typ	Max	Units
Input Specifications					
Input Voltage	Internal input capacitance rated 16 Vdc max.	3		14.0	V
Input Current (Max)				6	A
Input Current (No Load)	12.0 Vin, 2.5 Vout, 0 Aout		94		mA
Input Current (Standby)	12.0 Vin, Module disabled		14		mA
Input Capacitance (Internal)			10		uF
Input Capacitance (External)	Required for input ripple current		1		uF
Output Specifications					
Output Current		0		6	A
Output Capacitance (Internal)			20		uF
Output Capacitance (External)	12 Vin, 0.9 Vout (Startup capacitance)	10		7,500	uF
	12 Vin, 2.5 Vout (Startup capacitance)	10		1,500	uF
	12 Vin, 5.0 Vout (Startup capacitance)	10		750	uF
Output Ripple/Noise (Peak/Peak)	5 Vin, 0.9 Vout, 10 uF Cout		20		mV
	12 Vin, 2.5 Vout, 10 uF Cout		35		mV
	12 Vin, 5 Vout, 10 uF Cout		50		mV
Efficiency	5 Vin, 0.9 Vout, 6 Aout		80.1		%
	12 Vin, 2.5 Vout, 6 Aout		86.5		%
	12 Vin, 5 Vout, 6 Aout		92.1		%
Dynamic Load Response (Peak Deviation)	12 Vin, 0.9 Vout, 3-6 at 5 A/us, 10 uF Cout		125		mV
Dynamic Load Response (Setting Time)	12 Vin, 0.9 Vout, 3-6 at 5 A/us, 10 uF Cout		8		us
Dynamic Load Response (Peak Deviation)	12 Vin, 2.5 Vout, 3-6 at 5 A/us, 10 uF Cout		175		mV
Dynamic Load Response (Setting Time)	12 Vin, 2.5 Vout, 3-6 at 5 A/us, 10 uF Cout		8		us
Protection Specification					
Over Current Protection	Hiccup Mode		11		A
General Specifications					
MTBF	Telcordia SR-332, Method II, Parts Stress, 40 °C Ambient, 400 LFM, 100% Load		27,141,984		Hours
Weight			0.1		oz
Switching Frequency			1,000		kHz
Junction to Case Thermal Resistance			3		°C/W

LGA06C

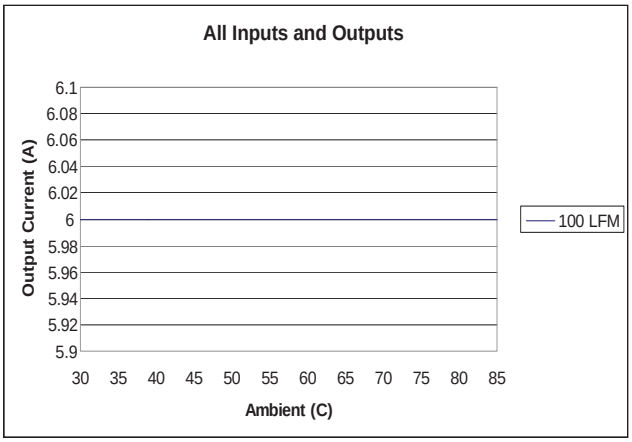


Figure 19: Thermal Derating Curve for All Inputs and Outputs

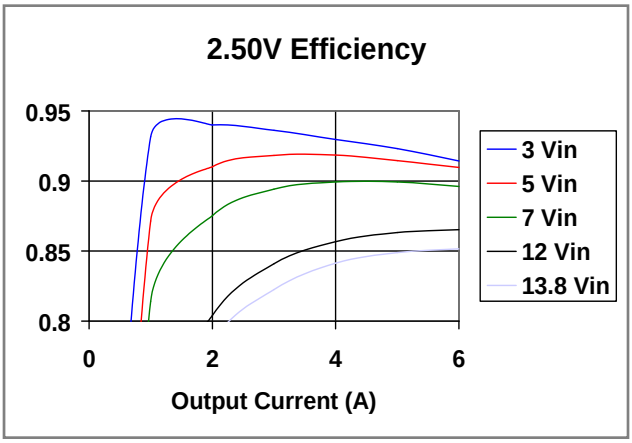


Figure 20: 2.5 V Efficiency vs. Load

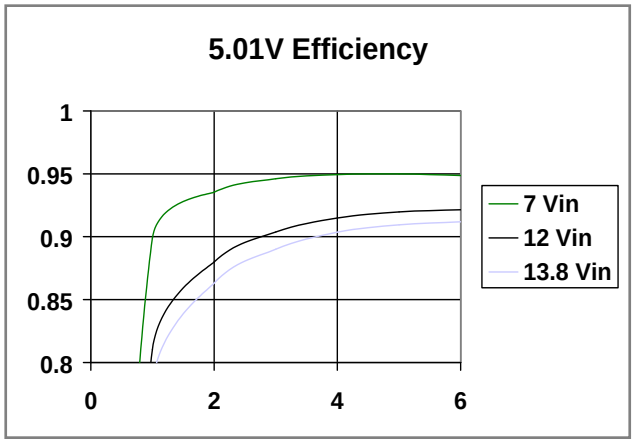


Figure 21: 5 V Efficiency vs. Load

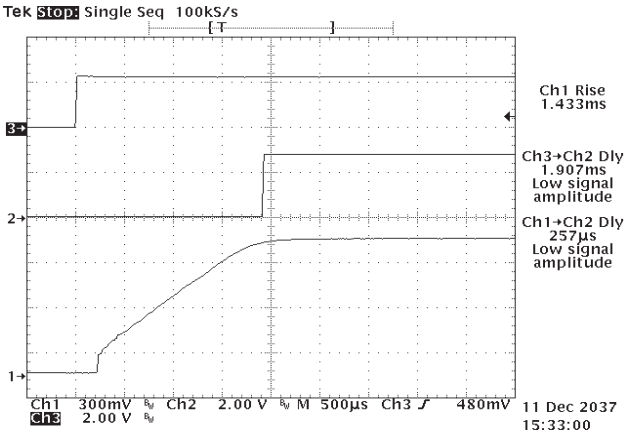


Figure 22: Remote On/Off
(Channel 1: Output Voltage, Channel 2: PGood,
Channel 3: Enable)

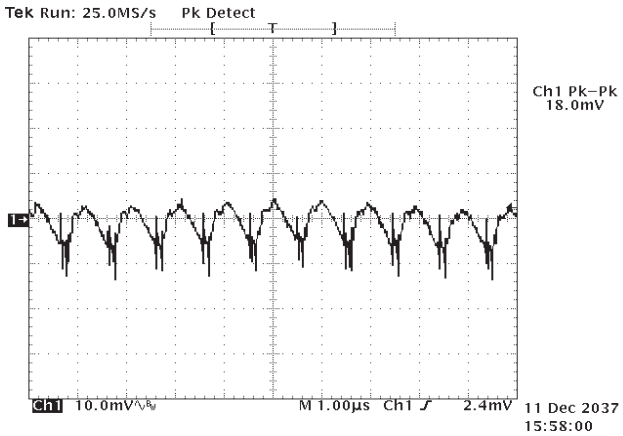


Figure 23: Typical Output Ripple

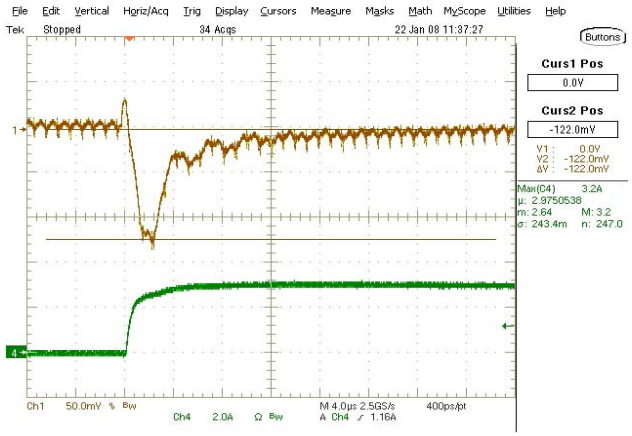


Figure 24: Transient Response 100% - 50%
(Channel 4: Current Step at 2 A/div,
Channel 1: Output Voltage Deviation)

LGA06C

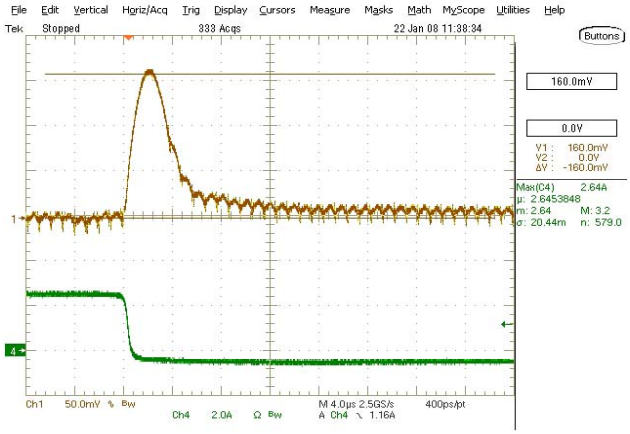


Figure 25: Transient Response 50% - 100%
(Channel 4: Current Step at 2 A/div,
Channel 1: Output Voltage Deviation)

LGA10C

Parameter	Test Conditions	Min	Typ	Max	Units
Input Specifications					
Input Voltage	Internal input capacitance rated 16 Vdc max.	3		14.0	V
Input Current (Max)				10	A
Input Current (No Load)	12.0 Vin, 2.5 Vout, 0 Aout		100		mA
Input Current (Standby)	12.0 Vin, Module disabled		14		mA
Input Capacitance (Internal)			10		uF
Input Capacitance (External)	Required for input ripple current		1		uF
Output Specifications					
Output Current		0		10	A
Output Capacitance (Internal)			20		uF
Output Capacitance (External)	12 Vin, 0.9 Vout (Startup capacitance)	10		7,500	uF
	12 Vin, 2.5 Vout (Startup capacitance)	10		2,400	uF
	12 Vin, 5.0 Vout (Startup capacitance)	10		1,200	uF
Output Ripple/Noise (Peak/Peak)	5 Vin, 0.9 Vout, 10 uF Cout		30		mV
	12 Vin, 2.5 Vout, 10 uF Cout		40		mV
	12 Vin, 5 Vout, 10 uF Cout		45		mV
Efficiency	5 Vin, 0.9 Vout, 10 Aout		76.6		%
	12 Vin, 2.5 Vout, 10 Aout		85.9		%
	12 Vin, 5 Vout, 10 Aout		91.7		%
Dynamic Load Response (Peak Deviation)	12 Vin, 0.9 Vout, 5-10 at 5 A/us, 10 uF Cout		90		mV
Dynamic Load Response (Setting Time)	12 Vin, 0.9 Vout, 5-10 at 5 A/us, 10 uF Cout		8		us
Dynamic Load Response (Peak Deviation)	12 Vin, 2.5 Vout, 5-10 at 5 A/us, 10 uF Cout		135		mV
Dynamic Load Response (Setting Time)	12 Vin, 2.5 Vout, 5-10 at 5 A/us, 10 uF Cout		8		us
Protection Specification					
Over Current Protection	Hiccup Mode		20		A
General Specifications					
MTBF	Telcordia SR-332, Method II, Parts Stress, 40 °C Ambient, 400 LFM, 100% Load		27,141,984		Hours
Weight			0.1		oz
Switching Frequency			1,000		kHz
Junction to Case Thermal Resistance			9		°C/W

LGA10C

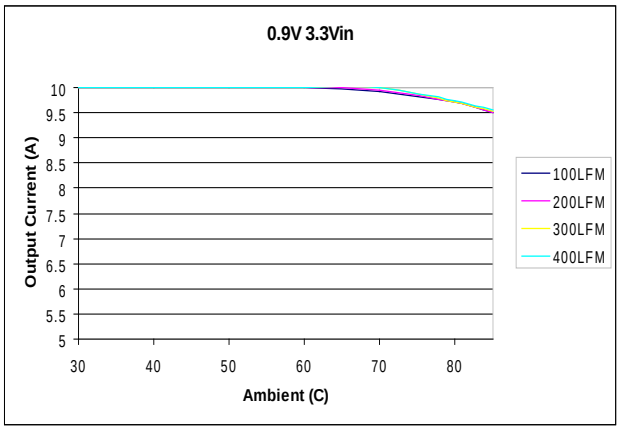


Figure 26: Thermal Derating Curve - 0.9 V

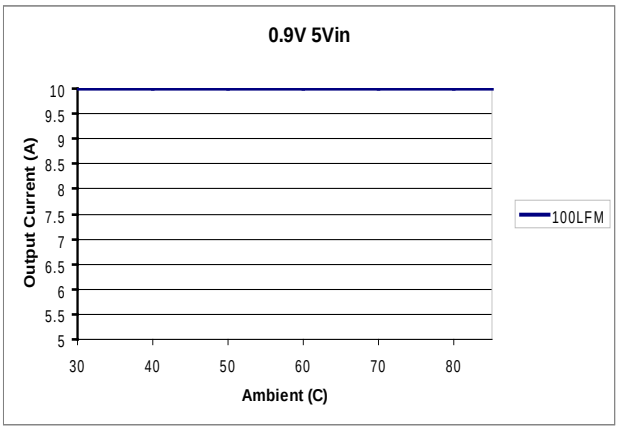


Figure 27: 2 Thermal Derating Curve - 0.9 V

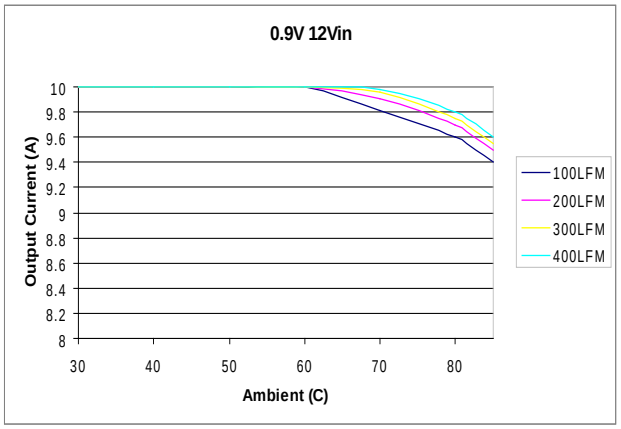


Figure 28: Thermal Derating Curve - 0.9 V

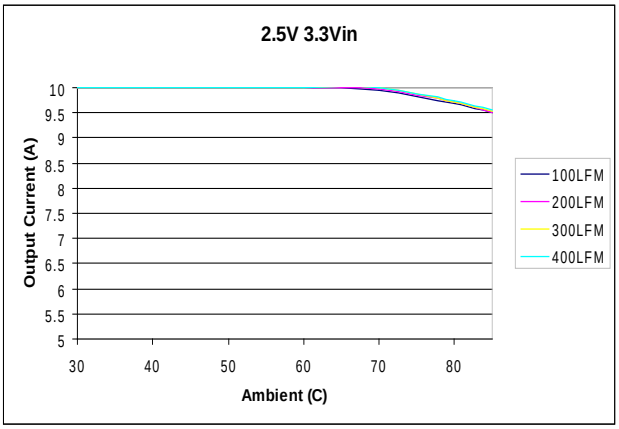


Figure 29: Thermal Derating Curve - 2.5 V

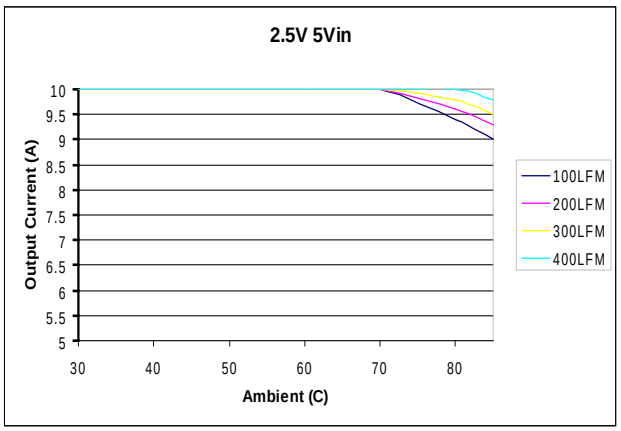


Figure 30: Thermal Derating Curve - 2.5 V

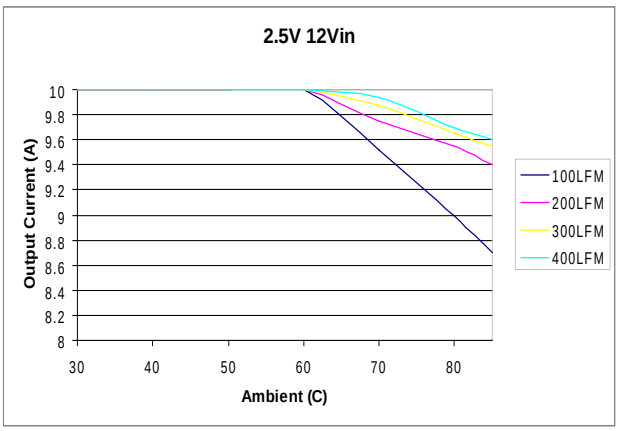


Figure 31: Thermal Derating Curve - 2.5 V

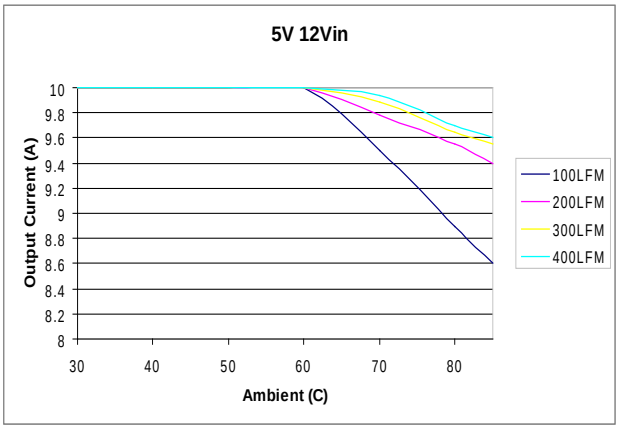


Figure 32: Thermal Derating Curve - 5 V

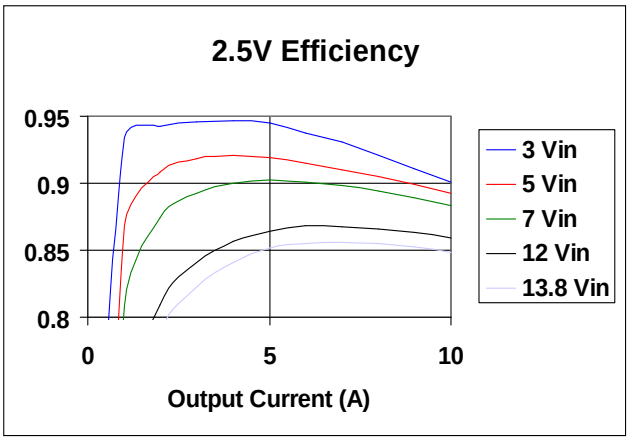


Figure 33: 2.5 V Efficiency vs. Load

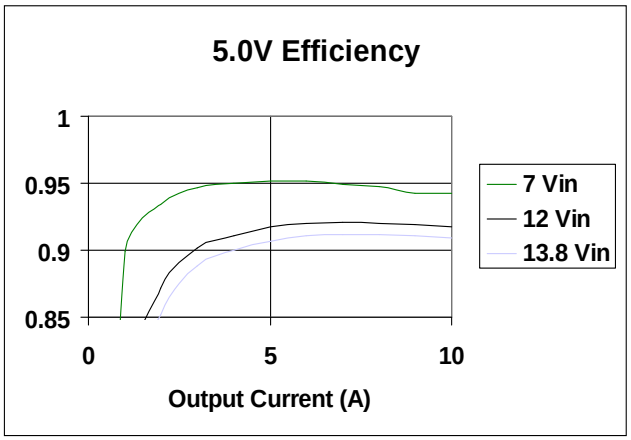


Figure 34: 5 V Efficiency vs. Load

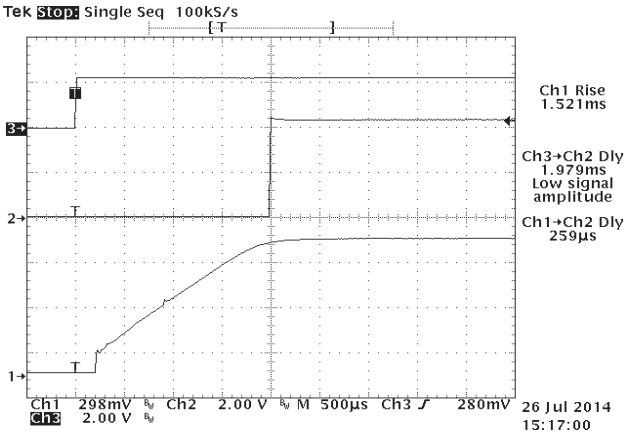


Figure 35: Remote On/Off
(Channel 1: Output Voltage, Channel 2: PGood,
Channel 3: Enable)

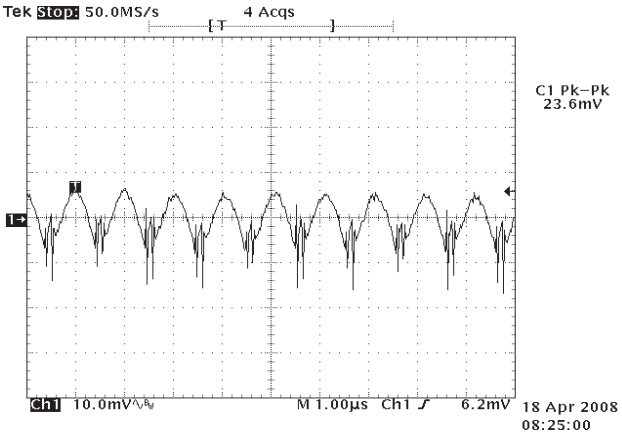


Figure 36: Typical Output Ripple

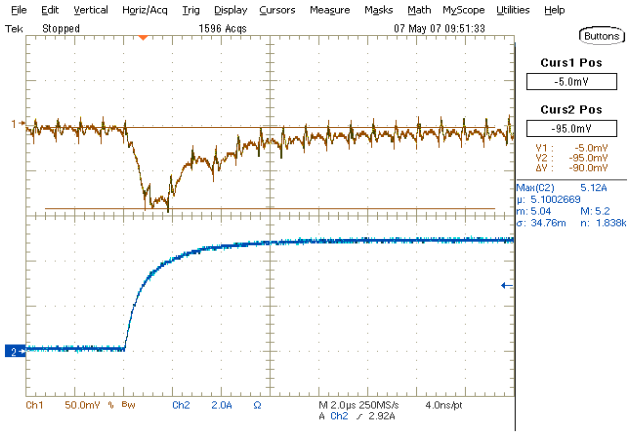


Figure 37: Transient Response 100% - 50%
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 2 A/div)

LGA10C

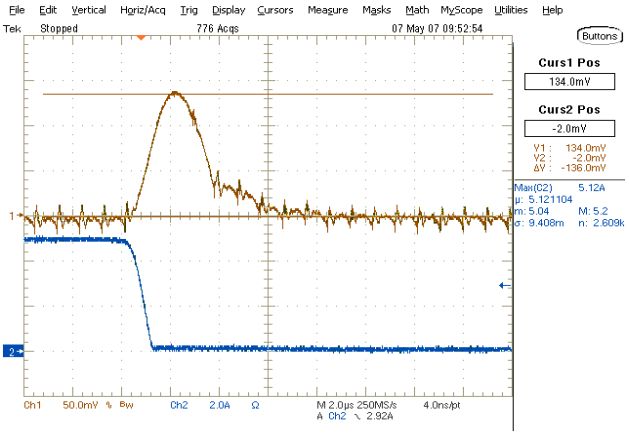


Figure 38: Transient Response 50% - 100%
(Channel 1: Output Voltage Deviation,
Channel 2: Current Step at 2 A/div)

LGA20C

Parameter	Test Conditions	Min	Typ	Max	Units
Input Specifications					
Input Voltage	Internal input capacitance rated 16 Vdc max.	4.5		14.0	V
Input Current (Max)				20	A
Input Current (No Load)	12.0 Vin, 2.5 Vout, 0 Aout		87		mA
Input Current (Standby)	12.0 Vin, Module disabled		13		mA
Input Capacitance (Internal)			10		uF
Input Capacitance (External)	Required for input ripple current		10		uF
Output Specifications					
Output Current		0		20	A
Output Capacitance (Internal)			20		uF
Output Capacitance (External)	12 Vin, 0.9 Vout (Startup capacitance)	50		7,500	uF
	12 Vin, 2.5 Vout (Startup capacitance)	50		2,400	uF
	12 Vin, 5.0 Vout (Startup capacitance)	50		500	uF
Output Ripple/Noise (Peak/Peak)	5 Vin, 0.9 Vout, 10 uF Cout		25		mV
	12 Vin, 2.5 Vout, 10 uF Cout		45		mV
	12 Vin, 5 Vout, 10 uF Cout		70		mV
Efficiency	5 Vin, 0.9 Vout, 20 Aout		77.3		%
	12 Vin, 2.5 Vout, 20 Aout		86.6		%
	12 Vin, 5 Vout, 20 Aout		91.2		%
Dynamic Load Response (Peak Deviation)	12 Vin, 0.9 Vout, 10-20 at 5 A/us, 50 uF Cout		95		mV
Dynamic Load Response (Setting Time)	12 Vin, 0.9 Vout, 10-20 at 5 A/us, 50 uF Cout		12		us
Dynamic Load Response (Peak Deviation)	12 Vin, 2.5 Vout, 10-20 at 5 A/us, 50 uF Cout		175		mV
Dynamic Load Response (Setting Time)	12 Vin, 2.5 Vout, 10-20 at 5 A/us, 50 uF Cout		20		us
Protection Specification					
Over Current Protection	Hiccup Mode		27		A
General Specifications					
MTBF	Telcordia SR-332, Method II, Parts Stress, 40 °C Ambient, 400 LFM, 100% Load		28,388,596		Hours
Weight			0.1		oz
Switching Frequency			800		kHz
Junction to Case Thermal Resistance			2		°C/W

LGA20C

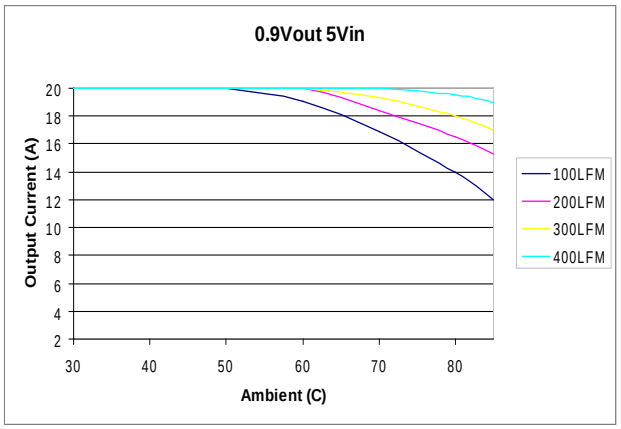


Figure 39: Thermal Derating Curve (5 Vin - 0.9 Vout)

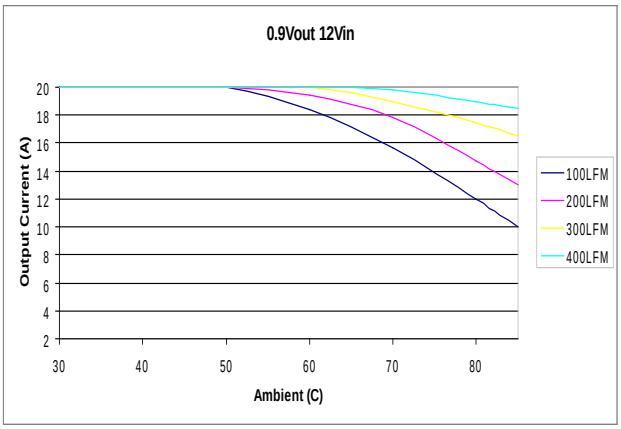


Figure 40: Thermal Derating Curve (12 Vin - 0.9 Vout)

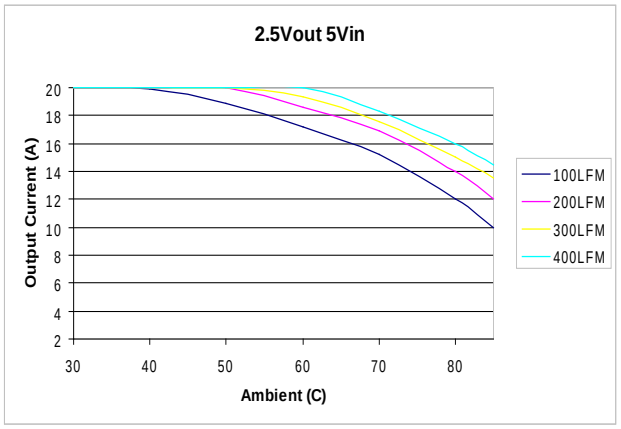


Figure 41: Thermal Derating Curve (5 Vin - 2.5 Vout)

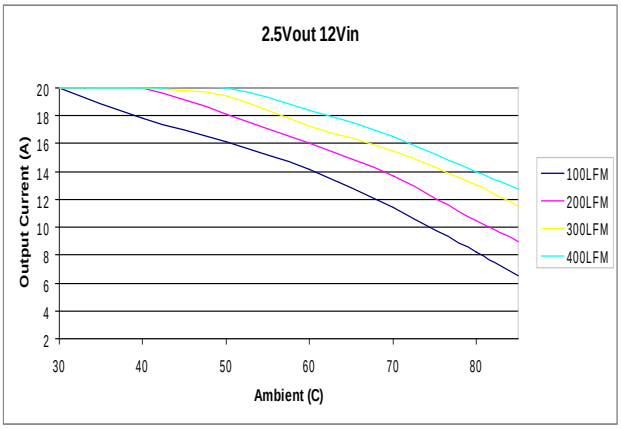


Figure 42: Thermal Derating Curve (12 Vin - 2.5 Vout)

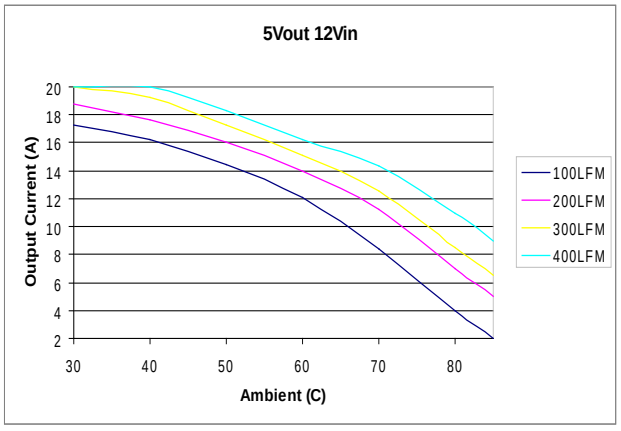


Figure 43: Thermal Derating Curve (12 Vin - 5 Vout)

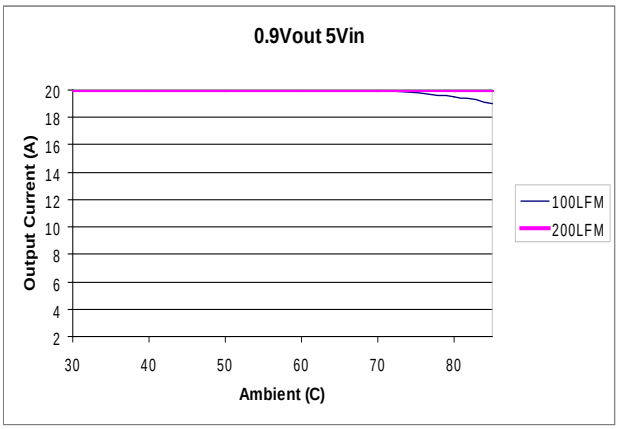


Figure 44: Thermal Derating Curve (5 Vin - 0.9 Vout) with 0.5" Heatsink

LGA20C

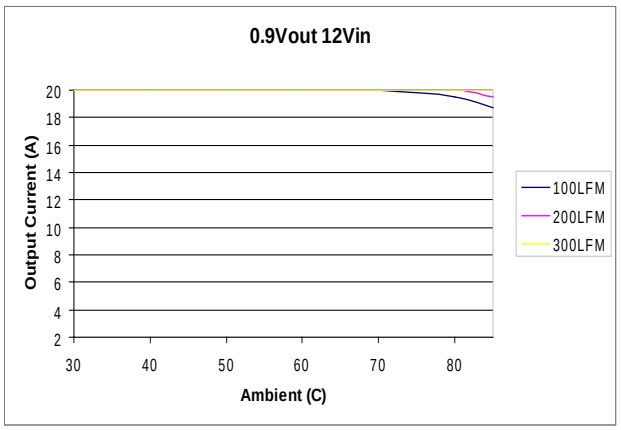


Figure 45: Thermal Derating Curve (12 Vin - 0.9 Vout) with 0.5" Heatsink

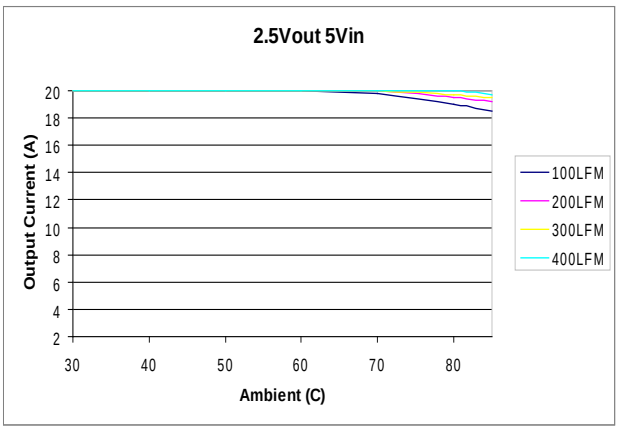


Figure 46: Thermal Derating Curve (5 Vin - 2.5 Vout) with 0.5" Heatsink

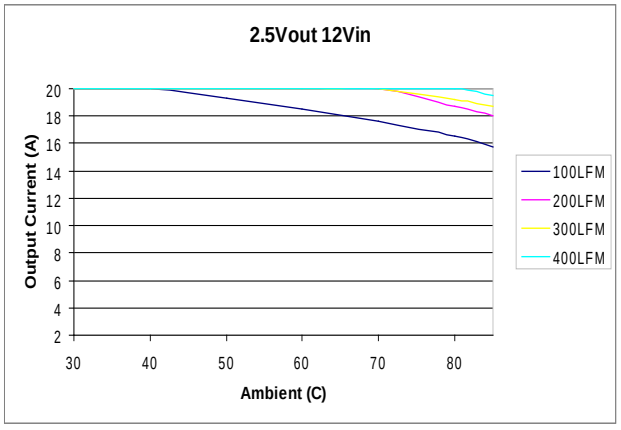


Figure 47: Thermal Derating Curve (12 Vin - 2.5 Vout) with 0.5" Heatsink

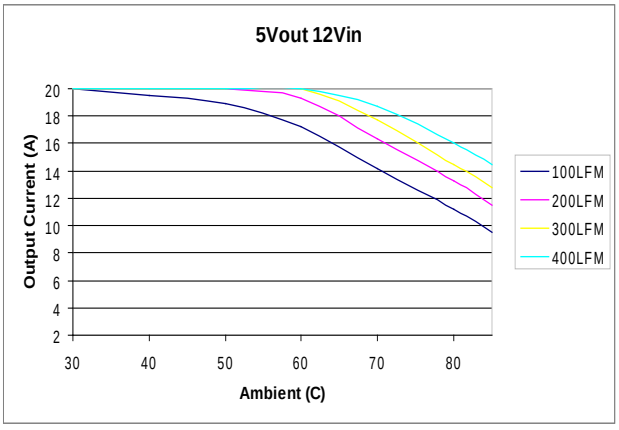


Figure 48: Thermal Derating Curve (12 Vin - 5 Vout) with 0.5" Heatsink

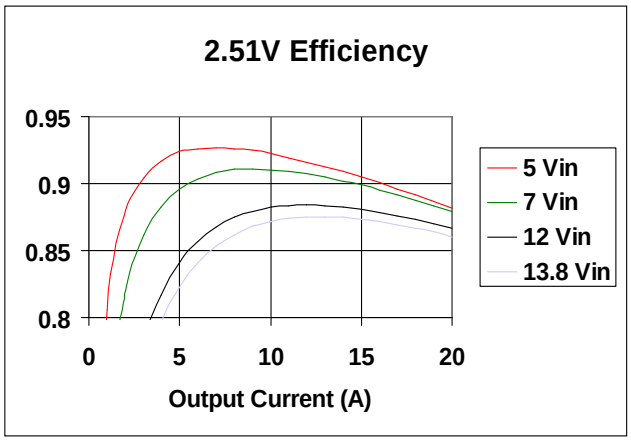


Figure 49: 2.5 V Efficiency vs. Load

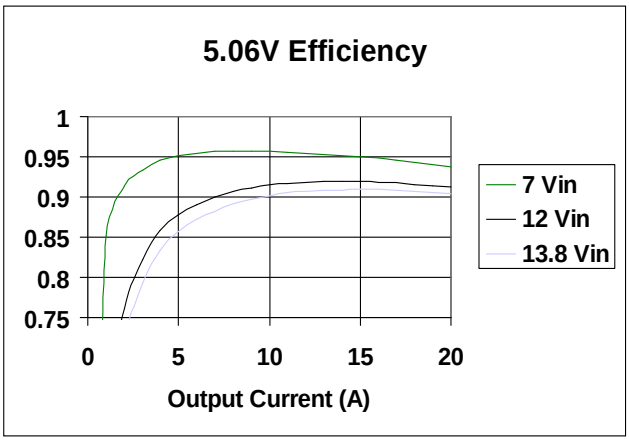


Figure 50: 5 V Efficiency vs. Load

LGA20C

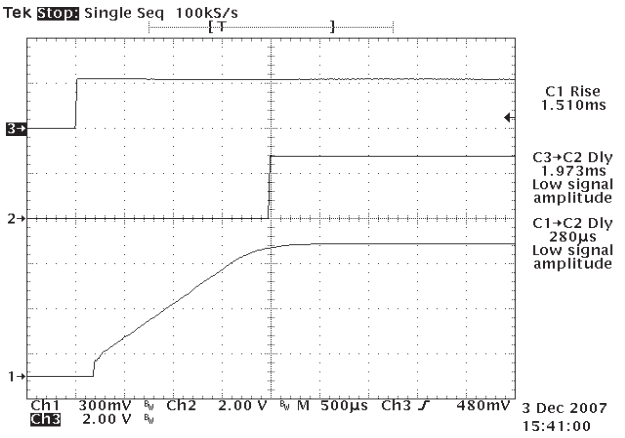


Figure 51: Remote On/Off
(Channel 1: Output Voltage, Channel 2: PGood,
Channel 3: Enable)

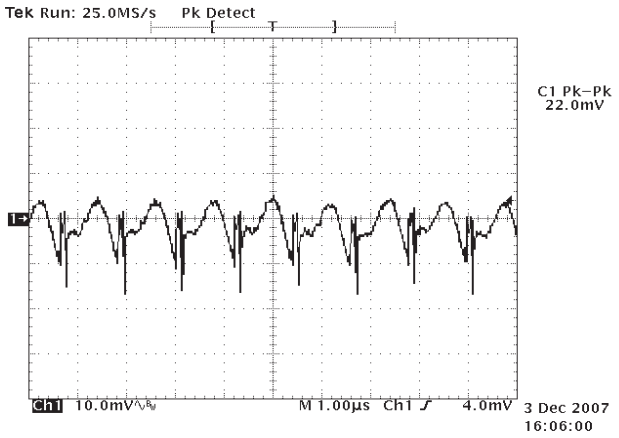


Figure 52: Typical Output Ripple

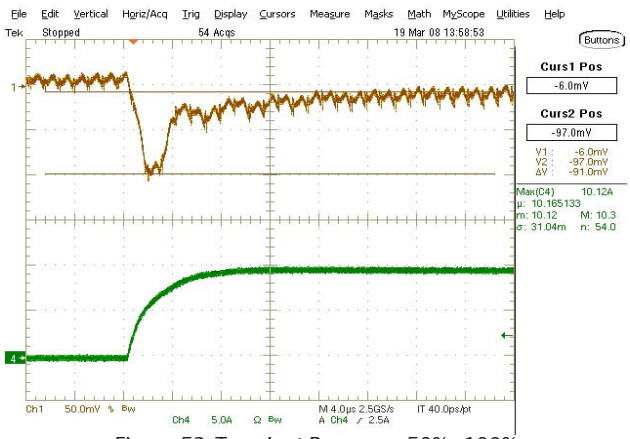


Figure 53 Transient Response 50% - 100%
(Channel 1: Output Voltage Deviation,
Channel 4: Current Step at 5 A/div)

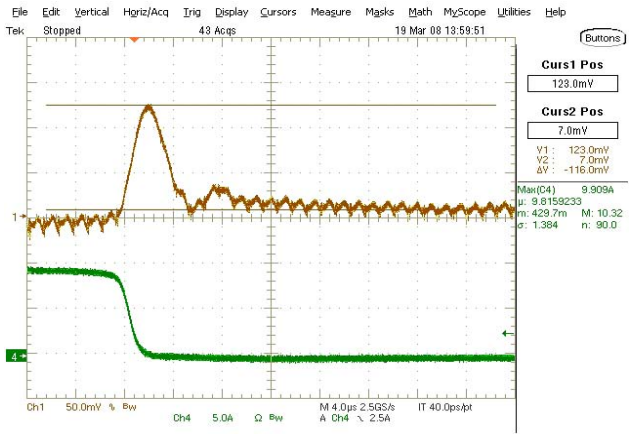
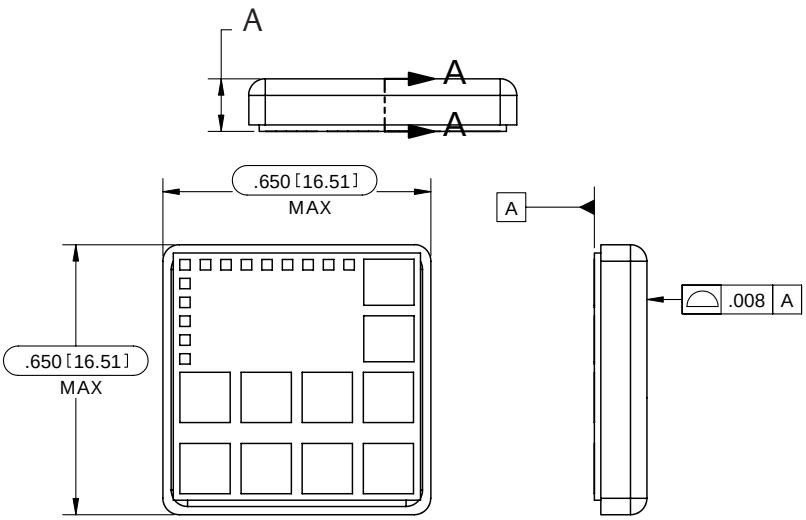


Figure 54: Transient Response 100% - 50%
(Channel 1: Output Voltage Deviation,
Channel 4: Current Step at 5 A/div)

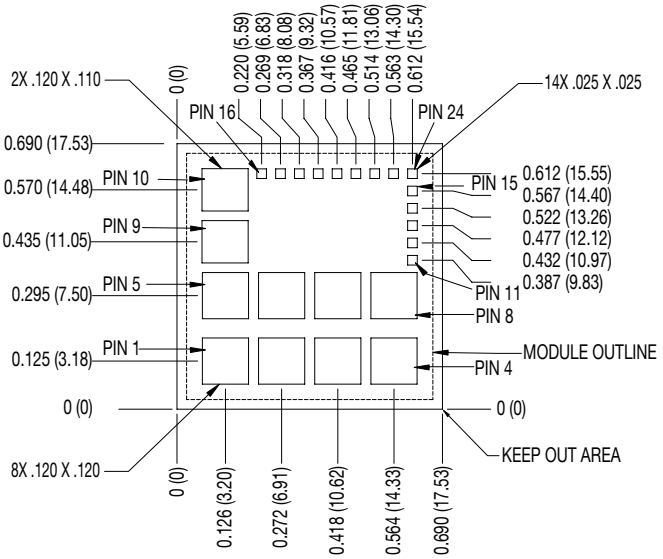
Mechanical drawings



Component Height	
Model #	DIM A in (mm)
LGA03 LGA06 LGA10	0.129 (3.27)
LGA20	0.210 (5.33)

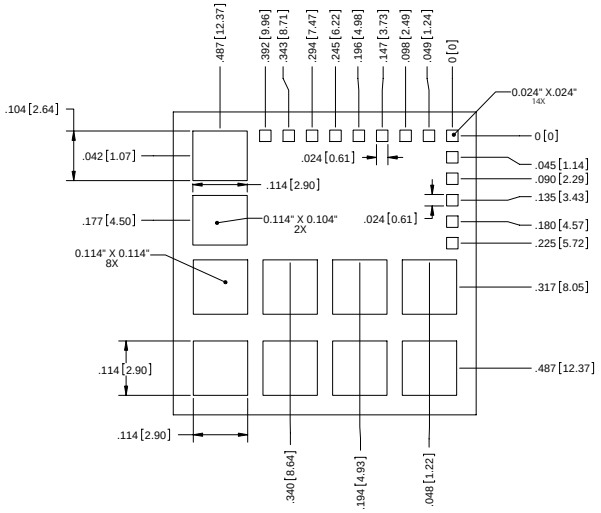
Recommended Application

System Board Footprint



Solder Paste Stencil

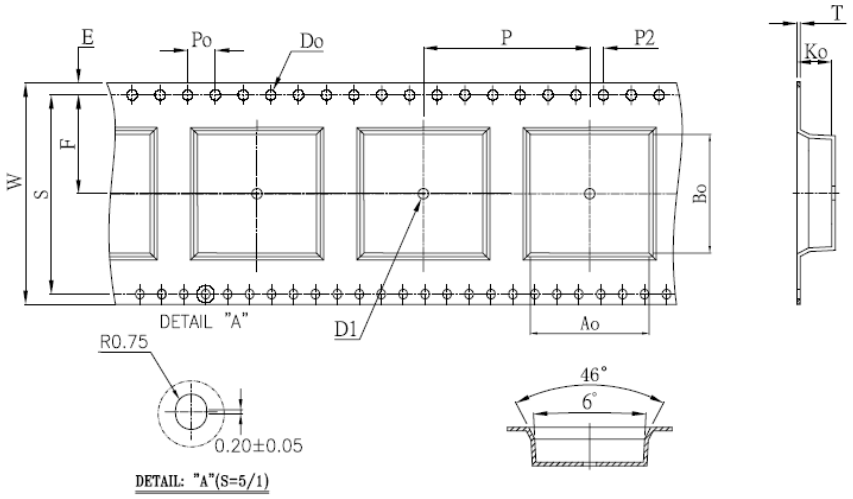
Recommend Stencil thickness of 6 mil
(see window paning on page 9)



Tolerance Note: ± 0.010 (0.25)

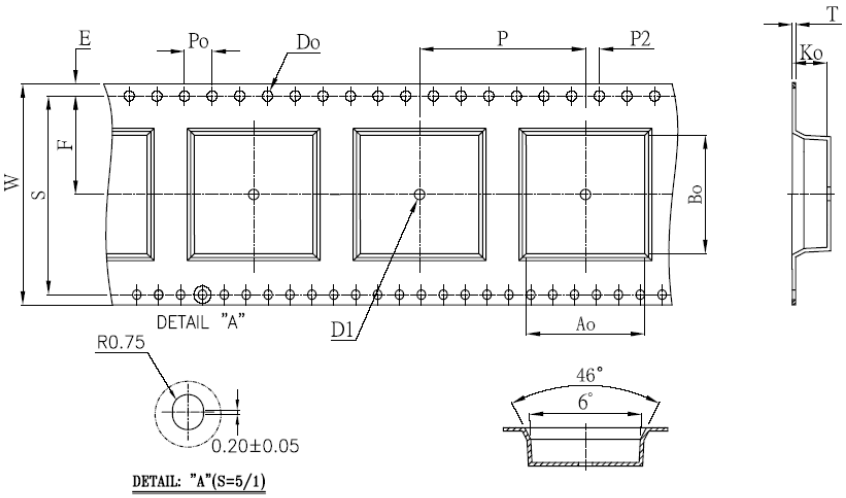
Packaging

LGA03C, 06C, 10C



EIA DIMENSIONS	
W	32.0 ±0.30
E	1.75 ±0.10
F	14.2 ±0.10
So	28.4 ±0.10
P	24.0 ±0.10
Po	4.0 ±0.10
P2	2.0 ±0.10
Do	Ø 1.5 +0.10 -0.00
D1	Ø 2.0 MIN
T	0.40 ±0.05
Ao	16.6 ±0.10
Bo	16.7 ±0.10
Ko	3.7 ±0.10

LGA20C



EIA DIMENSIONS	
W	32.0 ±0.30
E	1.75 ±0.10
F	14.2 ±0.10
So	28.4 ±0.10
P	24.0 ±0.10
Po	4.0 ±0.10
P2	2.0 ±0.10
Do	Ø 1.5 +0.10 -0.00
D1	Ø 2.0 MIN
T	0.40 ±0.05
Ao	16.8 ±0.10
Bo	16.8 ±0.10
Ko	5.8 ±0.10

Notes:

a) T&R packaging comes in Standard 13" reel size.

b) Tape material: Black, Anti-static Polystyrene Amine free.

c) Surface Resistivity: $<10^{12}$ Ohms/Sq

d) Module quanity/reel:

LGA03C, LGA06C, LGA10 C	= 600 pcs
LGA20C	= 450pcs.

e) Products are MSL 3.

Model Number System with Options

Product Family	Rated Output Current	Performance		Input Voltage	Type of Output	Options	RoHS Compliance
LGA	**XX**	**C**	**-**	**XX**	**SADJ**	**X**	**J**
Land Grid Array	**Rated Output Current** 03 = 3 Amp 06 = 6 Amp 10 = 10 Amp 20 = 20 Amp	**Performance** C = Cost Optimized		**Input Voltage** 00 = 3-14.0 V 01 = 4.5-14.0 V	**Type of Output** Single Adjustable Output	**Options** X = Various Options (see Sales Rep)	**RoHS Compliance** J = Pb free (RoHS 6/6 compliant)

Heatsink Number System with Options

Product Family		Product		Package		Height*
LGA	**-**	**HTSK**	**-**	**KIT**	**-**	**XXX**
Land Grid Array		**Product** HTSK = Heatsink		**Package** Heatsink and Adhesive		**LGA20 + Heatsink** 045 = 0.45" 048 = 0.48" 050 = 0.50"

*Height is the total height of the LGA20C-00SADJJ with heatsink attached.

Operating Information

Output Power (Max.)	Input Voltage	Output Voltage	Output Current (Min.)	Output Current (Max.)	Efficiency (Typical)	Regulation Load	Standard Model Numbers
15 W	3-14.0 Vdc	0.59-5.1 Vdc	0 A	3 A	92%	±0.5%	LGA03C-00SADJJ
30 W	3-14.0 Vdc	0.59-5.1 Vdc	0 A	6 A	92%	±0.5%	LGA06C-00SADJJ
50 W	3-14.0 Vdc	0.59-5.1 Vdc	0 A	10 A	92%	±0.5%	LGA10C-00SADJJ
100 W	4.5-14.0 Vdc	0.59-5.1 Vdc	0 A	20 A	91%	±0.5%	LGA20C-01SADJJ
NA	NA	NA	NA	NA	NA	NA	LGA-HTSK-KIT-XXX

Pin Chart

Pin Assignments

Single Output

1	Vout	9	Vin	17	NC
2	Vout	10	Vin	18	NC
3	Vout	11	NC	19	NC
4	Vout	12	- Offset	20	NC
5	GND	13	+ Offset	21	Enable
6	GND	14	- Sense	22	Power Good
7	GND	15	+ Sense	23	Margin Control
8	GND	16	NC	24	Trim

This is a Preliminary Datasheet. Emerson Network Power reserves the right to make changes to the information contained herein without notice and assumes no liability as a result of its use or application.

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