GSC24BC01/02/04/08/16

2-wire Serial EEPROMs 1K/2K/4K/8K/16K

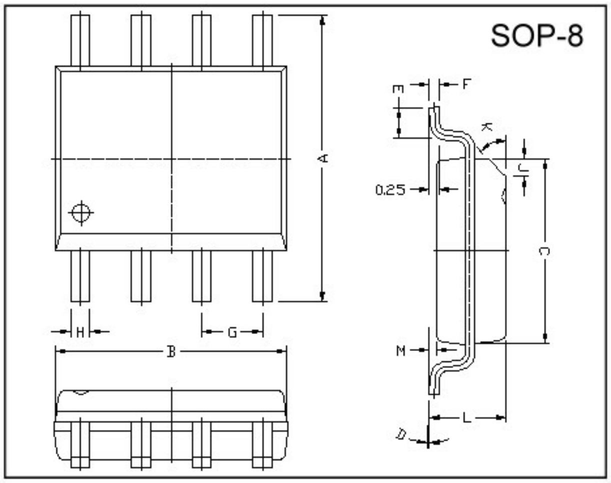
Description

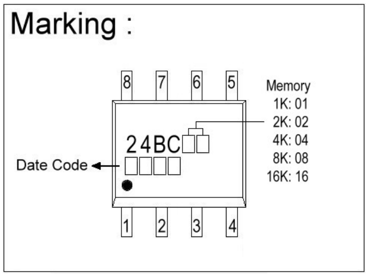
The GSC24BC family provides 1K, 2K, 4K, 8K and 16K of serial electrically erasable and programmable read-only memory (EEPROM). The wide Vdd range allows for low-voltage operation down to 1.8V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The device is accessed via a 2-wire serial interface.

Features

- Internally organized as 128x8 (1K), 256x8 (2K) 512x8 (4K), 1024x8 (8K), 2048x8 (16K),
- Low-voltage and standard-voltage operation: 1.8V~5.5V
- 2-wire serial interface bus
- Date retention: 100years
- High endurance: 1,000,000 Write Cycles
- 100KHz (1.8V) & 400KHz (5V) compatibility
- Bi-directional data transfer protocol
- Self-timed write cycle (5ms max)
- Write protect pin for hardware data protection
- 8-byte page (1K, 2K) and 16-byte page (4K,8K,16K) write modes
- Allows for partial page write

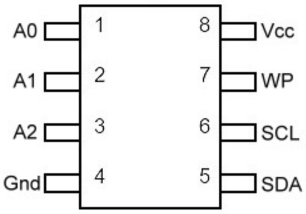
Package Dimensions





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Figure 1. Pin Configurations



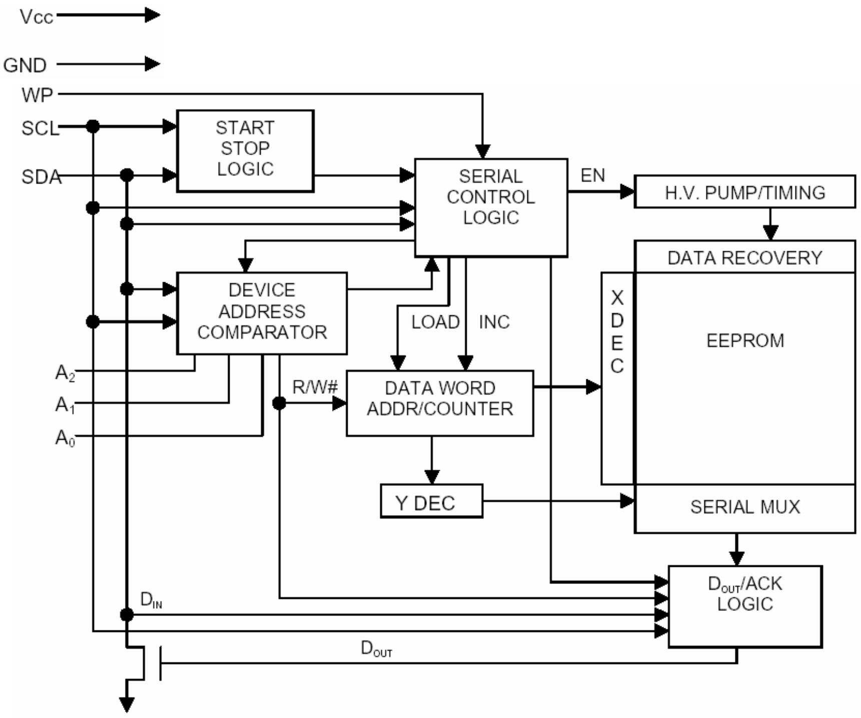
Pin Name	Function
A0 – A2	Address inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
Gnd	Ground
Vcc	Power Supply

Absolute Maximum Ratings

Parameter	Ratings	Unit
Voltage on Any Pin with Respect to Ground	-0.8 to Vcc +1.5	V
Maximum Operating Voltage	6.25	V
DC Output Current	5.0	mA
Operating Temperature Range	-55 ~ +125	℃
Storage Temperature Range	-65 ~ +150	℃

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of these specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram


Vcc
GND
WP
SCL
SDA
START STOP LOGIC
SERIAL CONTROL LOGIC
EN
H.V. PUMP/TIMING
DATA RECOVERY
DEVICE ADDRESS COMPARATOR
LOAD
INC
X DEC
EEPROM
A2
A1
A0
R/W#
DATA WORD ADDR/COUNTER
Y DEC
SERIAL MUX
DOUT/ACK LOGIC
DIN
DOUT

PIN Descriptions

Serial Data (SDA): The SDA pin used for sending and receiving data bits in serial mode. Since the SDA pin is defined as an open-drain connection, a pull-up resistor is needed.

Serial Clock (SCL): The SCL input is used to synchronize data input and output with the clocked out on the falling edge of SCL.

Device/Page Addresses (A2, A1, A0): The A2, A1, and A0 pins are used to address multiple devices on a single bus system and should be hard-wired.

The GSC24BC01 and GSC24BC02 use the A2, A1 and A0 pins to provide the capability for addressing up to eight 1K/2K devices on a single bus system (please see the Device Addressing section for further details)

- The GSC24BC04 uses the A2 and A1 inputs and a total of for 4K device may be addressed on a single bus system. The A0 pin in not used, but should be grounded if possible.
- The GSC24BC08 only uses the A2 input hardwire addressing. On a single bus system, a total of two 8K devices may be addressed. The A0 and A1 pins are not used, but should be grounded if possible.
- The GSC24BC16 does not uses the device address pins, so only one device can be connected to a single bus system. Therefore, the A0, A1 and A2 pins are not used, but should be grounded if possible.

Write Protect (WP): The GSC24BC01/02/04/08/16 has a Write Protect pin that provides hardware data protection. When connected to ground, the Write Protect pin allows for normal read/write operations. If the WP pin is connected to Vcc, no data can be overwritten.

Memory Organization

The internal memory organization for the GSC24BC family is arranged differently for each of the densities. The GSC24bc01, for instance, is internally organized as 16 pages of 8 bytes each and requires a 7-bit data word address. The GSC24BC16, on the other hand, is organized as 128 pages of 16 bytes each with an 11-bit data word address. The table below summarizes these differences.

Density	**# of pages**	**Bytes per page**	**Data word address length**
GSC24BC01 (1K)	**16 pages**	**8 bytes**	**7 bits**
GSC24BC02 (2K)	**32 pages**	**8 bytes**	**8 bits**
GSC24BC04 (4K)	**32 pages**	**16 bytes**	**9 bits**
GSC24BC08 (8K)	**64 pages**	**16 bytes**	**10 bits**
GSC24BC16 (16K)	**128 pages**	**16 bytes**	**11 bits**

PIN Capacitance

Applicable over recommended operating range from TA=25℃, f=1.0MHz, Vcc=+1.8V

Symbol	**Test Condition**	**Max**	**Unit**	**Condition**
CI/O	Input/Output Capacitance (SDA)	8	pF	VI/O=0V
CIN	Input Capacitance (A0, A1, A2, SCL)	6	pF	VIN=0V

Note: 1. This parameter is characterized and not 100% tested.

DC Characteristics

Applicable over recommended operating range from: TA=-40 ~ +85℃, VCC=+1.8 ~ +5V (unless otherwise noted)

Parameter	**Symbol**	**Test Condition**	**Min**	**TYP**	**Max**	**Unit**
Supply Voltage	VCC1		1.8	-	5.5	V
Supply Voltage	VCC2		2.7	-	5.5	V
Supply Voltage	VCC3		4.5	-	5.5	V
Supply Current VCC=5.0V	ICC	READ at 100KHz	-	0.4	1.0	mA
Supply Current VCC=5.0V	ICC	WRITE at 100KHz	-	2.0	3.0	mA
Standby Current VCC=1.8V	ISB1	VIN= VCC or VSS	-	0.6	3.0	μA
Standby Current VCC=2.5V	ISB2	VIN= VCC or VSS	-	1.4	4.0	μA
Standby Current VCC=5.5V	ISB3	VIN= VCC or VSS	-	5.0	18	μA
Input Leakage Current	ILI	VIN= VCC or VSS	-	0.2	5.0	μA
Output Leakage Current	ILO	VOUT= VCC or VSS	-	0.1	5.0	μA
Input Low Level (1)	VIL		-0.6	-	VCCx0.3	V
Input High Level (1)	VIH		VCCx0.7	-	VCC+0.5	V
Output Low Level VCC=3.0V	VOL2	IOL=2.1mA	-	-	0.4	V
Output Low Level VCC=3.0V	VOL1	IOL=0.15mA	-	-	0.2	V

Note 1: VIL and VIH max are reference only and are not tested.

AC Characteristics Applicable over recommended operating range from: T_A=-40 ~ +85℃, V_{CC}=+1.8 ~ 5.5V, C_L=1 TTL Gate & 100pF (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	TYP	Max	Unit
Clock Frequency, SCL	f_{SCL}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	-	-	100 400	KHz
Clock Pulse Width Low	t_{LOW}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.7 1.2	-	-	μs
Clock Pulse Width High	t_{HIGH}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.0 0.6	-	-	μs
Noise Suppression Time (1)	t_I	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	-	-	100 50	ns
Clock Low to Data Out Valid	t_{AA}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	0.1 0.1	-	4.5 0.9	μs
Time the bus must be free before a new transmission can start (1)	t_{BUF}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.7 1.2	-	-	μs
Start Hold Time	$t_{HD.STA}$	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.0 0.6	-	-	μs
Start Setup Time	$t_{SU.STA}$	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.7 0.6	-	-	μs
Data in Hold Time	$t_{HD.DAT}$	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	0 0	-	-	μs
Data in Setup Time	$t_{US.DAT}$	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	200 100	-	-	ns
Input Rise Time (1)	t_R	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	-	-	1.0 0.3	μs
Input Fall Time (1)	t_F	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	-	-	300 300	ns
Stop Setup Time	$t_{SU.STO}$	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	4.7 0.6	-	-	μs
Data Out Hold Time	t_{DH}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	100 50	-	-	ns
Write Cycle Time	t_{WR}	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	-	-	5 5	ms
5.0V, 25℃, Byte Mode	Endurance (1)	V_{CC}=1.8V V_{CC}=2.7 ~ 5.5V	1M 1M	-	-	Write Cycles

Note: 1. This parameter is characterized and not 100% tested.

Device Operation

Clock and Data Transitions: Transitions on the SDA pin should only occur when SCL is low (refer to the Data Validity timing diagram in Figure 5). If the SDA pin changes when SCL is high, then the transition will be interpreted as a START or STOP condition.

START Condition: A START condition occurs when the SDA transitions form high to low when SCL is high. The START signal is usually used to initiate a command (refer to the Start and Stop Definition timing diagram in Figure 6).

STOP Condition: A STOP condition occurs when the SDA transitions form low to high when SCL is high (refer to Figure 6. START and STOP Definition timing diagram). The STOP command will put the device into standby mode after no acknowledgment is issued during the read sequence.

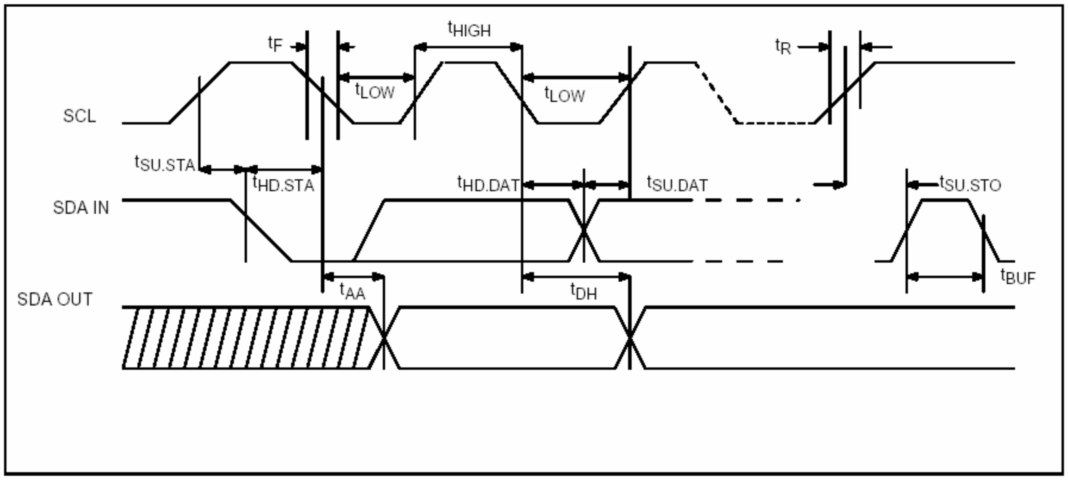
Acknowledge: An acknowledgement is sent by pulling the SDA low to confirm that a word has been successfully received. All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words, so acknowledgments are usually issued during the 9th clock cycle.

Standby Mode: Standby mode is entered when the chip is initially powered-on or after a STOP command has been issued and any internal operations have been completed. .

Memory Reset: In the event of unexpected power or connection loss, a START condition can be issued to restart the input command sequence. If the device is currently in write cycle mode, this command will be ignored.

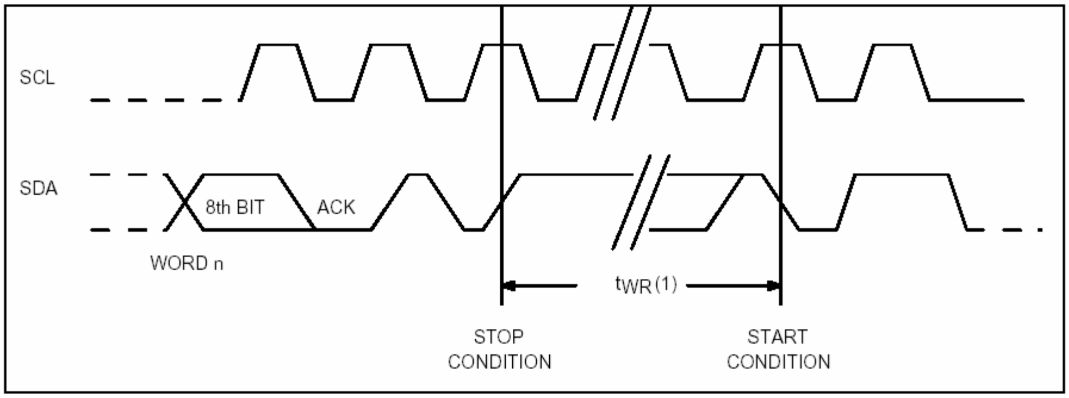
BUS TIMING

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O


t_{F}
t_{HIGH}
t_{R}
t_{LOW}
t_{LOW}
SCL
$t_{SU.STA}$
$t_{HD.STA}$
$t_{HD.DAT}$
$t_{SU.DAT}$
$t_{SU.STO}$
SDA IN
t_{AA}
t_{DH}
t_{BUF}
SDA OUT

WRITE CYCLE TIMING

Figure 4. SCL: Serial Clock, SDA: Serial Data I/O


SCL
SDA
8th BIT
ACK
WORD n
t_{WR} (1)
STOP CONDITION
START CONDITION

Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

Figure 5. DATA VALIDITY

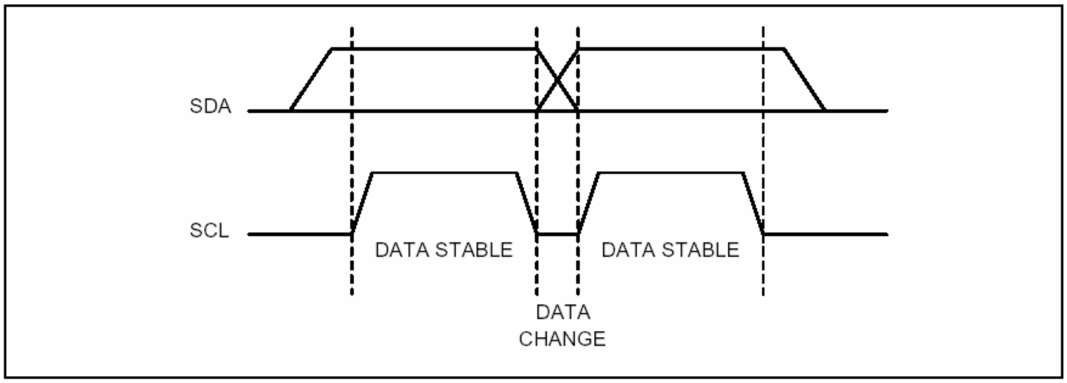

SDA
SCL
DATA STABLE
DATA STABLE
DATA CHANGE

Figure 6. START & STOP DEFINITION

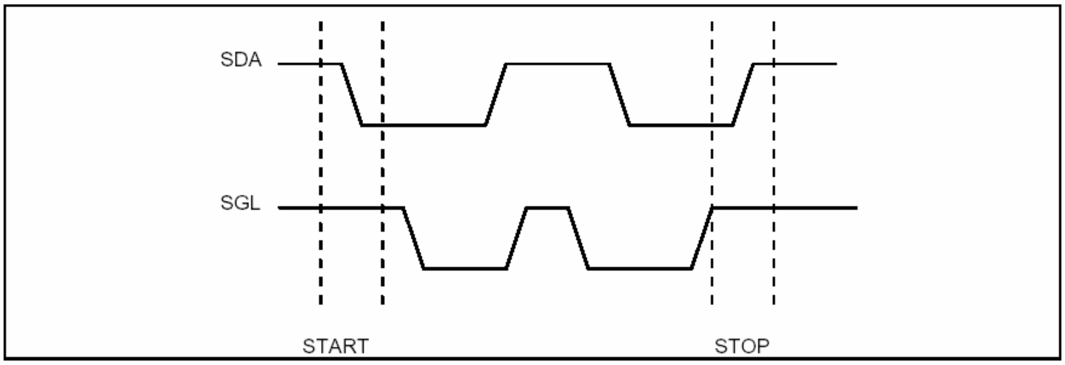
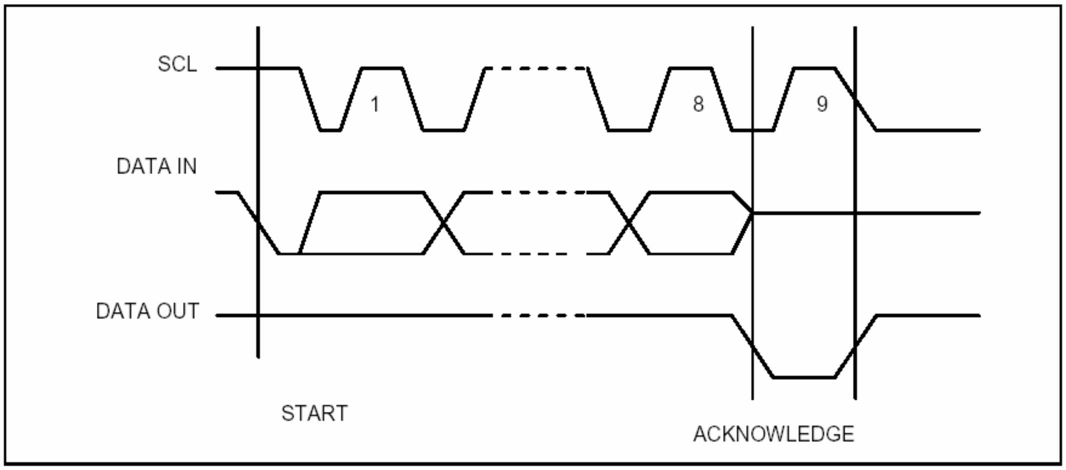


Figure 7. Output ACKNOWLEDGE



Device Addressing

To enable the chip for a read or write operation, an 8-bit device address word followed by a START condition must be issued. The 1st four bits of the device address word consists of a mandatory ‘1010’ pattern, while the 2nd four bits depend on the particular density being used (refer to Figure 8):

- In the 1K/2K chip, the next 3 bits should correspond to the hard-wired input A2, A1 and A0 device address bits.
- In the 4K chip, the next 3 bits are the A2 and A1 device address bits and a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins.
- In the 8K chip, the next 3 bits include the A2 device address bits with the next 2 bits used for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin.
- In the 16K chip does not use any device address bits but instead the 3 bits are used for memory page addressing.

Figure 8. Device Address

1K/2K	1	0	1	0	A_2	A_1	A_0	R/W
	MSB							LSB
4K	1	0	1	0	A_2	A_1	P0	R/W
8K	1	0	1	0	A_2	P1	P0	R/W
16K	1	0	1	0	P2	P1	P0	R/W

The memory page address bits, P2, P1 and P0 are used to select the page in the array. P2 represents the most significant bit, while P1 and P0 are considered the next most significant bits.

The eight bit of the device address determines read or write operation. If the R/W bit is high, then a read operation is initiated. Otherwise, if the R/W bit is low, then a write operation is started.

After comparing the device address and finding a match, the EEPROM device will issue an acknowledgment by pulling SDA low. If the comparison fails, the chip will return to standby mode.

Figure 9. Byte Write

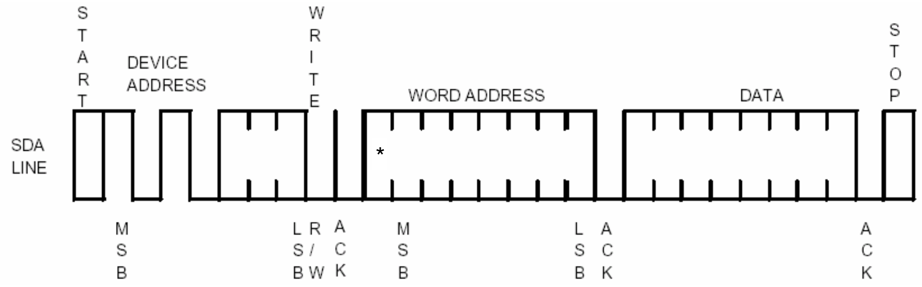
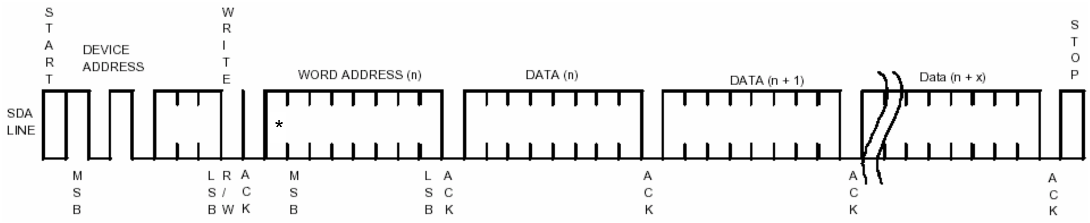


Figure 10. Page Write



(* = DON'T CARE bit for 1K)

Write Operations

Byte/Page Write:

If a write operation is entered ($R/\overline{W}=0$) and an acknowledgment is sent, then the next sequence requires an 8-bit data word address. After an acknowledgment is received from this word address, the 1st byte of data can be loaded. The device will send an acknowledgment after each byte to confirm the transmission.

To being the write cycle, a STOP condition must be issued (refer to Figure 9). Both byte and page write operations are supported, so the STOP condition can be issued after the 1st byte or the last byte in the page. When the STOP condition occurs, an internal time is started, all input are disabled, and the EEPROM will not respond to any more commands until the write cycle is completed.

Note: The number of bytes in a page depends on the density used. If 1K density is used, then the page size is 8 bytes. In contrast, if the 16K density is used, then the page size is 16 bites. Refer to the Memory Organization section for more details.

The internal page counter is incremented after each byte received, but the row location of the memory page will always remain the same. Therefore, the device will wrap around to the 1st byte in the page after the last byte in the page is received. Any further data loaded into the page buffer will overwrite the previous data loaded.

Acknowledge Polling: After the STOP condition is issued, the write cycle begins. Acknowledge polling can be initiated by sending a START condition followed by the device address word. If the EEPROM has completed the internal write cycle and returned to standby mode, the device will respond by sending back an acknowledgment by pulling the SDA pin low. Otherwise, the sequence will be ignored and no acknowledgment will be sent.

Read Operations

There are three types of read operations: current address read, random address read, and sequence read. A random address read can be considered a current address read operation with an additional sequence in the beginning to load a different address into the internal counter. A sequential read occurs when subsequent bytes are clocked out after a current address read or random address read occurs.

Current Address Read: A current address read operation is initiated by issuing R/W=1 in the device address word (refer to Figure 11). Since the internal address counter maintains the last address incremented by one accessed during the last read or write operation, the internal address counter will always retain the last address incremented by one.

Random Read: To access a different address location that the one currently stored in the internal counter, a random read operation is provided. The random read is actually a combination of a “dummy” byte write sequence with a current address read command (refer to Figure 12). The “dummy” byte write loads a different address into the internal counter, and the data can then be accessed using the current address read.

Sequential Read: In order to access subsequent data word after a current address read or random read has been initiated, the user should send an acknowledgment to the EEPROM chip after each data byte received. If an acknowledgment is not received, then the chip will not send any more data and expect a STOP condition on the next cycle to reset back to standby more (refer to Figure 13).

Sequential reads can be used to perform an entire chip read. Unlike the page write operation, the internal counter will increment to the next row after the last byte of the page has been reached. When the address reaches the last byte of the last memory page, the next address will increment to the 1st byte of the 1st memory page.

Once the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. When the microcontroller does not respond with a zero but does generate a following stop condition, the sequential read operations is terminated.

Figure 11. Current Address Read

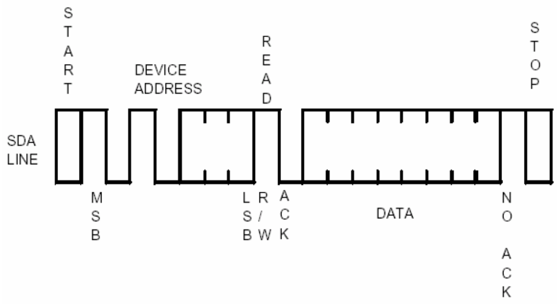
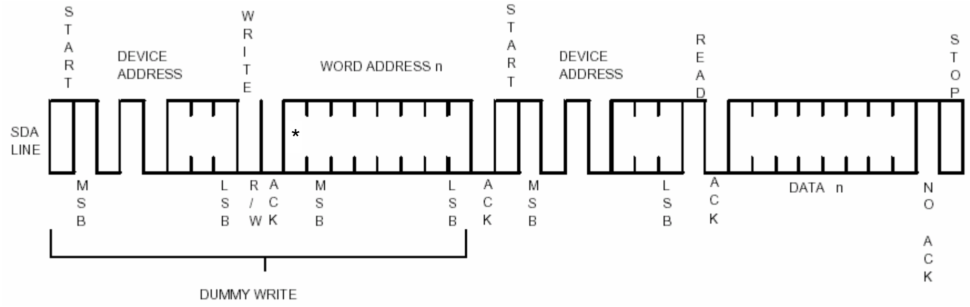
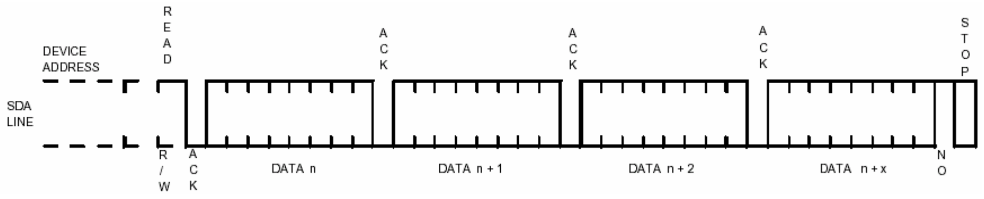

START
DEVICE ADDRESS
READ
STOP
SDA LINE
MSB
LSB
R/W
ACK
DATA
NO ACK

Figure 12. Random Read


START
DEVICE ADDRESS
WRITE
WORD ADDRESS n
START
DEVICE ADDRESS
READ
STOP
SDA LINE
*
MSB
LSB
R/W
ACK
MSB
LSB
ACK
MSB
LSB
ACK
DATA n
NO ACK
DUMMY WRITE

(* = DON’T CARE bit for 1K)

Figure 13. Sequential Read


DEVICE ADDRESS
READ
ACK
ACK
ACK
STOP
SDA LINE
R/W
ACK
DATA n
DATA n + 1
DATA n + 2
DATA n + x
NO

GSC24BC Ordering Information

Ordering Code	Package	Operating Ranges
GSC24BC01I	**SOP-8**	**Industrial (-40 ~ +85℃)**
GSC24BC02I		
GSC24BC04I		
GSC24BC08I		
GSC24BC16I		

Product Ordering Information

GSC24BCXXY

G=GTM

SC=SOP-8

24=Device Type

Supply Voltage
BC=1.8V to 5.5V

Device Function
01= 1 Kbit (128x8)
02= 2 Kbit (256x8)
04= 4 Kbit (512x8)
08= 8 Kbit (1024x8)
16=16 Kbit (2048x8)

Temperature
I=Industrial (-40 ~ +85℃)

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