# R8A66160DD/SP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

REJ03F0261-0100
Rev. 1.00
Jan.10. 2008

## DESCRIPTION

R8A66160 is a LED array driver having a 16-bit serial input and parallel output shift register function with direct coupled reset input and output latch function.
This product guarantees the output current of 24mA (Vcc =5V case) which is sufficient for cathode common LED drive, capable of following 16-bits continuously at the same time. Parallel output is open drain output.
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products. Furthermore, pin layout ensures the realization of an easy printed circuit. R8A66160 is the succession product of M66310.

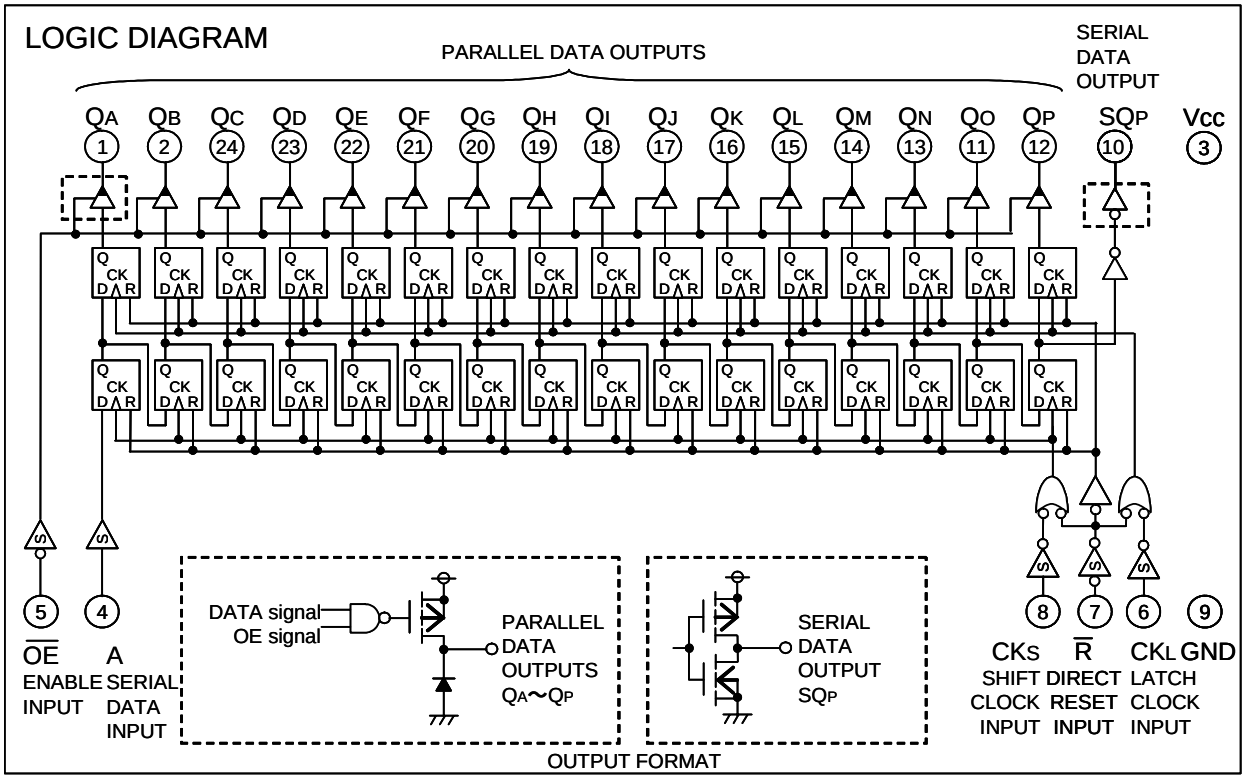
## FEATURES

- Cathode common LED drive
- $V_{CC}$ 5V or 3.3V single power supply
- High output current: all parallel outputs $Q_A$~$Q_P$ $I_{OH}$=-24mA (at $V_{CC}$ =5.0V) $I_{OH}$=-12mA (at $V_{CC}$ =3.3V) simultaneous lighting available
- Low power dissipation: 100uW/package (max) (Vcc=5.0V, Ta=25°C, quiescent state)
- High noise margin: Schmitt input circuit provides responsiveness to a long line length
- Equipped with direct-coupled reset
- Open drain output: (except serial data output $SQ_P$)
- Wide operating temperature range: Ta=-40°C~+85°C
- Pin layout facilitates printed circuit wiring. (This layout facilitates cascade connection and LED connection)

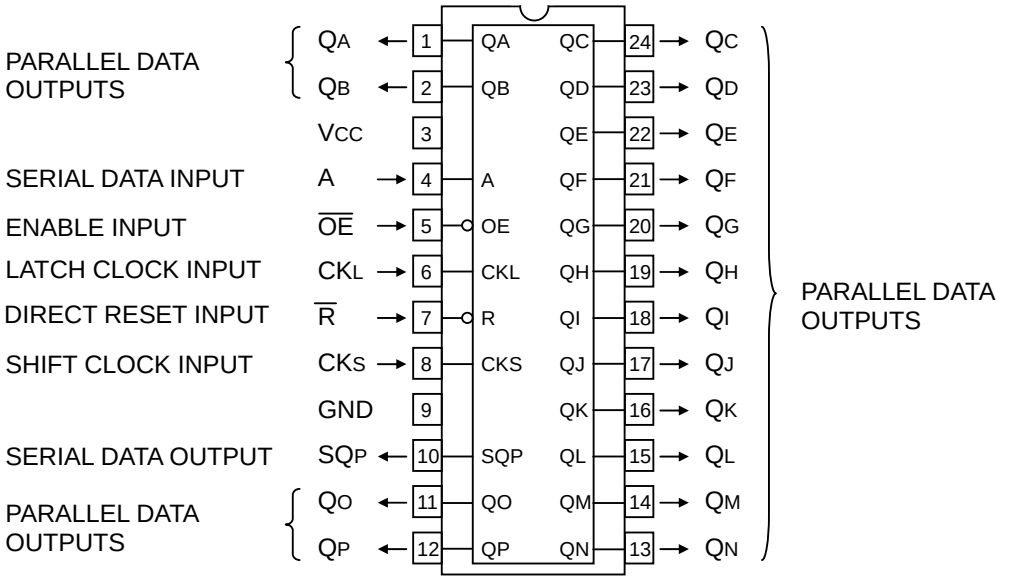
## APPLICATION

- LED array drive, The various LED display modules
- PPC, Printer, VCR, Mini-compo, Button-Telephone etc.  All of LED display equipment

## BLOCK DIAGRAM



## PIN CONFIGURATION ( TOP VIEW )




## FUNCTIONAL DESCRIPTION

As R8A66160 uses silicon gate CMOS process. It realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.
Each bit of a shift register consists of two flip-flop having independent clocks for shifting and latching.
As for clock input, shift clock input $CK_S$ and latch clock input $CK_L$ are independent from each other, shift and latch operations being made when “L” changes to “H”.
Serial data input A is the data input of the first-step shift register and the signal of A shifts shifting registers one by one when a pulse is impressed to $CK_S$. When A is “L”, the signal of “L” shifts.
When the pulse is impressed to $CK_L$, the contents of the shifting register at that time are stored in a latching register, and they appear in the parallel data outputs from $Q_A$ ~ $Q_P$.
Outputs $Q_A$ ~ $Q_P$ are open drain outputs.
To extend the number of bits, use the serial data output $SQ_P$ which shows the output of the shifting register of the 16th bit.
When reset input $\overline{R}$ is changed to “L”, $Q_A$ ~ $Q_P$ and $SQ_P$ are reset. In this case, shifting and latching register are reset.
If “H” is impressed to output enable input $\overline{OE}$, $Q_A$ ~ $Q_P$ reaches the high impedance state, but $SQ_P$ does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

## FUNCTION TABLE (Note: 1)

| Operation mode | | Input | | | | | Parallel data output | | | | | | | | | | | | | | | | Serial data output SQP | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $\overline{R}$ | $CK_S$ | $CK_L$ | A | $\overline{OE}$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ | $Q_H$ | $Q_I$ | $Q_J$ | $Q_K$ | $Q_L$ | $Q_M$ | $Q_N$ | $Q_O$ | $Q_P$ | | |
| Reset | | L | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | L | — |
| Shift Latch operation | Shift $t_1$ | H | ↑ | X | H | L | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ | $Q_E^0$ | $Q_F^0$ | $Q_G^0$ | $Q_H^0$ | $Q_I^0$ | $Q_J^0$ | $Q_K^0$ | $Q_L^0$ | $Q_M^0$ | $Q_N^0$ | $Q_O^0$ | $Q_P^0$ | $q_O^0$ | Output lighting “H” |
| | Latch $t_2$ | H | X | ↑ | X | L | H | $q_A^0$ | $q_B^0$ | $q_C^0$ | $q_D^0$ | $q_E^0$ | $q_F^0$ | $q_G^0$ | $q_H^0$ | $q_I^0$ | $q_J^0$ | $q_K^0$ | $q_L^0$ | $q_M^0$ | $q_N^0$ | $q_O^0$ | $q_O^0$ | |
| | Shift $t_1$ | H | ↑ | X | L | L | $Q_A^0$ | $Q_B^0$ | $Q_C^0$ | $Q_D^0$ | $Q_E^0$ | $Q_F^0$ | $Q_G^0$ | $Q_H^0$ | $Q_I^0$ | $Q_J^0$ | $Q_K^0$ | $Q_L^0$ | $Q_M^0$ | $Q_N^0$ | $Q_O^0$ | $Q_P^0$ | $q_O^0$ | Output lights-out “L” |
| | Latch $t_2$ | H | X | ↑ | X | L | Z | $q_A^0$ | $q_B^0$ | $q_C^0$ | $q_D^0$ | $q_E^0$ | $q_F^0$ | $q_G^0$ | $q_H^0$ | $q_I^0$ | $q_J^0$ | $q_K^0$ | $q_L^0$ | $q_M^0$ | $q_N^0$ | $q_O^0$ | $q_O^0$ | |
| Output disable | | X | X | X | X | H | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | $q_P$ | — |

Note1: ↑ : Change from low-level to high-level
$Q^0$ : Output state Q before $CK_L$ changed
X : Irrelevant
$q^0$ : Contents of shift register before $CK_S$ changed
q : Contents of shift register
$t_1$, $t_2$ : $t_2$ is set after $t_1$ is set
Z : High Impedance

## ABSOLUTE MAXIMUM RATINGS (Ta=-40~+85°C, unless otherwise noted)

| Symbol | Parameter | | Conditions | Ratings | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | -0.5 ~ +7.0 | V |
| $V_I$ | Input voltage | | | -0.5 ~ $V_{CC}$+0.5 | V |
| $V_O$ | Output voltage | | | -0.5 ~ $V_{CC}$+0.5 | V |
| $I_O$ | Output current per output pin | $Q_A$ ~ $Q_P$ | | -50 | mA |
| | | $SQ_P$ | | ±25 | |
| $I_{CC}$ | Supply / GND current | | $V_{CC}$, GND | -410, +20 | mA |
| $P_d$ | Power dissipation | | (Note 2) | 500 | mW |
| $T_{stg}$ | Storage temperature range | | | -65 ~+150 | °C |

Note 2: R8A66160SP; Ta=-40~+70°C, Ta=+70~+85°C are derated at -6mW/°C.

## RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | 5.0V support | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V support | 3.0 | 3.3 | 3.6 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $T_{opr}$ | Operating temperature range | | -40 | | +85 | °C |

# ELECTRICAL CHARACTERISTICS

## ■5.0V version support specifications (Ta=-40~+85°C,Vcc=4.5V~5.5V, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| VT+ | Positive-going threshold voltage | | VO=0.1V, VCC-0.1V<br>\|IO\|=20uA | | 0.35xVCC | | 0.70xVCC | V |
| VT- | Negative-going threshold voltage | | VO=0.1V, VCC-0.1V<br>\|IO\|=20uA | | 0.20xVCC | | 0.55xVCC | V |
| VOH | High-level output voltage | QA ~ QP | VI=VT+,VT-<br>VCC=4.5V<br>(Note3) | IOH= -20uA | VCC-0.1 | | | V |
| | | | | IOH= -24mA | 3.66 | | | |
| | | | | IOH= -40mA | 3.25 | | | |
| VOH | High-level output voltage | SQP | VI=VT+,VT-<br>VCC=4.5V | IOH= -20uA | VCC-0.1 | | | V |
| | | | | IOH= -4mA | 3.66 | | | |
| VOL | Low-level output voltage | SQP | VI=VT+,VT-<br>VCC=4.5V | IOL= 20uA | | | 0.10 | V |
| | | | | IOL= 4mA | | | 0.53 | |
| IIH | High-level input current | | VI=VCC, VCC=5.5V | | | | 5 | uA |
| IIL | Low-level input current | | VI=GND, VCC=5.5V | | | | -5 | uA |
| IO | Maximum output leakage current | QA ~ QP | VI=VT+,VT-<br>VCC=5.5V | VO=VCC | | | 10 | uA |
| | | | | VO=GND | | | -10 | |
| ICC | Quiescent supply current | | VI=VCC,GND, VCC=5.5V | | | | 200 | uA |

Note 3: R8A66160 is used under the condition of an output current IOH=-40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle – IOH of TYPICAL CHARACTERISTICS.

## ■3.3V version support specifications (Ta=-40~+85°C,Vcc=3.0V~3.6V, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| VT+ | Positive-going threshold voltage | | VO=0.1V, VCC-0.1V<br>\|IO\|=20uA | | 0.35xVCC | | 0.70xVCC | V |
| VT- | Negative-going threshold voltage | | VO=0.1V, VCC-0.1V<br>\|IO\|=20uA | | 0.20xVCC | | 0.55xVCC | V |
| VOH | High-level output voltage | QA ~ QP | VI=VT+,VT-<br>VCC=3.0V | IOH= -20uA | VCC-0.1 | | | V |
| | | | | IOH= -12mA | 2.34 | | | |
| | | | | IOH= -20mA | 2.08 | | | |
| VOH | High-level output voltage | SQP | VI=VT+,VT-<br>VCC=3.0V | IOH= -20uA | VCC-0.1 | | | V |
| | | | | IOH= -2mA | 2.60 | | | |
| VOL | Low-level output voltage | SQP | VI=VT+,VT-<br>VCC=3.0V | IOL= 20uA | | | 0.10 | V |
| | | | | IOL= 2mA | | | 0.40 | |
| IIH | High-level input current | | VI=VCC, VCC=3.6V | | | | 5 | uA |
| IIL | Low-level input current | | VI=GND, VCC=3.6V | | | | -5 | uA |
| IO | Maximum output leakage current | QA ~ QP | VI=VT+,VT-<br>VCC=3.6V | VO=VCC | | | 10 | uA |
| | | | | VO=GND | | | -10 | |
| ICC | Quiescent supply current | | VI=VCC,GND, VCC=3.6V | | | | 200 | uA |

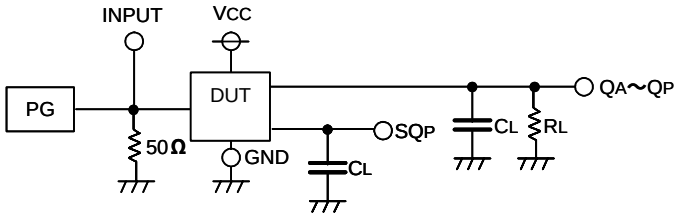
## SWITCHING CHARACTERISTICS (Ta=-40~+85°C,Vcc=5.0V or 3.3V)

| Symbol | Parameter | | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| fmax | Maximum clock frequency | | CL=50pF RL=1KΩ (Note 4) | | | 4 | | | 3.3 | MHz |
| tPLH | Output "L"-"H" and "H"-"L" propagation time | CKS - SQP | | | | 125 | | | 150 | ns |
| tPHL | | | | | | 125 | | | 150 | ns |
| tPHL | Output "H"-"L" propagation time | $\overline{R}$ - SQP | | | | 125 | | | 150 | ns |
| tPHZ | Output "H"-"Z" propagation time | $\overline{R}$ - QA ~ QP (turned off) | | | | 200 | | | 220 | ns |
| tPZH | Output "Z"-"H" propagation time | CKL - QA ~ QP (turned on) | | | | 125 | | | 150 | ns |
| tPHZ | Output "H"-"Z" propagation time | CKL - QA ~ QP (turned off) | | | | 200 | | | 220 | ns |
| tPZH | Output "Z"-"H" propagation time | $\overline{OE}$ - QA ~ QP (turned on) | | | | 125 | | | 150 | ns |
| tPHZ | Output "H"-"Z" propagation time | $\overline{OE}$ - QA ~ QP (turned off) | | | | 200 | | | 220 | ns |
| CI | Input capacitance | | | | | 10 | | | 10 | pF |

## TIMING REQUIREMENTS (Ta=-40~+85°C,Vcc=5.0V or 3.3V)

| Symbol | Parameter | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| tw | CKS, CKL, $\overline{R}$ pulse width | (Note 4) | 125 | | | 150 | | | ns |
| tsu | A setup time with respect to CKS | | 125 | | | 150 | | | ns |
| tsu | CKS setup time with respect to CKL | | 125 | | | 150 | | | ns |
| th | A hold time with respect to CKS | | 15 | | | 20 | | | ns |
| trec | $\overline{R}$ recovery time with respect to CKS, CKL | | 70 | | | 80 | | | ns |

Note4 : Test Circuit

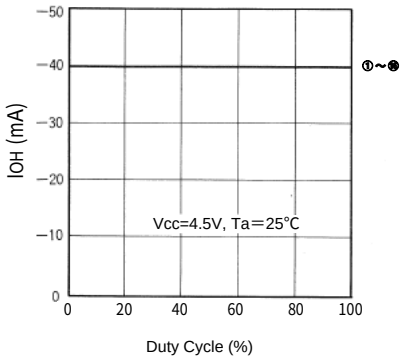



(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr=6ns,tf=6ns
(2) The capacitance CL includes stray wiring capacitance and the probe input capacitance.

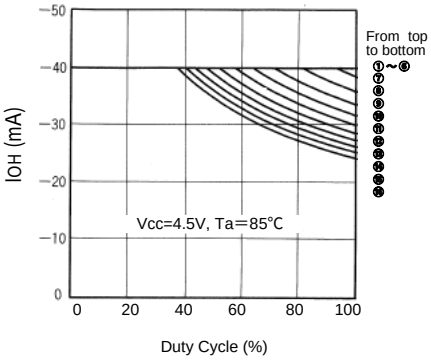
## TYPICAL CHARACTERISTICS

- Repetition frequency > 10Hz
- Numbers in ◯ indicate the number of output circuits that operate simultaneously.
- Current values are per circuit.

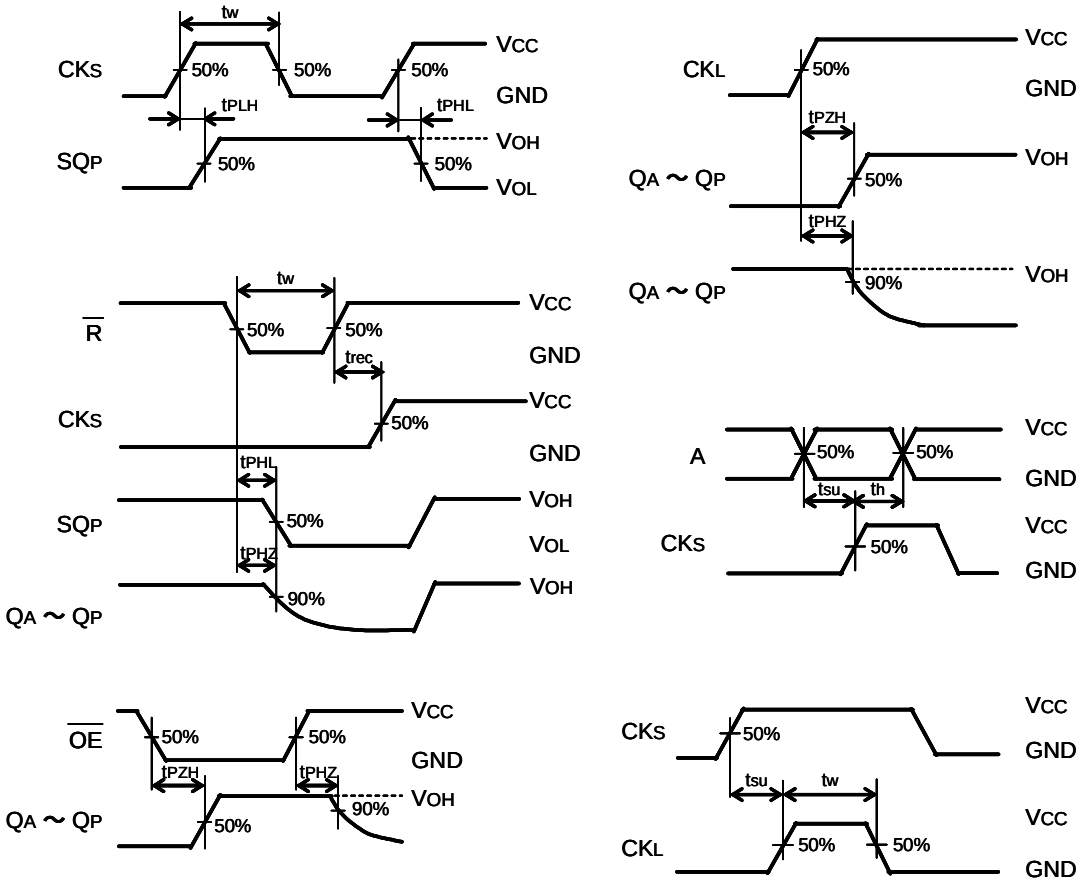
Duty Cycle-IOH Characteristics




Duty Cycle-IOH Characteristics

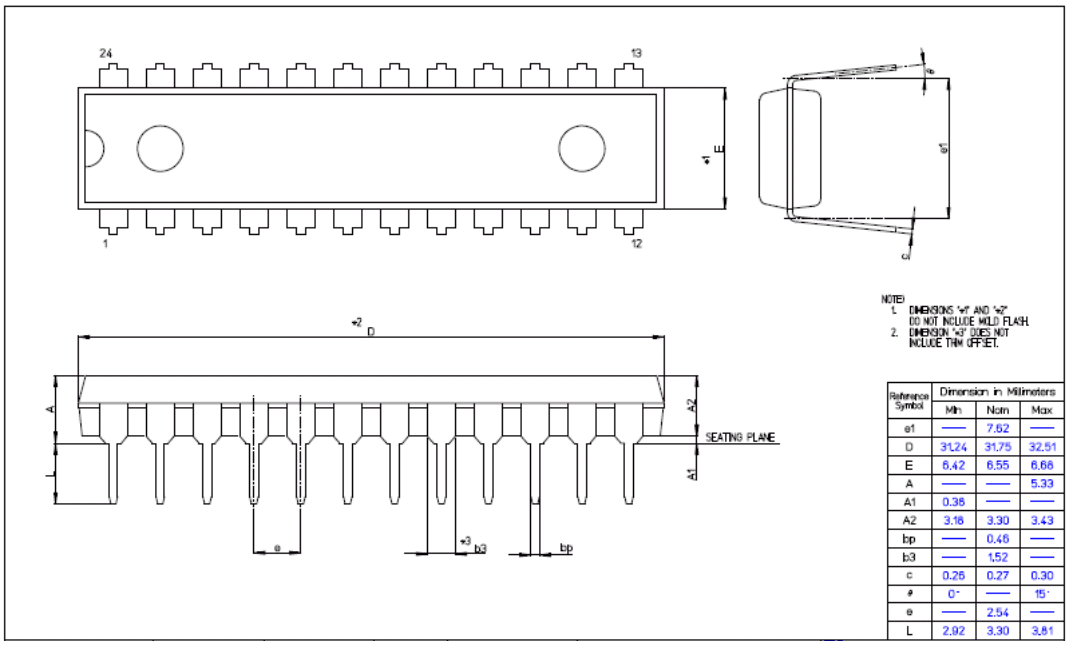



## TIMING DIAGRAM

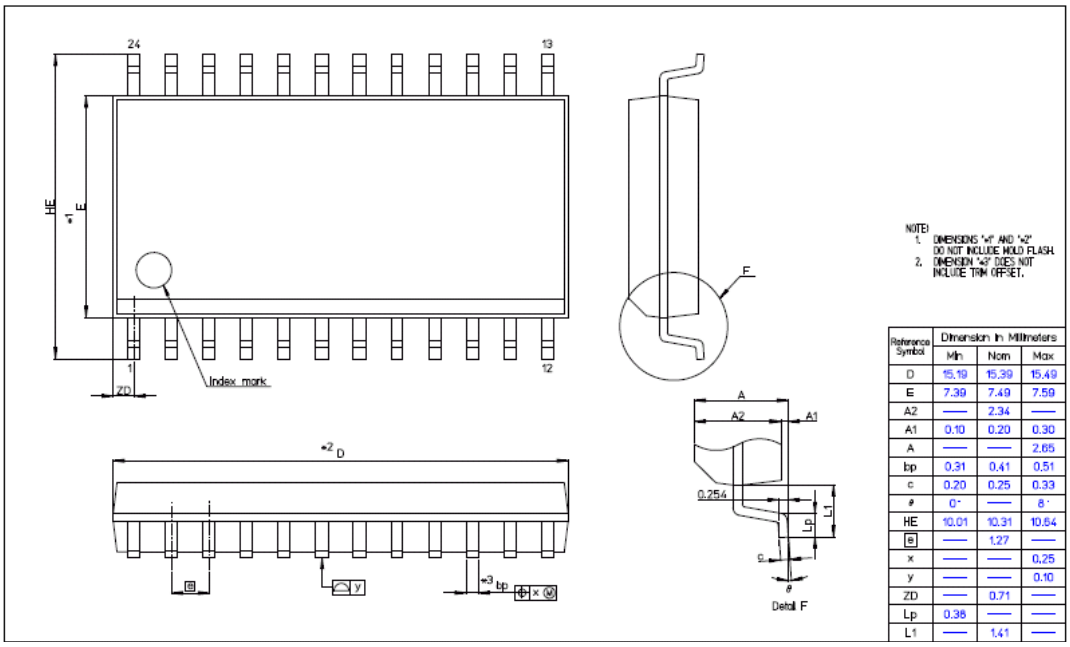


# PACKAGE OUTLINE

| Product name | Package | RENESAS Code | Previous Code |
|---|---|---|---|
| R8A66160DD | 24pin DIP | PRDP0024AF-A | 24P4X-A |
| R8A66160SP | 24pin SOP | PRSP0024DF-A | 24P2X-B |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e1 | — | 7.62 | — |
| D | 31.24 | 31.75 | 32.51 |
| E | 6.42 | 6.55 | 6.68 |
| A | — | — | 5.33 |
| A1 | 0.38 | — | — |
| A2 | 3.18 | 3.30 | 3.43 |
| bp | — | 0.46 | — |
| b3 | — | 1.52 | — |
| c | 0.26 | 0.27 | 0.30 |
| θ | 0° | — | 15° |
| e | — | 2.54 | — |
| L | 2.92 | 3.30 | 3.81 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 15.19 | 15.39 | 15.49 |
| E | 7.39 | 7.49 | 7.59 |
| A2 | — | 2.34 | — |
| A1 | 0.10 | 0.20 | 0.30 |
| A | — | — | 2.65 |
| bp | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.33 |
| θ | 0° | — | 8° |
| HE | 10.01 | 10.31 | 10.64 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.10 |
| ZD | — | 0.71 | — |
| Lp | 0.38 | — | — |
| L1 | — | 1.41 | — |

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan



## RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

**Renesas Technology America, Inc.**
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

**Renesas Technology Hong Kong Ltd.**
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

**Renesas Technology Taiwan Co., Ltd.**
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

**Renesas Technology Singapore Pte. Ltd.**
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510



Colophon .7.2