4MX9 CMOS DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM594000A- 7	70ns	20ns	130ns
KMM594000A- 8	80ns	20ns	150ns
KMM594000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

The Samsung KMM594000A is a 4M bit × 9 Dynamic RAM high density memory module. The Samsung KMM594000A consist of nine KM41C4000AJ DRAMs in 20-pin SOJ package mounted on a 30-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each 4M Bit DRAM.

The KMM594000A is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

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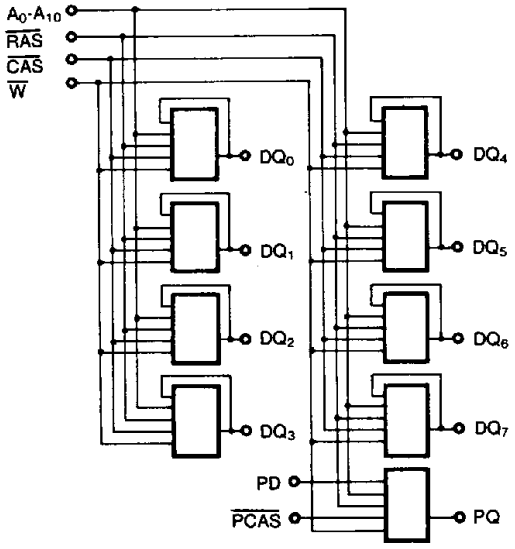
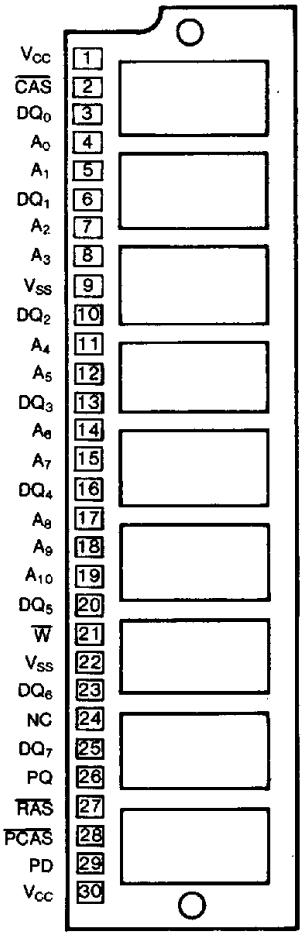
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{0-7}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	CAS for Parity
PD	Data In for Parity
PQ	Data Out for Parity
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	5.4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM594000A- 7	I_{CC1}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	18	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM594000A- 7	I_{CC3}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM594000A- 7	I_{CC4}	—	720	mA
	KMM594000A- 8		—	630	mA
	KMM594000A-10		—	540	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	9	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM594000A- 7	I_{CC6}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−90	90	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	55	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	65	pF
Input Capacitance (PD, $\overline{PCAS}$)	C_{IN3}	—	10	pF
Input/Output Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF
Output Capacitance (PQ)	C_Q	—	10	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM594000A-7		KMM594000A-8		KMM594000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

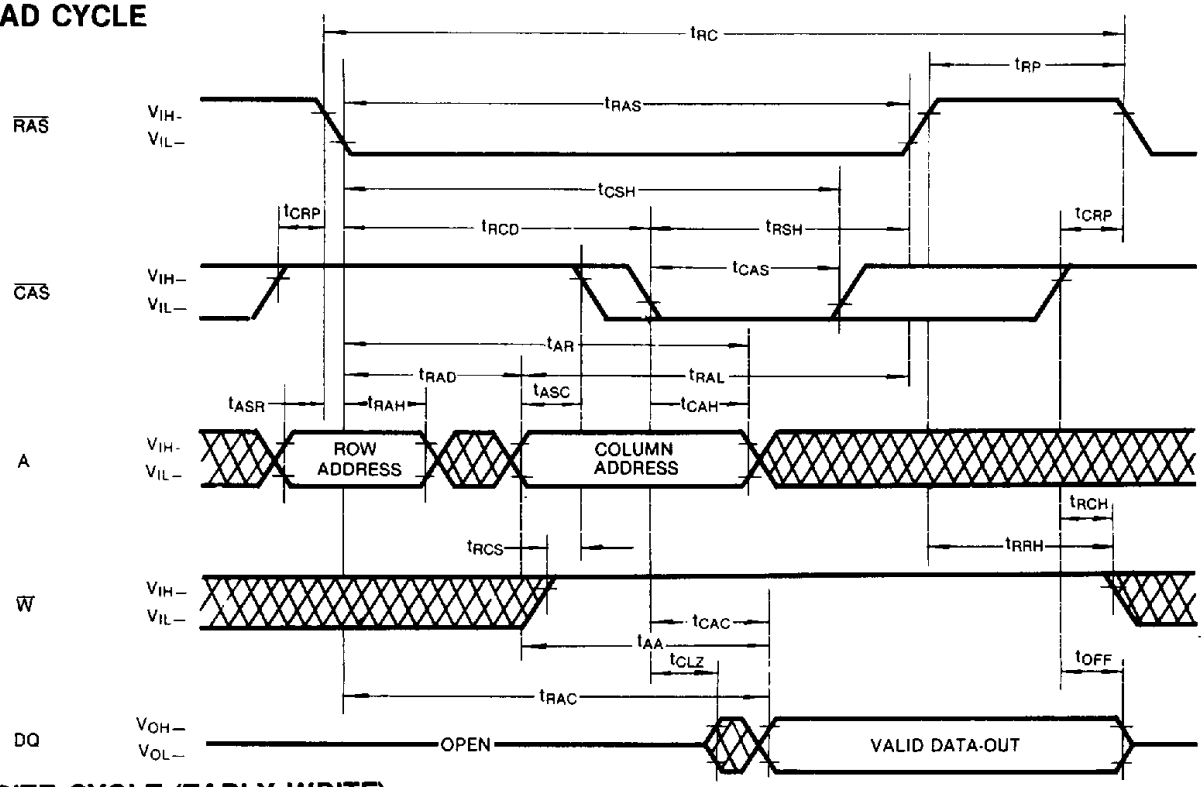
Standard Operation	Symbol	KMM594000A-7		KMM594000A-8		KMM594000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ setup time (C-B-R refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	

NOTES

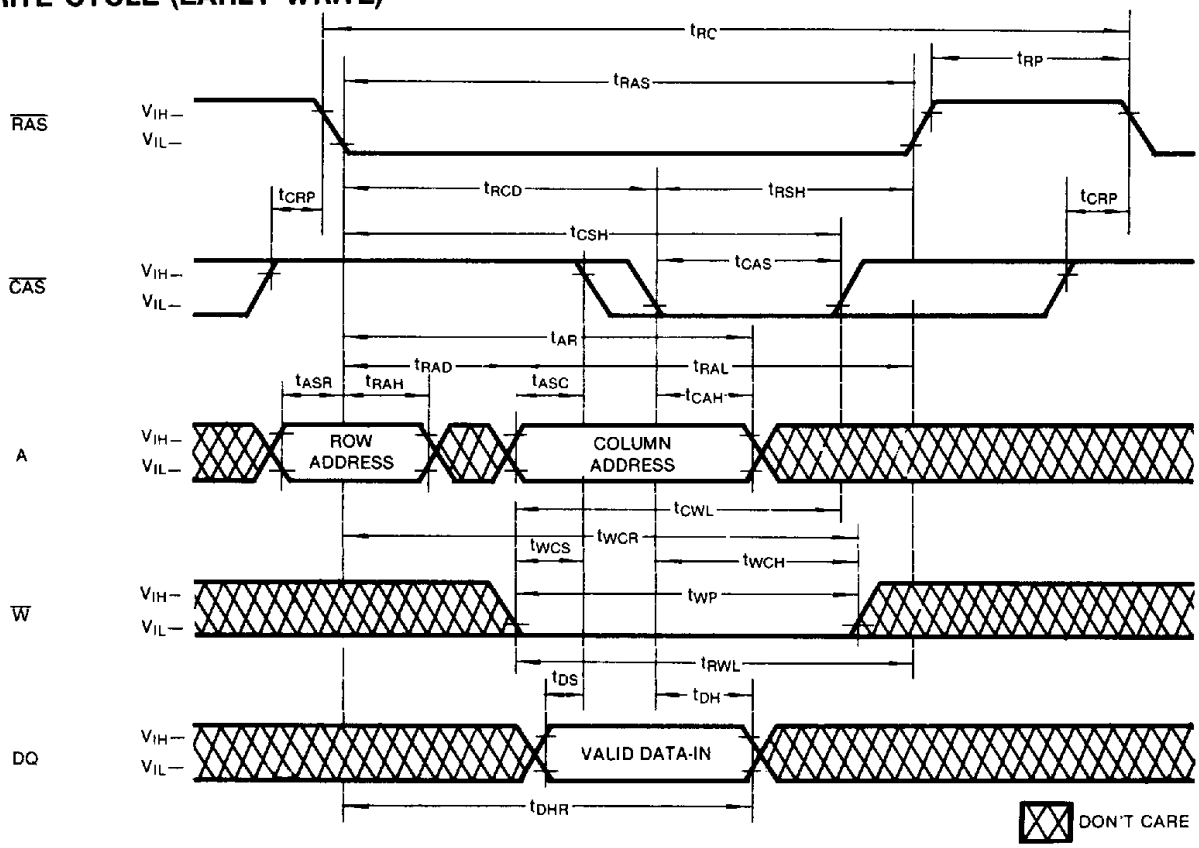
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

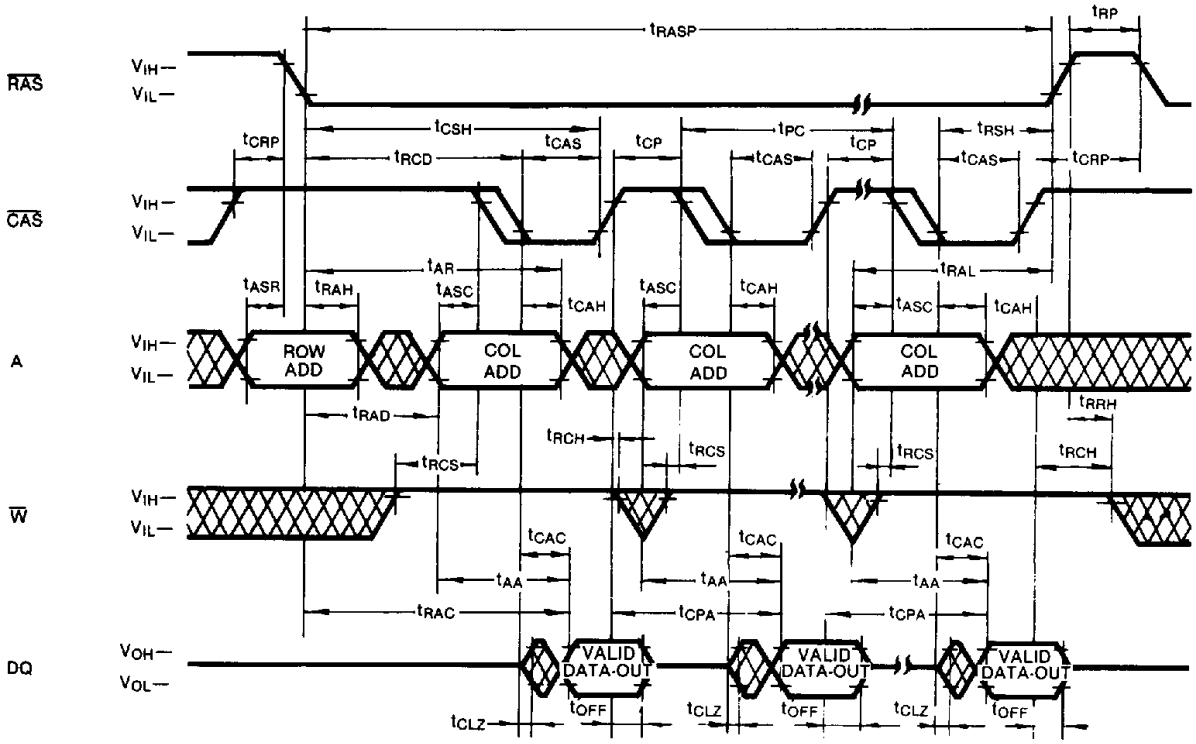


WRITE CYCLE (EARLY WRITE)

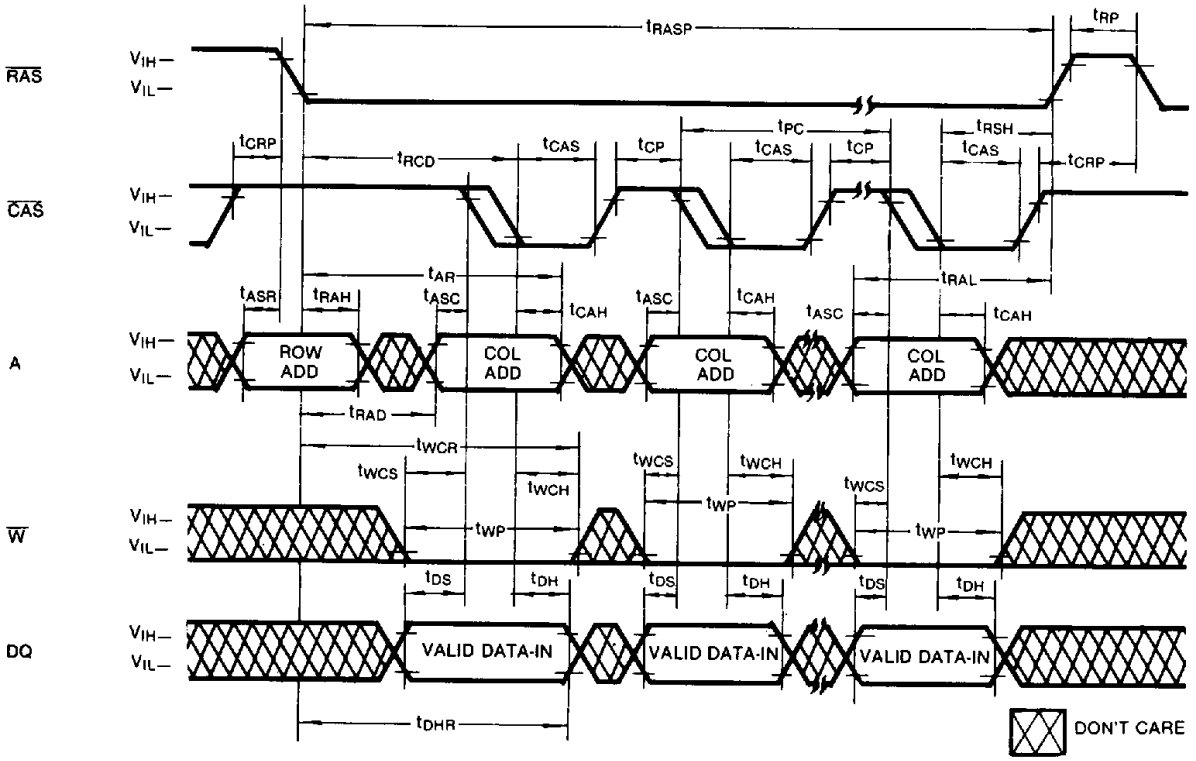


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



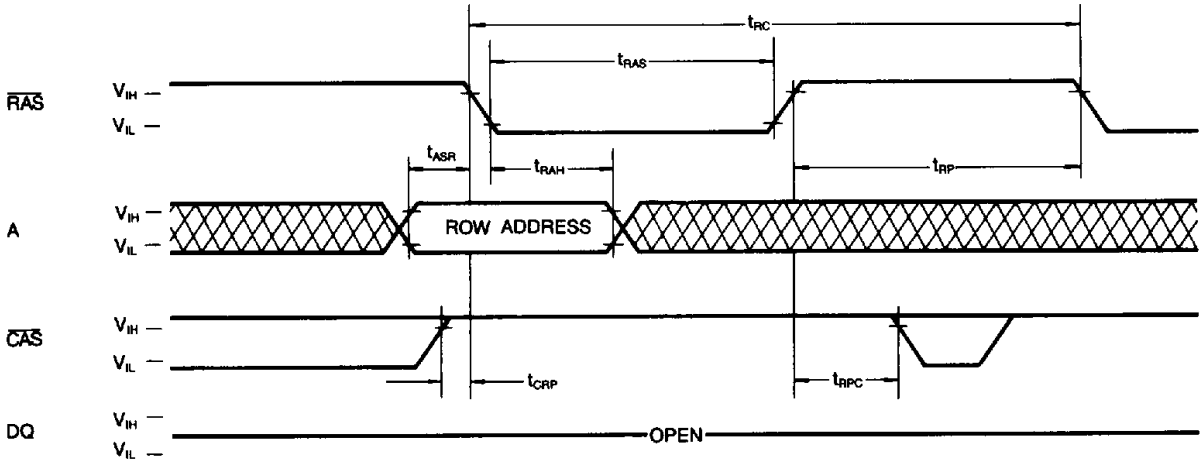
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

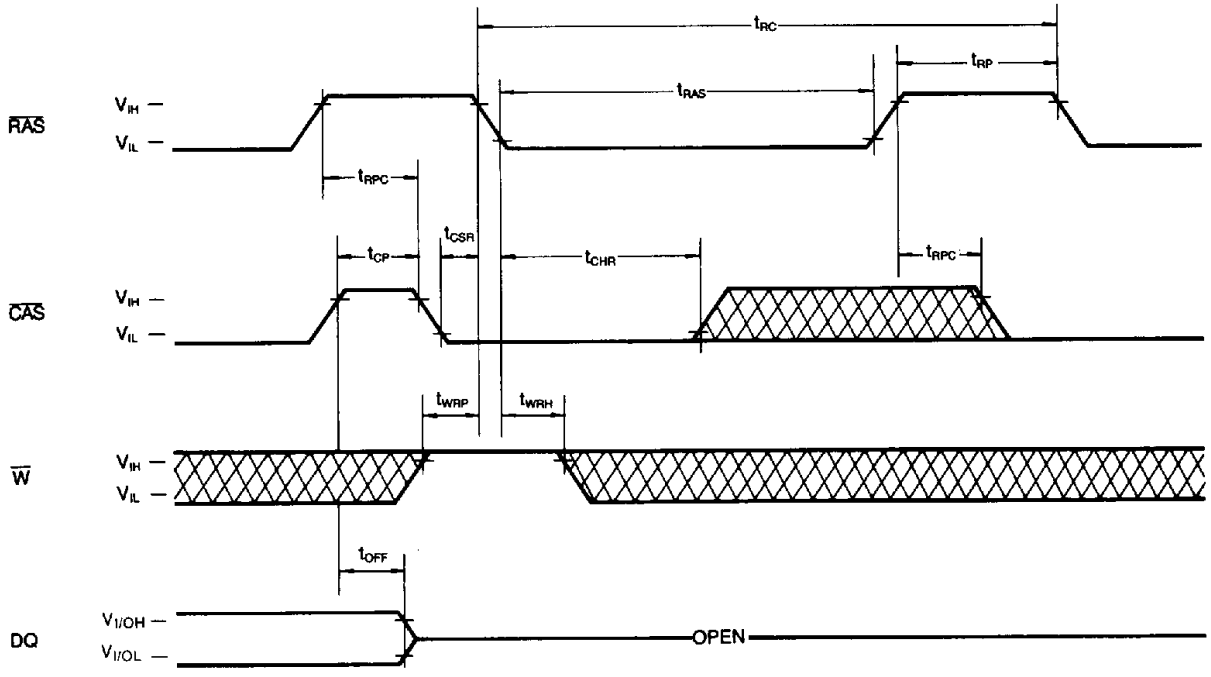
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



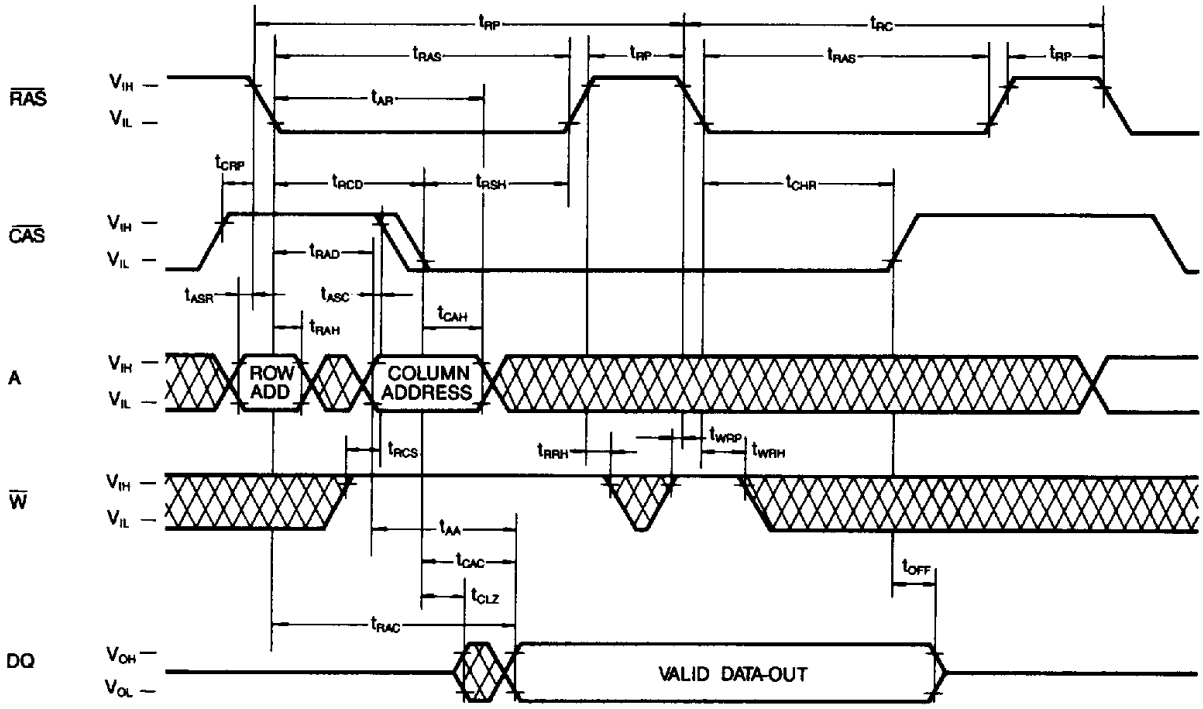
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

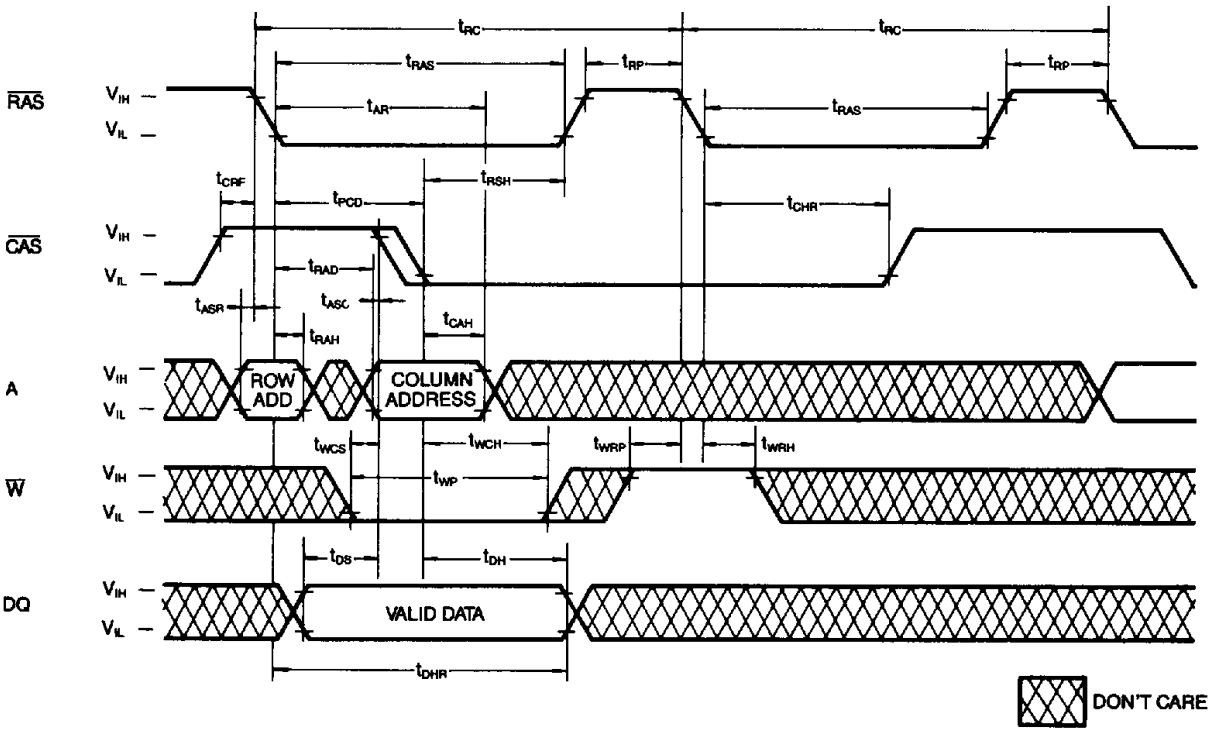


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

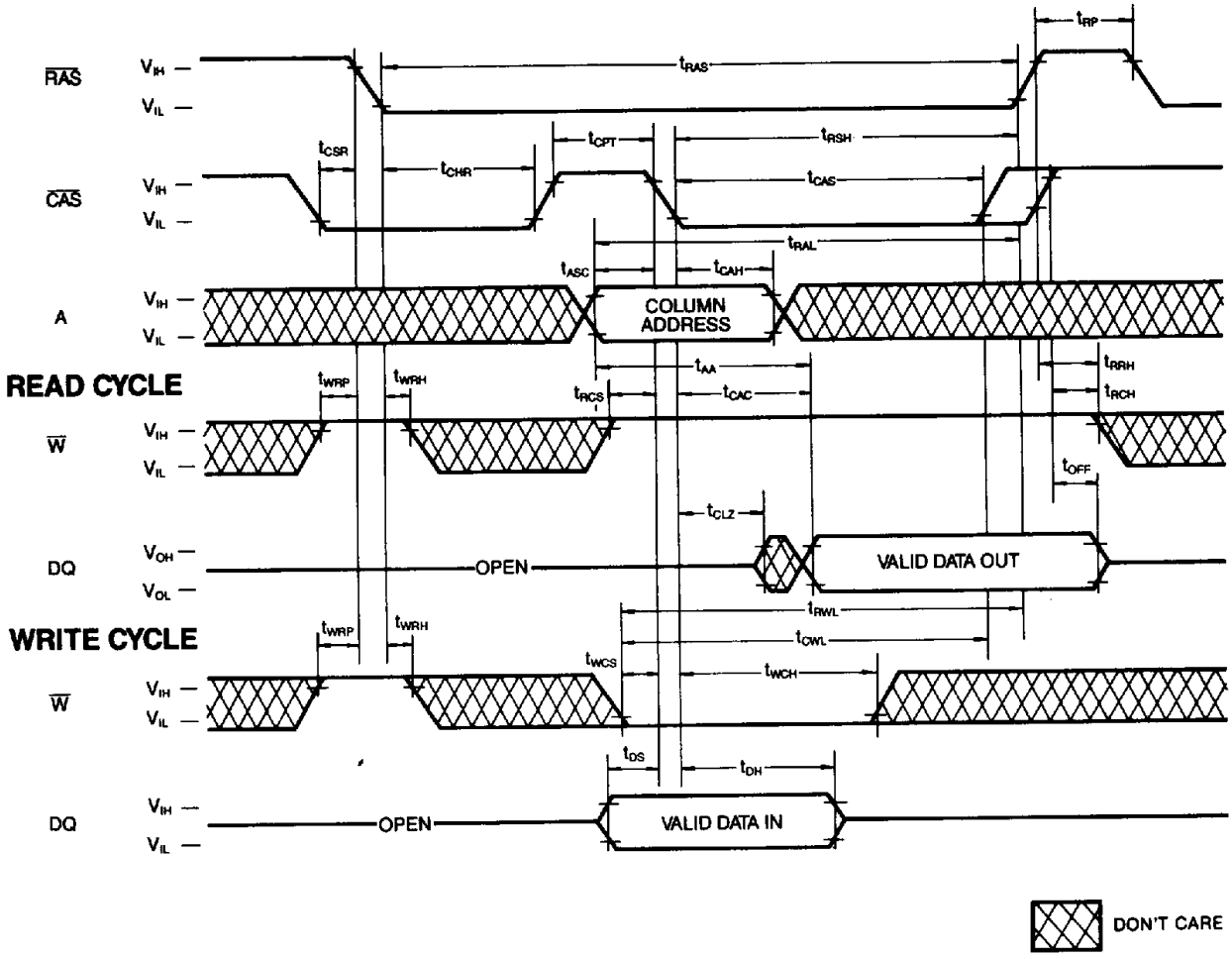


HIDDEN REFRESH CYCLE (WRITE)



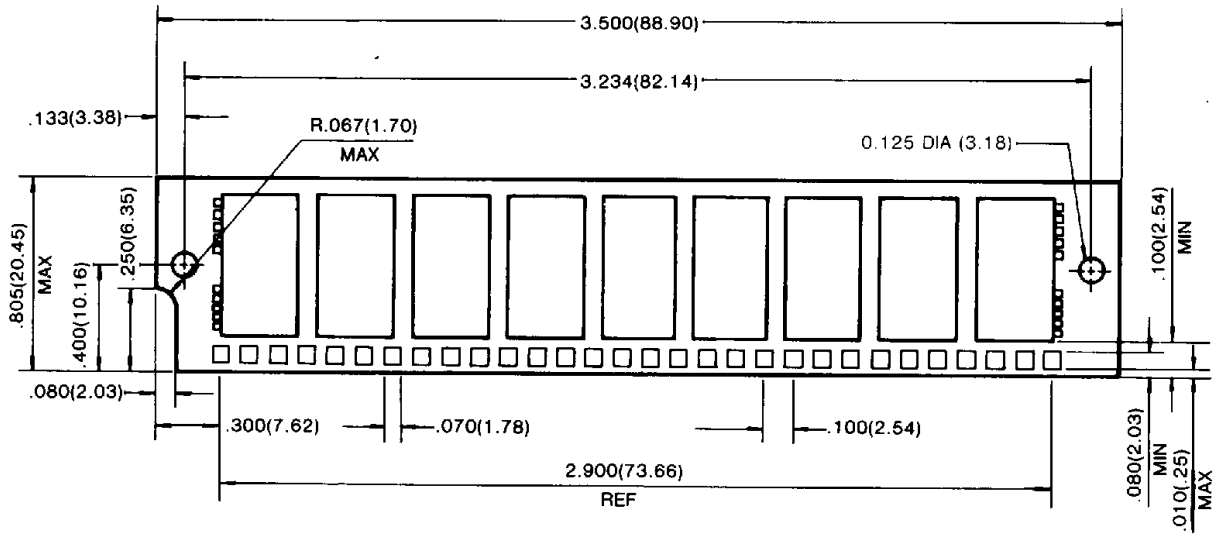
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSIONS

Units: Inches (millimeters)



Tolerances: ±.005(.13) unless otherwise specified