

2Mx36 DRAM SIMM

(1MX16 Base, Quad CAS EDO)

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Revision 0.0

November 1997

Revision History

Version 0.0 (November 1997)

- Changed module PCB from 6-Layer to 4-Layer.
- Changed Module Part No. from KMM5362205CW/CWG to KMM5362205C2W/C2WG caused by PCB revision .

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KMM5362205C2W/C2WG Fast Page Mode with Extended Data Out
 2M x 36 DRAM SIMM using 1Mx16 and 4M Quad CAS EDO, 1K Refresh,

GENERAL DESCRIPTION

The Samsung KMM5362205C2W is a 2Mx36bits Dynamic RAM high density memory module. The Samsung KMM5362205C2W consists of four CMOS 1Mx16bits DRAMs in 42-pin SOJ package and two CMOS 1Mx4 bit Quad CAS with EDO DRAM in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5362205C2W is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
-5	50ns	15ns	90ns	25ns
-6	60ns	17ns	110ns	30ns

FEATURES

- Part Identification
 - KMM5362205C2W(1024 cycles/16ms Ref, SOJ, Solder)
 - KMM5362205C2WG(1024 cycles/16ms Ref, SOJ, Gold)
- Fast Page Mode with Extended Data Out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V ±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(750mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ19	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ20	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ21	45	$\overline{\text{RAS1}}$
10	Vcc	46	NC
11	NC	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	Res(A10)	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	Res(A11)	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{\text{A9}}$	68	PD2
33	$\overline{\text{RAS1}}$	69	PD3
34	$\overline{\text{RAS0}}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

Pin Name	Function
A0 - A9	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Row Address Strobe
$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
Res	Reserved Pin

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

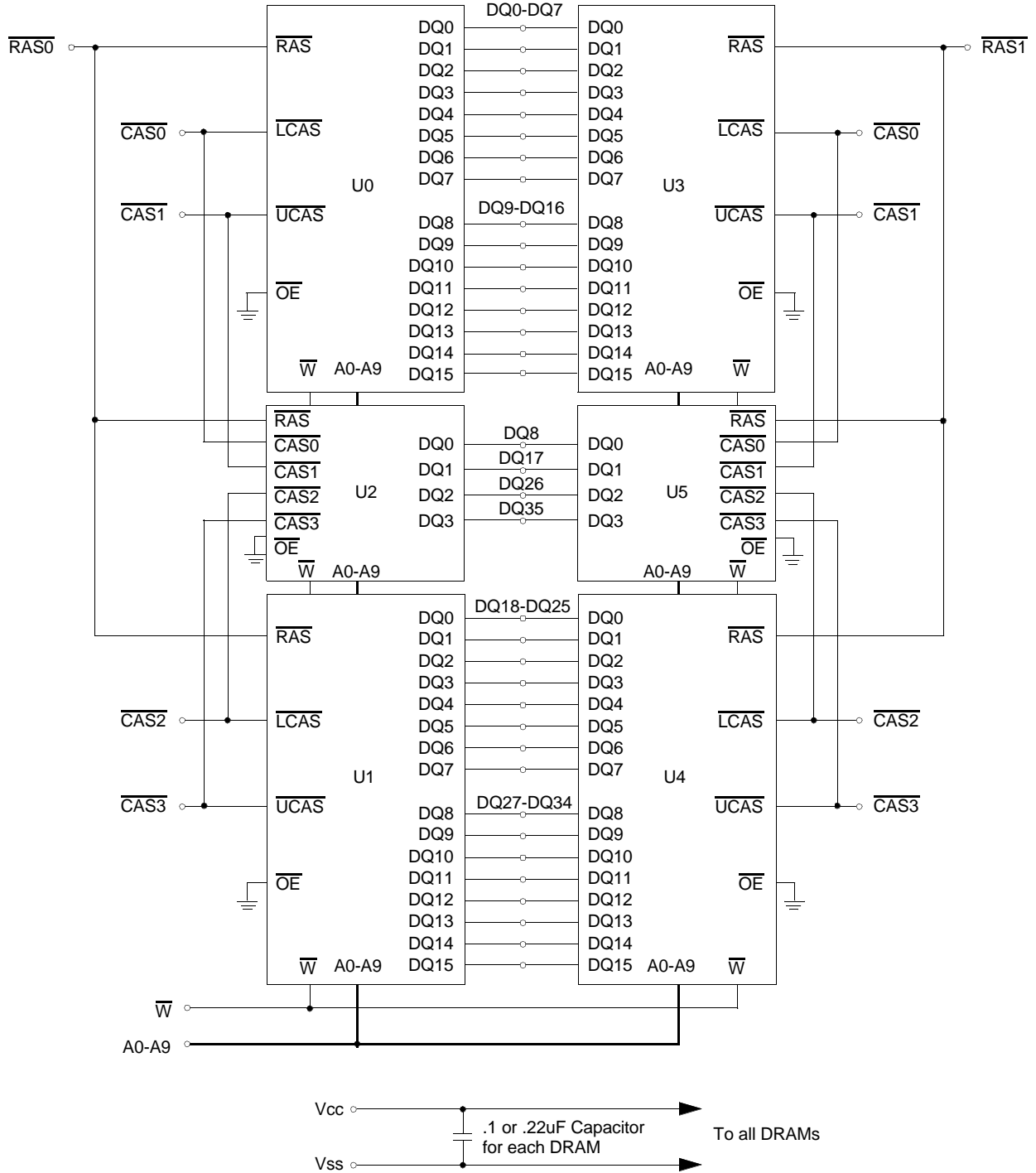
* Pin connection changing available

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DRAM MODULE

KMM5362205C2W/C2WG

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{ss}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	6	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1*1	V
Input Low Voltage	V _{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5322205C2W/C2WG		Unit
		Min	Max	
I _{CC1}	-5	-	391	mA
	-6	-	361	mA
I _{CC2}	Don't care	-	12	mA
I _{CC3}	-5	-	391	mA
	-6	-	361	mA
I _{CC4}	-5	-	331	mA
	-6	-	301	mA
I _{CC5}	Don't care	-	6	mA
I _{CC6}	-5	-	391	mA
	-6	-	361	mA
I _{I(L)}	Don't care	-30	30	uA
I _{O(L)}	Don't care	-10	10	uA
V _{OH}	Don't care	2.4	-	V
V _{OL}		-	0.4	V

I_{CC1} : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @ t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @ t_{RC}=min)

I_{CC4} : EDO Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @ t_{RC}=min)

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.5V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

DRAM MODULE

KMM5362205C2W/C2WG

CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	CIN1	-	50	pF
Input capacitance[\overline{W}]	CIN2	-	60	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS1}$]	CIN3	-	35	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	CIN4	-	40	pF
Input/Output capacitance[$\overline{DQ0-35}$]	CDQ1	-	30	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=5.0V ± 10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		ns	
Access time from \overline{RAS}	trAC		50		60	ns	3,4,10
Access time from \overline{CAS}	tcAC		15		17	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
\overline{CAS} to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	tT	2	50	2	50	ns	2
\overline{RAS} precharge time	trP	30		40		ns	
\overline{RAS} pulse width	trAS	50	10K	60	10K	ns	
\overline{RAS} hold time	trSH	13		17		ns	
\overline{CAS} hold time	tcSH	40		50		ns	
\overline{CAS} pulse width	tcAS	8	10K	10	10K	ns	13
\overline{RAS} to \overline{CAS} delay time	trCD	20	37	20	45	ns	4
\overline{RAS} to column address delay time	trAD	15	25	15	30	ns	10
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	trAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to \overline{RAS} lead time	trAL	25		30		ns	
Read command set-up time	trCS	0		0		ns	
Read command hold time referenced to \overline{CAS}	trCH	0		0		ns	8
Read command hold time referenced to \overline{RAS}	trRH	0		0		ns	8
Write command hold time	twCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to \overline{RAS} lead time	trWL	13		15		ns	
Write command to \overline{CAS} lead time	tcWL	13		10		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	8		10		ns	9
Refresh period	tREF		16		16	ms	
Write command set-up time	twCS	0		0		ns	7
\overline{CAS} setup time(\overline{CAS} -before- \overline{RAS} refresh)	tcSR	5		5		ns	
\overline{CAS} hold time(\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		ns	
\overline{RAS} precharge to \overline{CAS} hold time	trPC	5		5		ns	
Access time from \overline{CAS} precharge	tCPA		30		35	ns	3

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

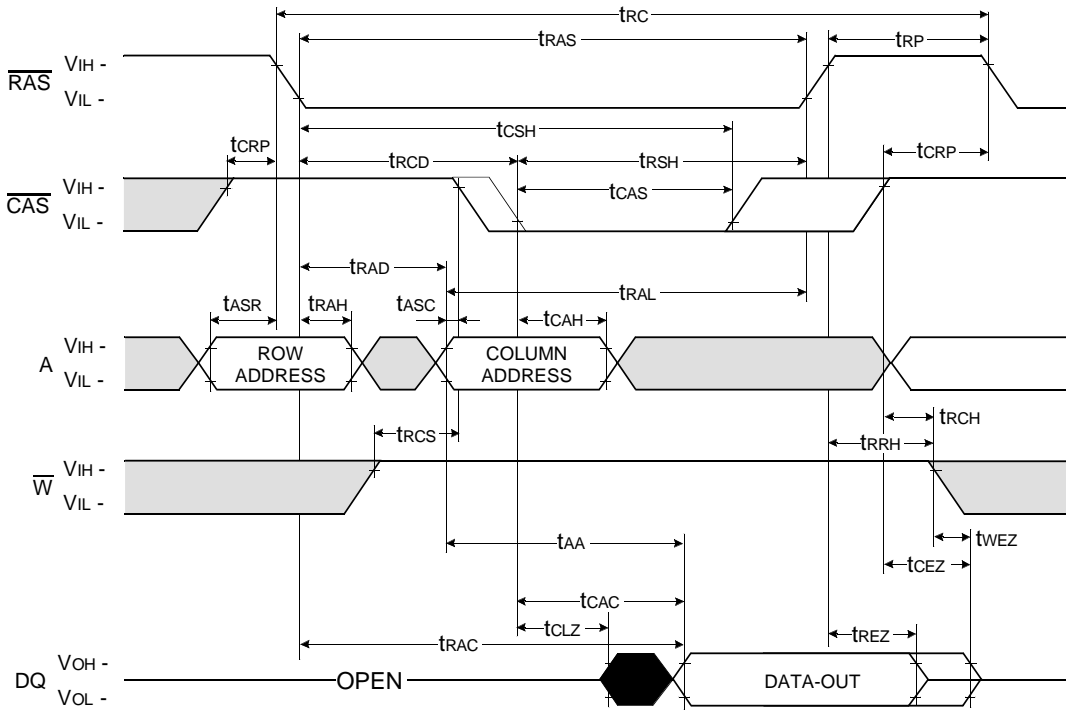
Test condition : Vin/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	tHPC	25		30		ns	13
$\overline{\text{CAS}}$ precharge time(Hyper page cycle)	tCP	8		10		ns	
$\overline{\text{RAS}}$ pulse width(Hyper page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	13	3	15	ns	6,11,12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	13	3	15	ns	6,11
$\overline{\text{W}}$ to data delay	tWED	15		15		ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	tWPE	5		5		ns	
Hold time $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high	tCLCH	5		5		ns	

NOTES

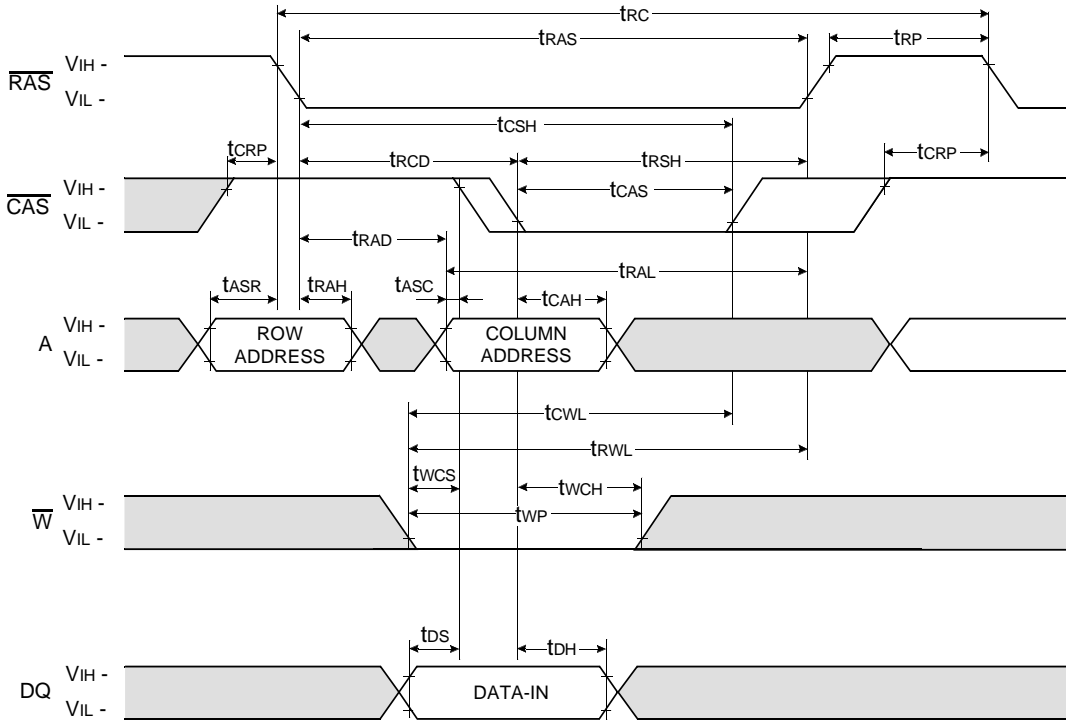
- An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t_{RCD}(max) limit insures that t_{TRAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RCD}≥t_{RCD}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristic s only. If t_{WCS}≥t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{TRAD}(max) limit insures that t_{TRAC}(max) can be met. t_{TRAD}(max) is specified as reference point only. If t_{TRAD} is greater than the specified t_{TRAD}(max) limit, then access time is controlled by t_{AA}.
- t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
- t_{ASC}≥t_{CP} min
- In order to hold the address latched by the first $\overline{\text{CAS}}$ going low, the parameter t_{CLCH} must be met.

READ CYCLE



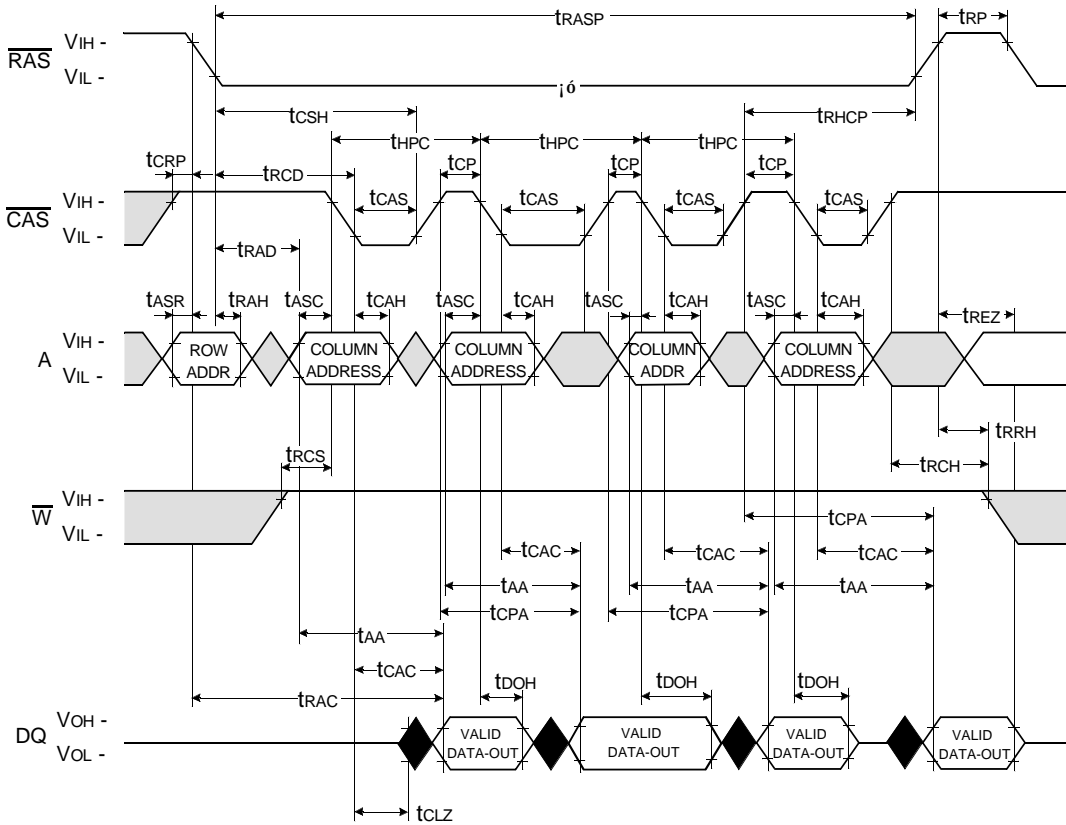
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

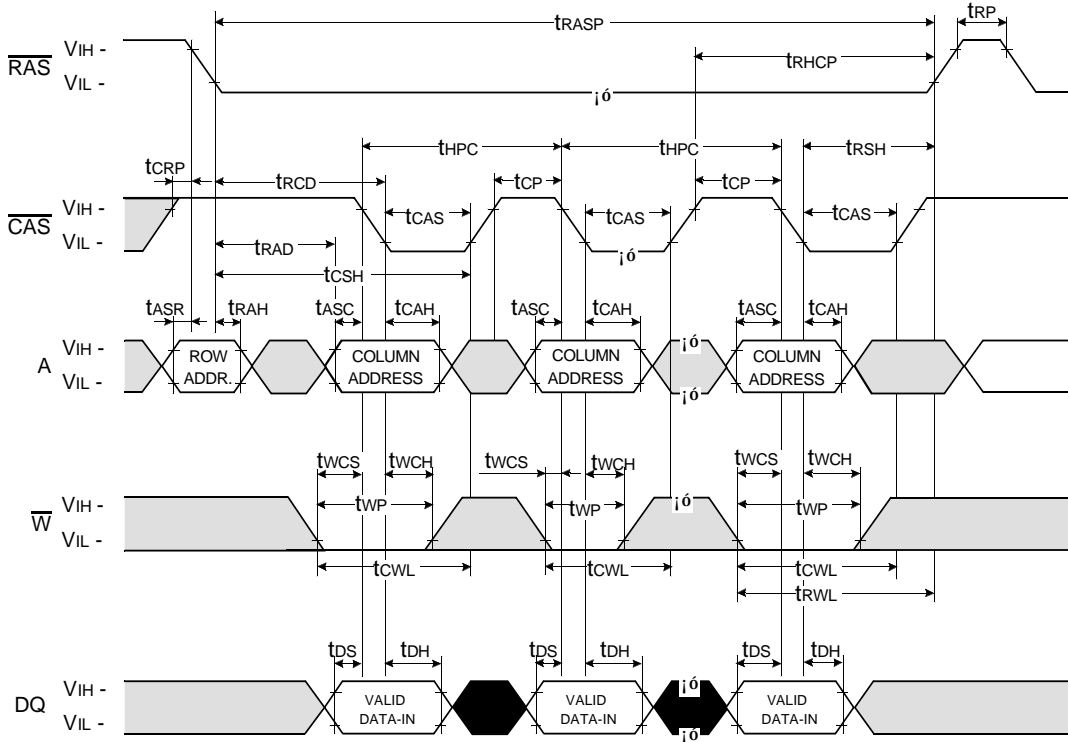
HYPER PAGE READ CYCLE



Don't care
 Undefined

HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

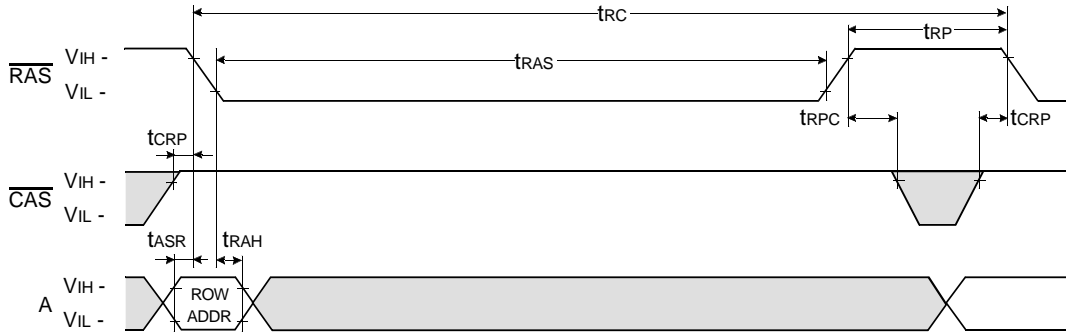


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

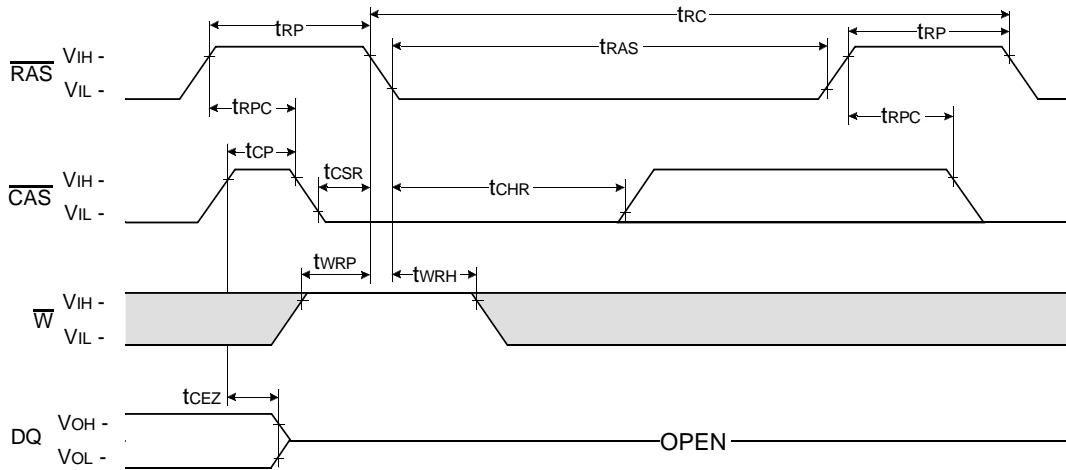
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

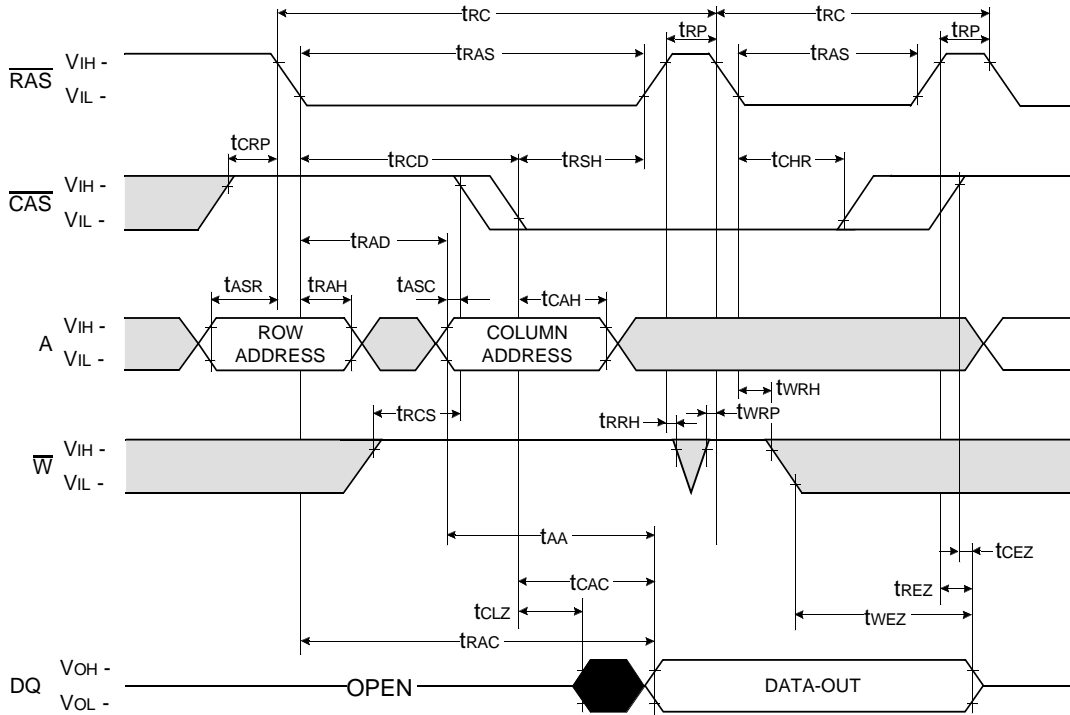
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

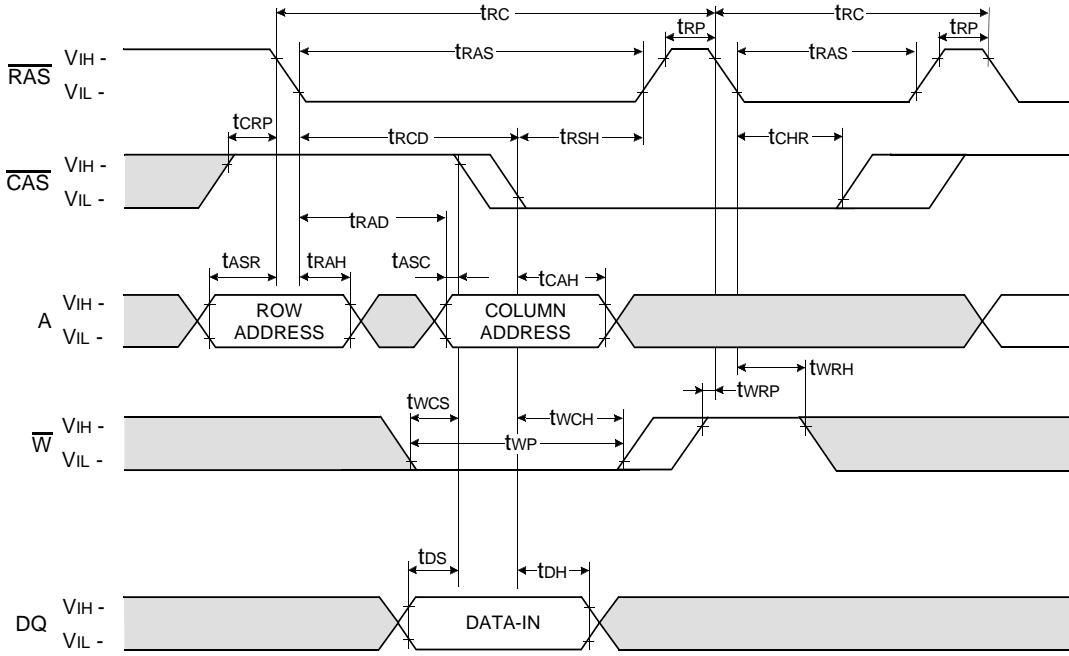
HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined

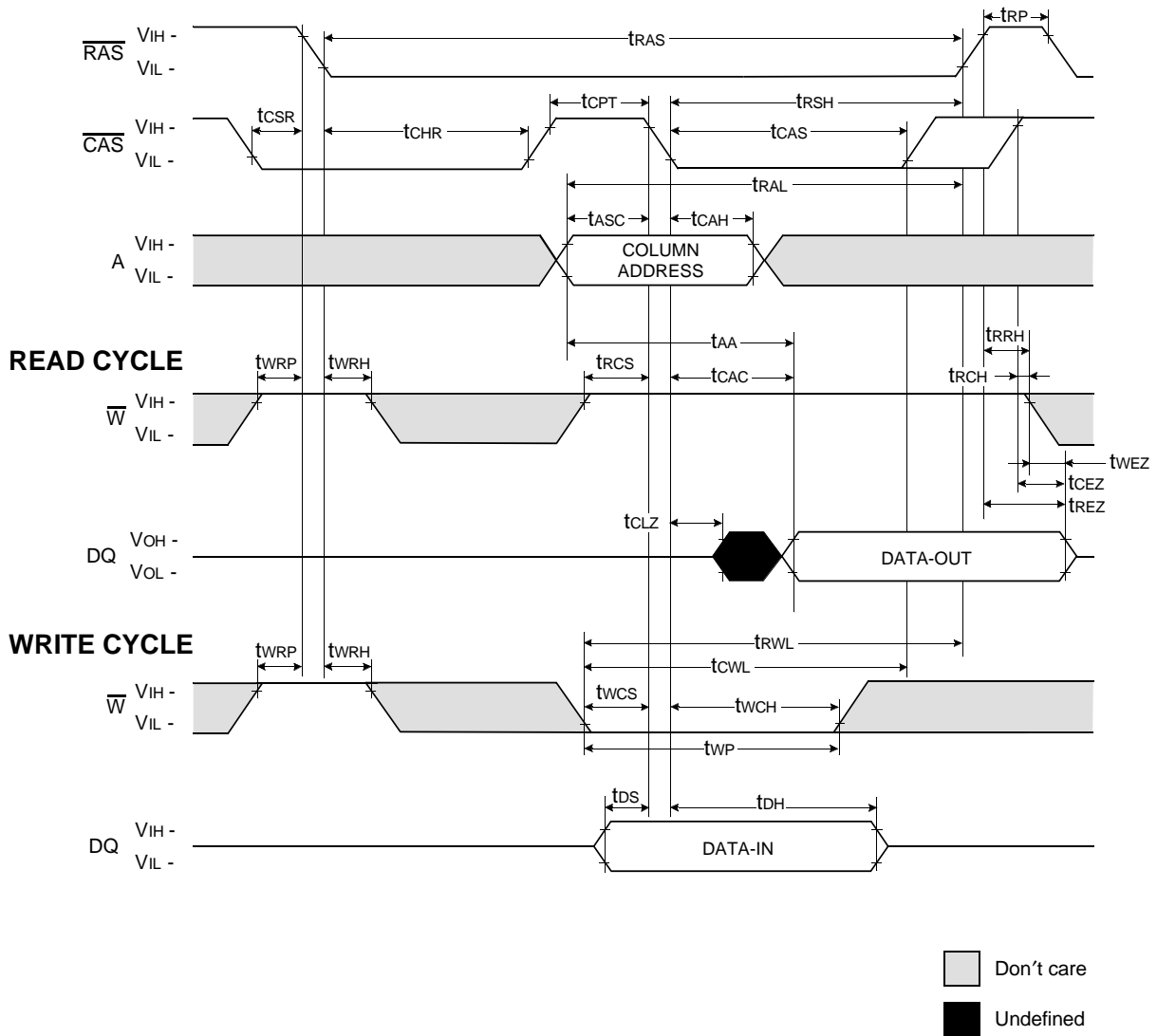
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

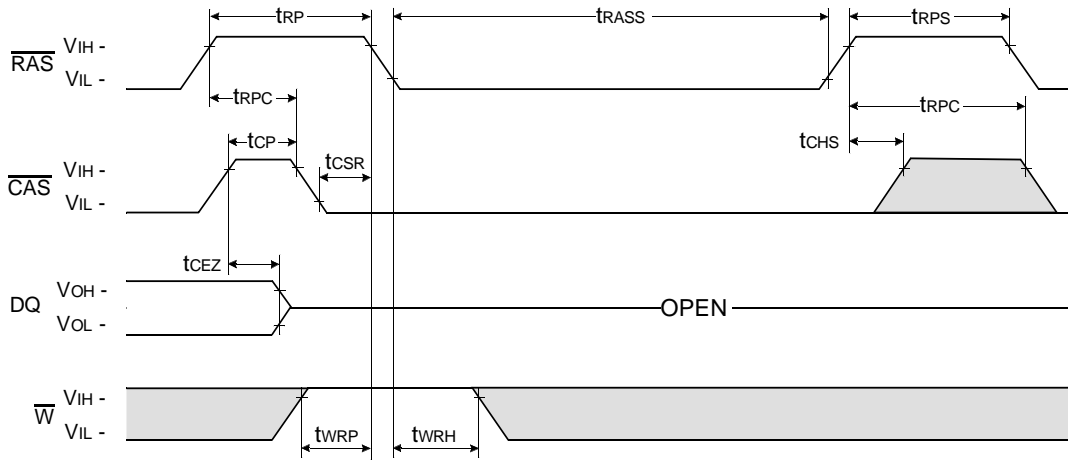
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

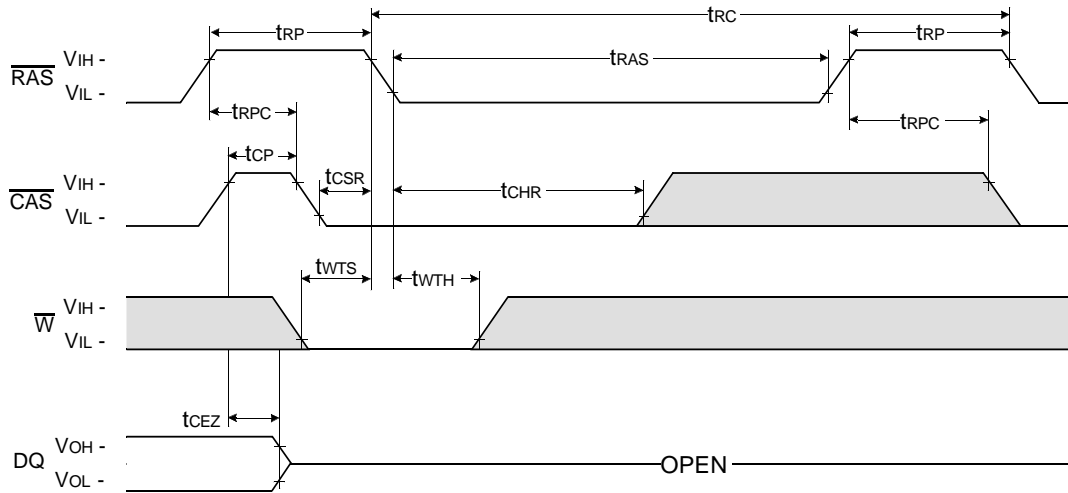
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



□ Don't care
 ■ Undefined

