

KMM53616000BK/BKG Fast Page Mode

16M x 36 DRAM SIMM Using 16Mx4 & 16Mx1, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53616000B is a 16Mx36bits Dynamic RAM high density memory module. The Samsung KMM53616000B consists of eight CMOS 16Mx4bits DRAMs and four CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53616000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | t _{RAC} | t _{CAC} | t _{RC} | t _{PC} |
|-------|------------------|------------------|-----------------|-----------------|
| -5 | 50ns | 13ns | 90ns | 35ns |
| -6 | 60ns | 15ns | 110ns | 40ns |

FEATURES

- Part Identification
 - KMM53616000BK(4K cycles/64ms Ref, SOJ, Solder)
 - KMM53616000BKG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ & Hidden Refresh capability
- $\overline{\text{RAS}}$ -only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

| Pin | Symbol | Pin | Symbol |
|-----|--------------------------|-----|--------------------------|
| 1 | V _{ss} | 37 | DQ17 |
| 2 | DQ0 | 38 | DQ35 |
| 3 | DQ18 | 39 | $\overline{\text{Vss}}$ |
| 4 | DQ1 | 40 | $\overline{\text{CAS0}}$ |
| 5 | DQ19 | 41 | $\overline{\text{CAS2}}$ |
| 6 | DQ2 | 42 | $\overline{\text{CAS3}}$ |
| 7 | DQ20 | 43 | $\overline{\text{CAS1}}$ |
| 8 | DQ3 | 44 | $\overline{\text{RAS0}}$ |
| 9 | DQ21 | 45 | NC |
| 10 | V _{cc} | 46 | NC |
| 11 | NC | 47 | $\overline{\text{W}}$ |
| 12 | A0 | 48 | NC |
| 13 | A1 | 49 | DQ9 |
| 14 | A2 | 50 | DQ27 |
| 15 | A3 | 51 | DQ10 |
| 16 | A4 | 52 | DQ28 |
| 17 | A5 | 53 | DQ11 |
| 18 | A6 | 54 | DQ29 |
| 19 | A10 | 55 | DQ12 |
| 20 | DQ4 | 56 | DQ30 |
| 21 | DQ22 | 57 | DQ13 |
| 22 | DQ5 | 58 | DQ31 |
| 23 | DQ23 | 59 | V _{cc} |
| 24 | DQ6 | 60 | DQ32 |
| 25 | DQ24 | 61 | DQ14 |
| 26 | DQ7 | 62 | DQ33 |
| 27 | DQ25 | 63 | DQ15 |
| 28 | A7 | 64 | DQ34 |
| 29 | A11 | 65 | DQ16 |
| 30 | V _{cc} | 66 | NC |
| 31 | A8 | 67 | PD1 |
| 32 | A9 | 68 | PD2 |
| 33 | NC | 69 | PD3 |
| 34 | $\overline{\text{RAS2}}$ | 70 | PD4 |
| 35 | DQ26 | 71 | NC |
| 36 | DQ8 | 72 | V _{ss} |

PIN NAMES

| Pin Name | Function |
|---|-----------------------|
| A0 - A11 | Address Inputs |
| DQ0 - DQ35 | Data In/Out |
| $\overline{\text{W}}$ | Read/Write Enable |
| $\overline{\text{RAS0}}, \overline{\text{RAS2}}$ | Row Address Strobe |
| $\overline{\text{CAS0}} - \overline{\text{CAS3}}$ | Column Address Strobe |
| PD1 -PD4 | Presence Detect |
| V _{cc} | Power(+5V) |
| V _{ss} | Ground |
| NC | No Connection |

PRESENCE DETECT PINS (Optional)

| Pin | 50NS | 60NS |
|-----|-----------------|-----------------|
| PD1 | V _{ss} | V _{ss} |
| PD2 | NC | NC |
| PD3 | V _{ss} | NC |
| PD4 | V _{ss} | NC |

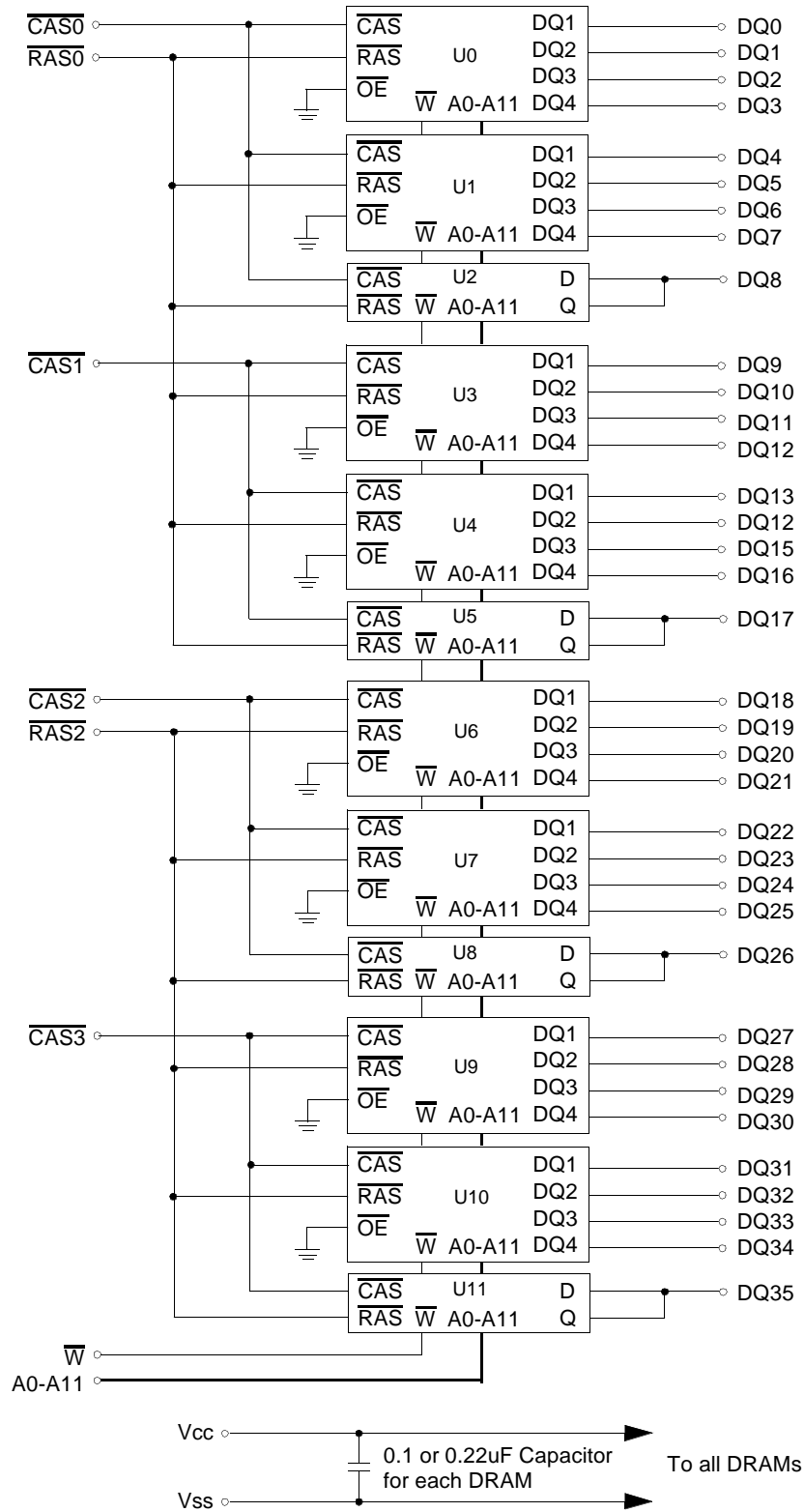
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DRAM MODULE

KMM53616000BK/BKG

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|-------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -1 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _d | 12 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|-------------------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{CC} ^{*1} | V |
| Input Low Voltage | V _{IL} | -1.0 ^{*2} | - | 0.8 | V |

*1 : V_{CC}+2.0V at pulse width ≤ 20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | KMM53616000BK/BKG | | Unit |
|-------------------|------------|-------------------|------|------|
| | | Min | Max | |
| I _{CC1} | -5 | - | 1320 | mA |
| | -6 | - | 1200 | mA |
| I _{CC2} | Don't care | - | 24 | mA |
| I _{CC3} | -5 | - | 1320 | mA |
| | -6 | - | 1200 | mA |
| I _{CC4} | -5 | - | 880 | mA |
| | -6 | - | 760 | mA |
| I _{CC5} | Don't care | - | 12 | mA |
| I _{CC6} | -5 | - | 1320 | mA |
| | -6 | - | 1200 | mA |
| I _{I(L)} | Don't care | -10 | 10 | uA |
| I _{O(L)} | | -5 | 5 | uA |
| V _{OH} | Don't care | 2.4 | - | V |
| V _{OL} | | - | 0.4 | V |

I_{CC1} : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : tpc=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.5V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, tpc.



DRAM MODULE

KMM53616000BK/BKG

CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Input capacitance[A0-A11] | CIN1 | - | 70 | pF |
| Input capacitance[\overline{W}] | CIN2 | - | 94 | pF |
| Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$] | CIN3 | - | 52 | pF |
| Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$] | CIN4 | - | 31 | pF |
| Input/Output capacitance[$\overline{DQ0-35}$] | CDQ | - | 17 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading $CL=100pF$

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|--|--------|-----|-----|-----|-----|------|--------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 90 | | 110 | | ns | |
| Access time from \overline{RAS} | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from \overline{CAS} | tCAC | | 13 | | 15 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | ns | 3,10 |
| \overline{CAS} to output in Low-Z | tCLZ | 0 | | 0 | | ns | 3 |
| Output buffer turn-off delay | tOFF | 0 | 13 | 0 | 15 | ns | 6 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| \overline{RAS} precharge time | tRP | 30 | | 40 | | ns | |
| \overline{RAS} pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| \overline{RAS} hold time | tRSH | 13 | | 15 | | ns | |
| \overline{CAS} hold time | tCSH | 50 | | 60 | | ns | |
| \overline{CAS} pulse width | tCAS | 13 | 10K | 15 | 10K | ns | |
| \overline{RAS} to \overline{CAS} delay time | tRCD | 20 | 37 | 20 | 45 | ns | 4 |
| \overline{RAS} to column address delay time | tRAD | 15 | 25 | 15 | 30 | ns | 10 |
| \overline{CAS} to \overline{RAS} precharge time | tCRP | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 10 | | 10 | | ns | |
| Column address to \overline{RAS} lead time | tRAL | 25 | | 30 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to \overline{CAS} | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to \overline{RAS} | tRRH | 0 | | 0 | | ns | 8 |
| Write command hold time | tWCH | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | ns | |
| Write command to \overline{RAS} lead time | tRWL | 15 | | 15 | | ns | |
| Write command to \overline{CAS} lead time | tCWL | 13 | | 15 | | ns | |
| Data set-up time | tDS | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 10 | | 10 | | ns | 9 |
| Refresh period | tREF | | 64 | | 64 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| \overline{CAS} setup time(\overline{CAS} -before- \overline{RAS} refresh) | tCSR | 5 | | 5 | | ns | |
| \overline{CAS} hold time(\overline{CAS} -before- \overline{RAS} refresh) | tCHR | 10 | | 10 | | ns | |
| \overline{RAS} to \overline{CAS} precharge time | tRPC | 5 | | 5 | | ns | |
| Access time from \overline{CAS} precharge | tCPA | | 30 | | 35 | ns | 3 |



AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V, output loading CL=100pF

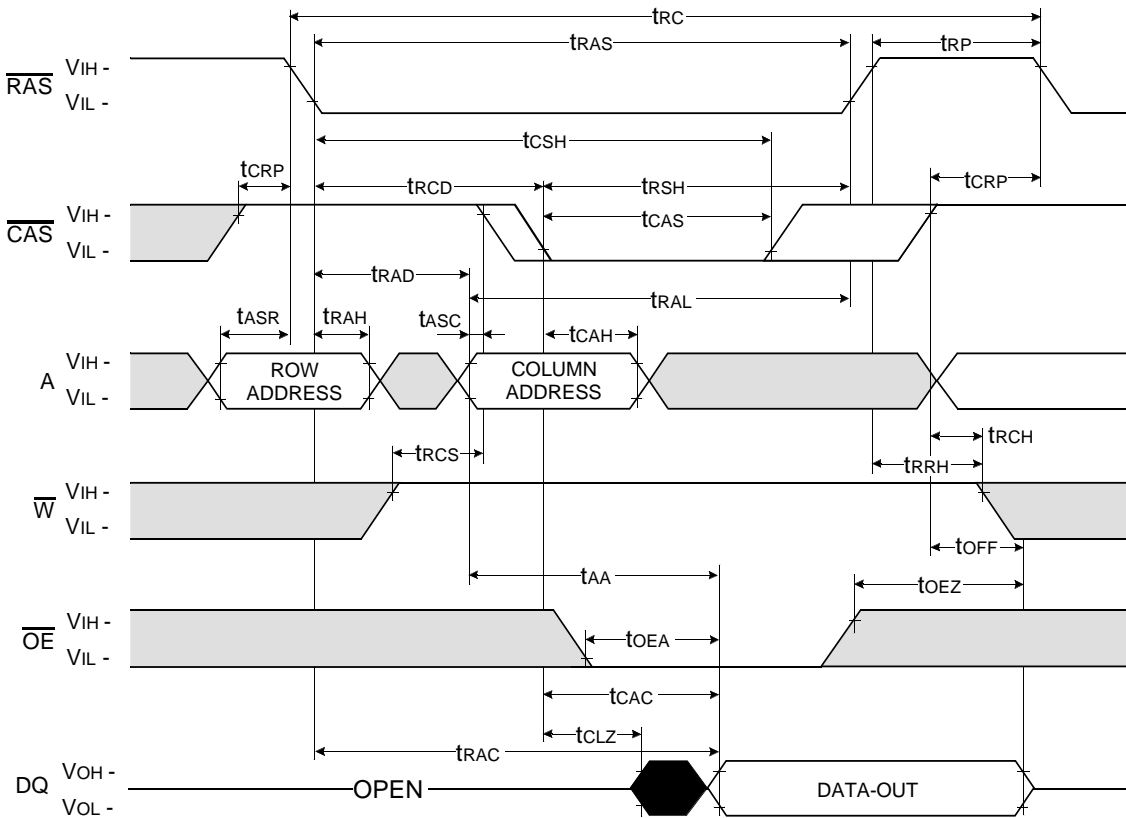
| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|--|--------|-----|------|-----|------|------|------|
| | | Min | Max | Min | Max | | |
| Fast page mode cycle time | tPC | 35 | | 40 | | ns | |
| $\overline{\text{CAS}}$ precharge time(Fast page cycle) | tCP | 10 | | 10 | | ns | |
| $\overline{\text{RAS}}$ pulse width(Fast page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh) | tWRP | 10 | | 10 | | ns | |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh) | tWRH | 10 | | 10 | | ns | |

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are VIH/VIL. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.



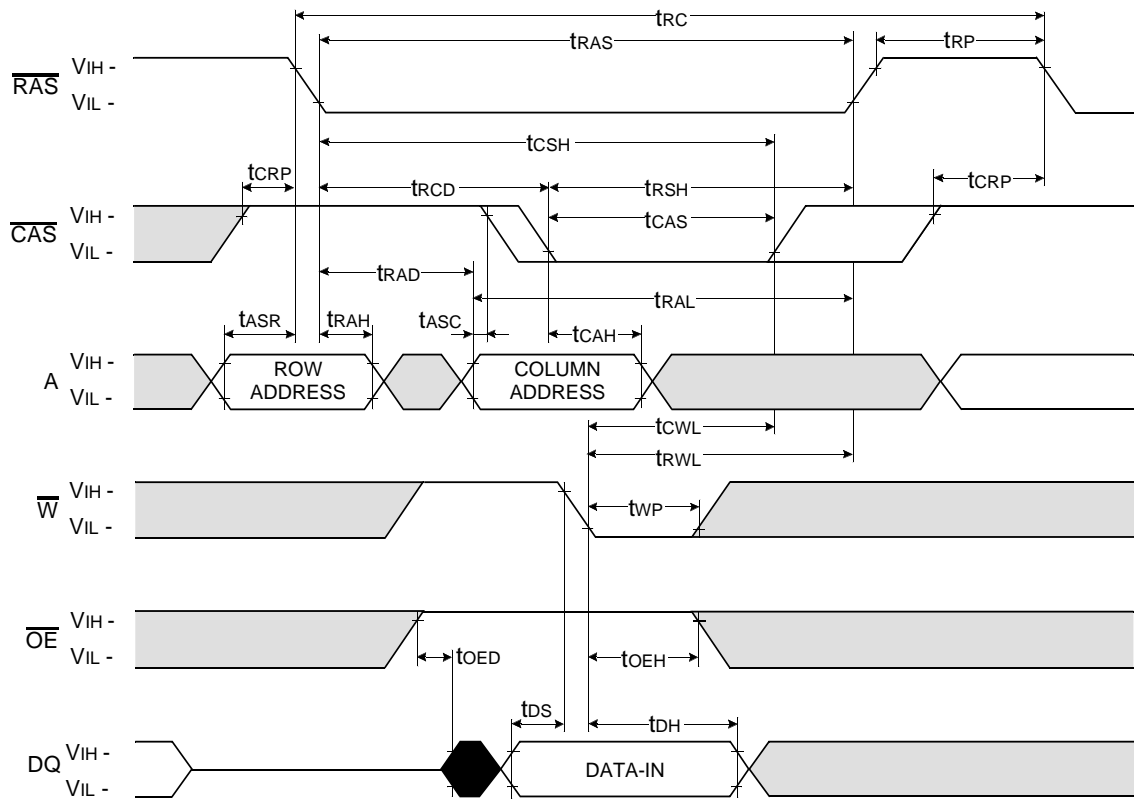
READ CYCLE



Don't care
 Undefined

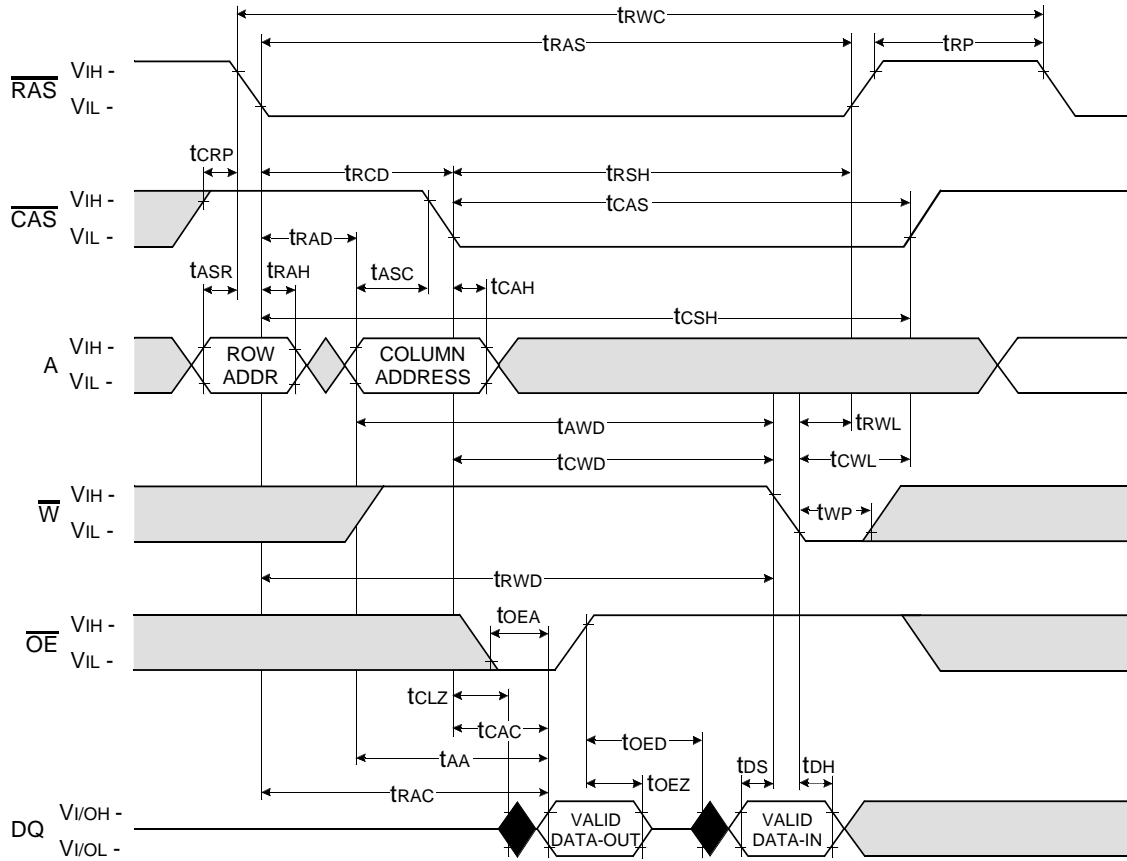
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

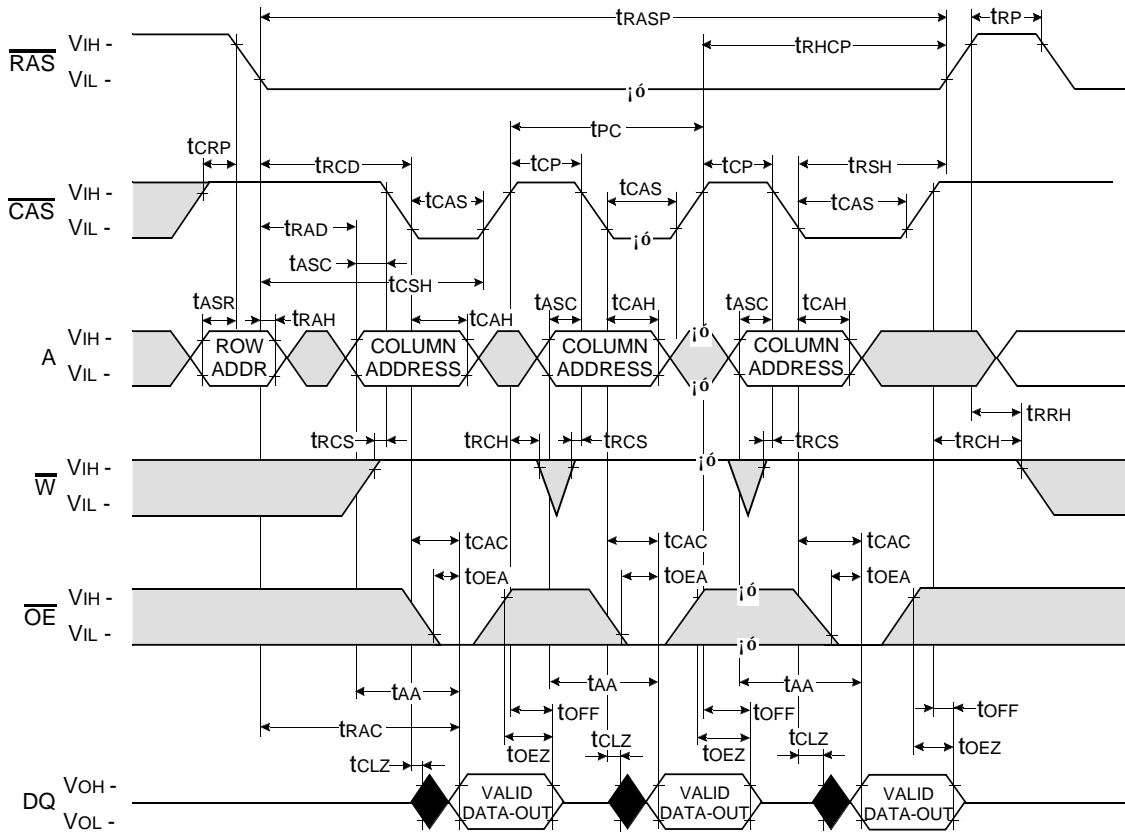
READ - MODIFY - WRTIE CYCLE



Don't care
 Undefined

FAST PAGE READ CYCLE

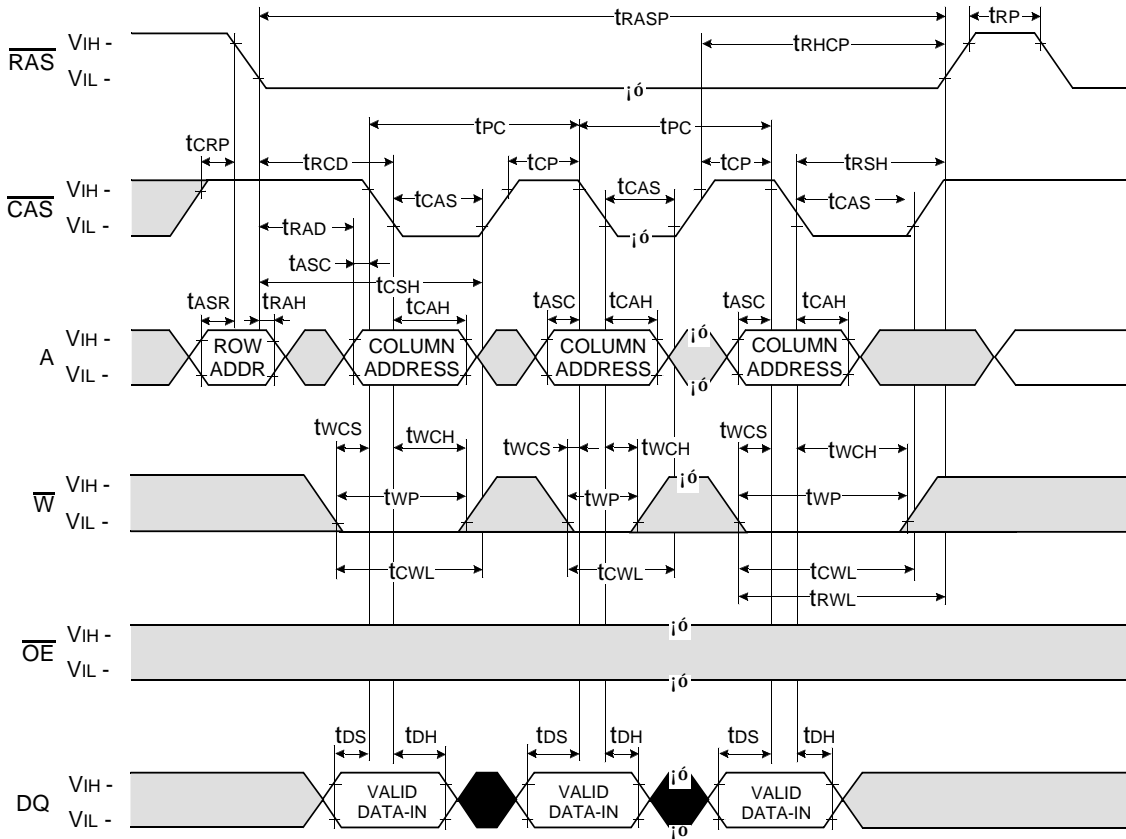
NOTE : DOUT = OPEN



Don't care
 Undefined

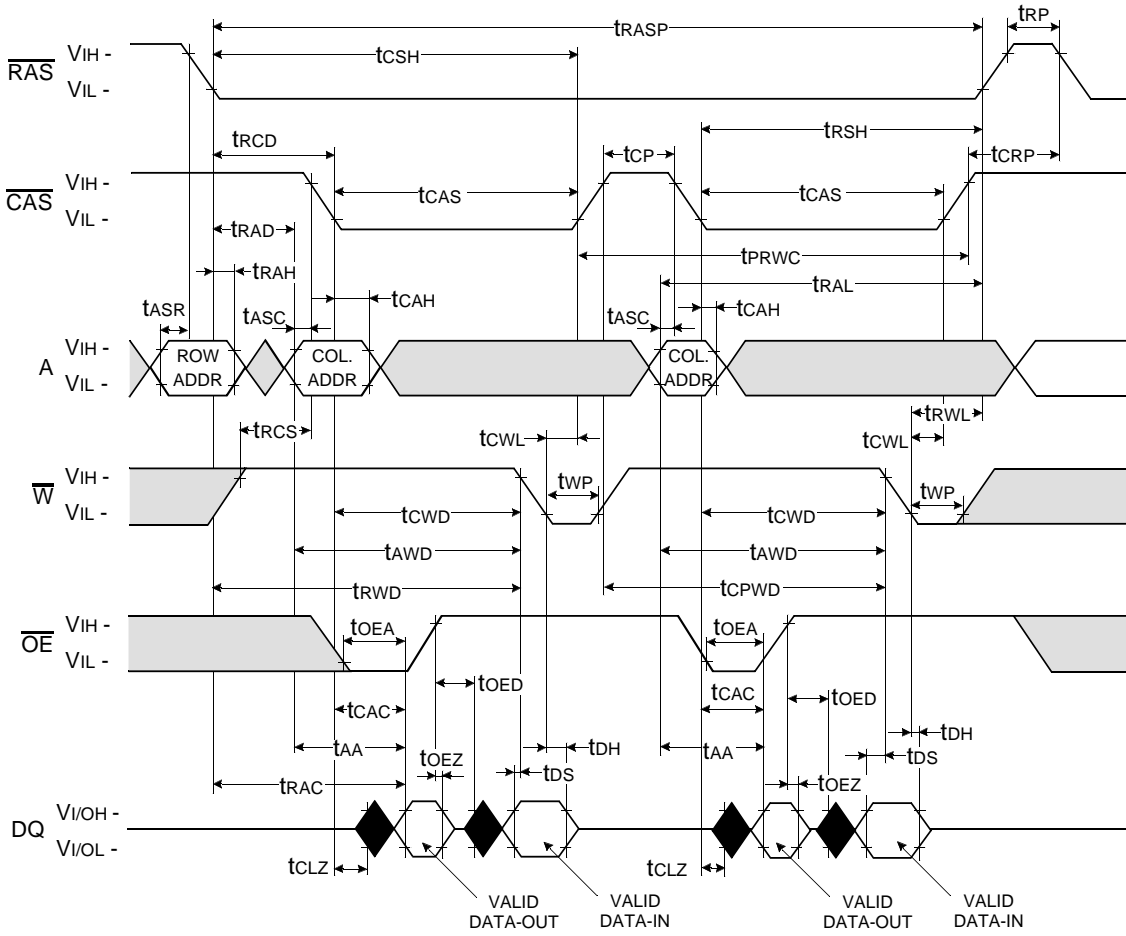
FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE

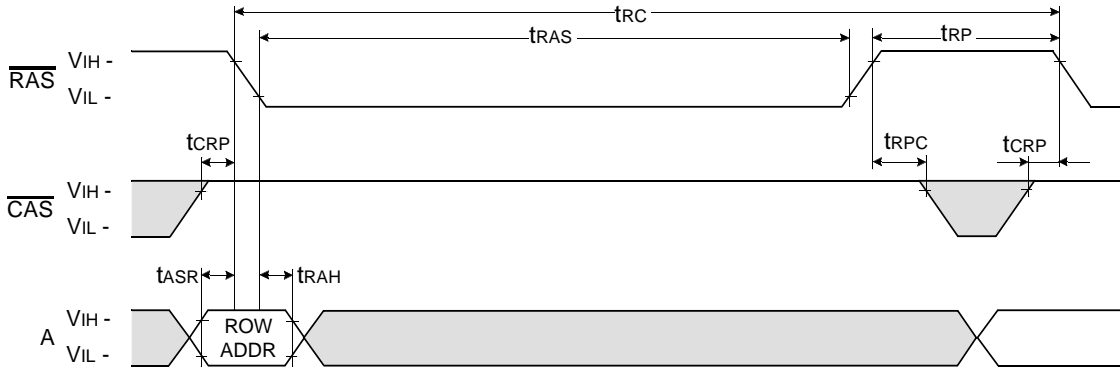


Don't care
 Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

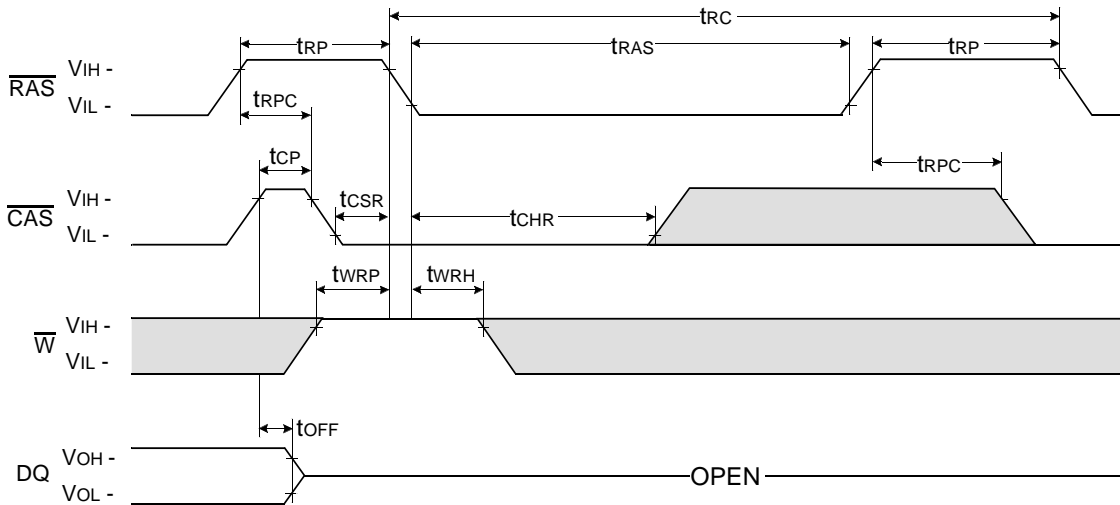
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



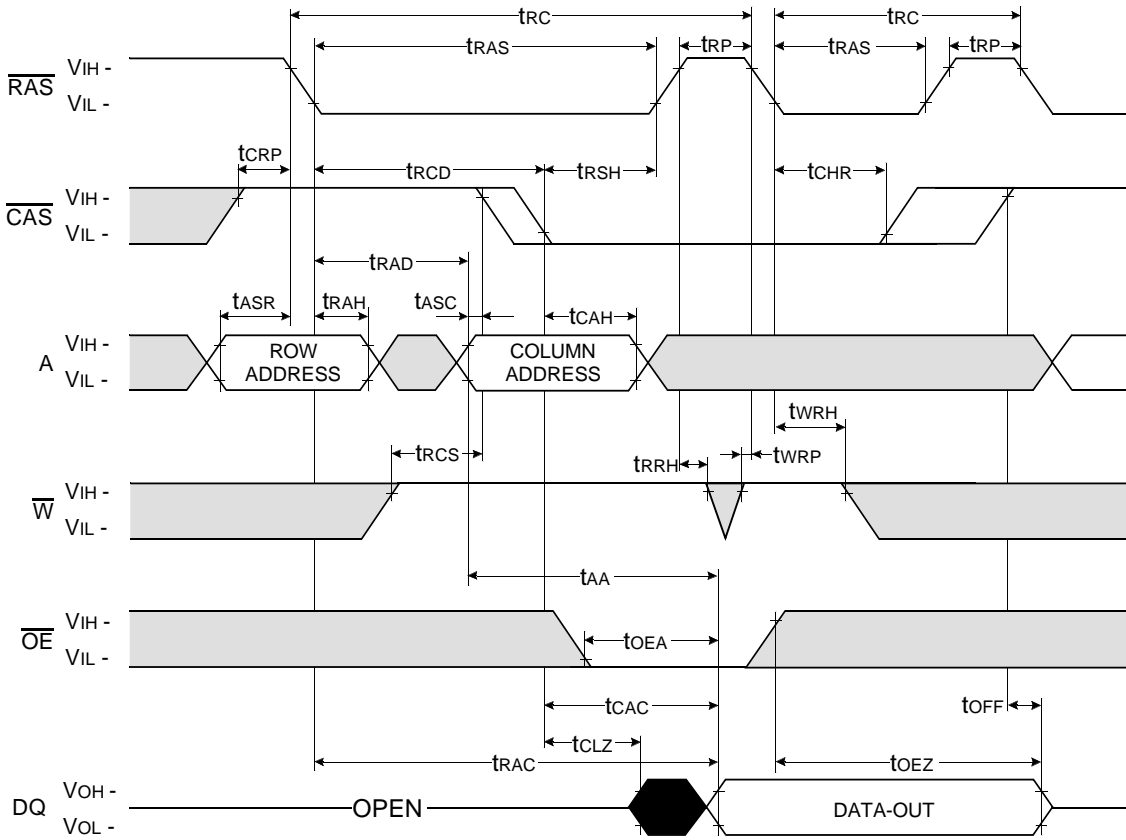
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

