1Mx36 DRAM SIMM

(1MX16 Base)

Revision 0.0

November 1997

Revision History

Version 0.0 (November 1997)

- Changed module PCB from 6-Layer to 4-Layer.
- Changed Module Part No. from KMM5361205CW/CWG to KMM5361205C2W/C2WG caused by PCB revision .

KMM5361205C2W/C2WG Fast Page Mode with Extended Data Out

1M x 36 DRAM SIMM using 1Mx16 and 4M Quad CAS EDO, 1K Refresh,

GENERAL DESCRIPTION

The Samsung KMM5361205C2W is a 1Mx36bits Dynamic RAM high density memory module. The Samsung KMM5361205C2W consists of two CMOS 1Mx16bits DRAMs in 42-pin SOJ package and one CMOS 1Mx4 bit Quad CAS with EDO DRAM in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5361205C2W is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	15ns	90ns	25ns
-6	60ns	17ns	110ns	30ns

FEATURES

- Part Identification
  - KMM5361205C2W(1024 cycles/16ms Ref, SOJ, Solder)
  - KMM5361205C2WG(1024 cycles/16ms Ref, SOJ, Gold)
- Fast Page Mode with Extended Data Out
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(750mil), single sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	Res($\overline{RAS1}$)
10	Vcc	46	NC
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	Res(A10)	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	Res(A11)	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	Res($\overline{RAS1}$)	69	PD3
34	$\overline{RAS0}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

Pin Name	Function
A0 - A9	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
Res	Reserved Pin

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

* Pin connection changing available

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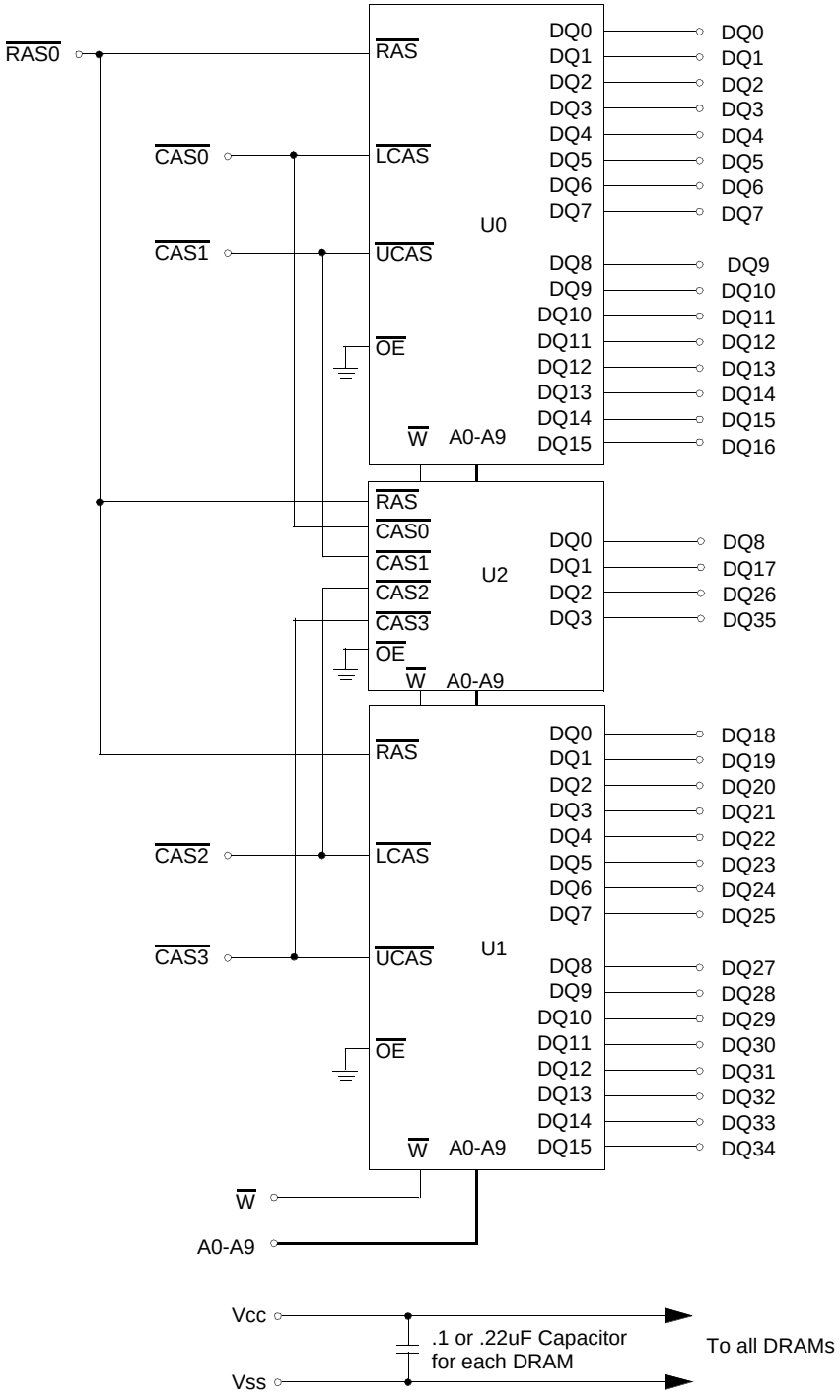
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	3	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1[*1]	V
Input Low Voltage	V_{IL}	-1.0[*2]	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5321205C2W/C2WG		Unit
		Min	Max	
I_{CC1}	-5	-	385	mA
	-6	-	355	mA
I_{CC2}	Don't care	-	6	mA
I_{CC3}	-5	-	385	mA
	-6	-	355	mA
I_{CC4}	-5	-	325	mA
	-6	-	295	mA
I_{CC5}	Don't care	-	3	mA
I_{CC6}	-5	-	385	mA
	-6	-	355	mA
$I_{I(L)}$	Don't care	-15	15	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	40	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	30	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	25	pF
Input/Output capacitance[DQ0-35]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		15		17	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		17		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		10		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

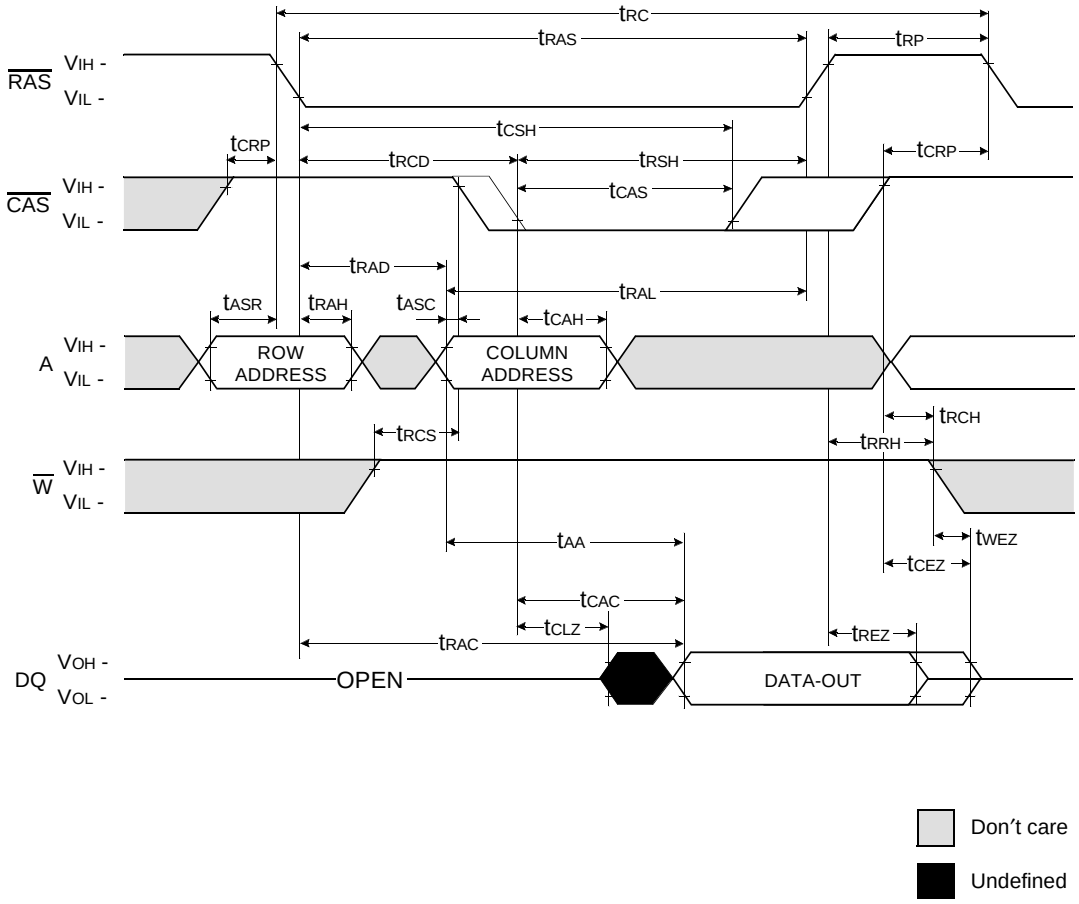
Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	25		30		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width(Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6,11
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		ns	

NOTES

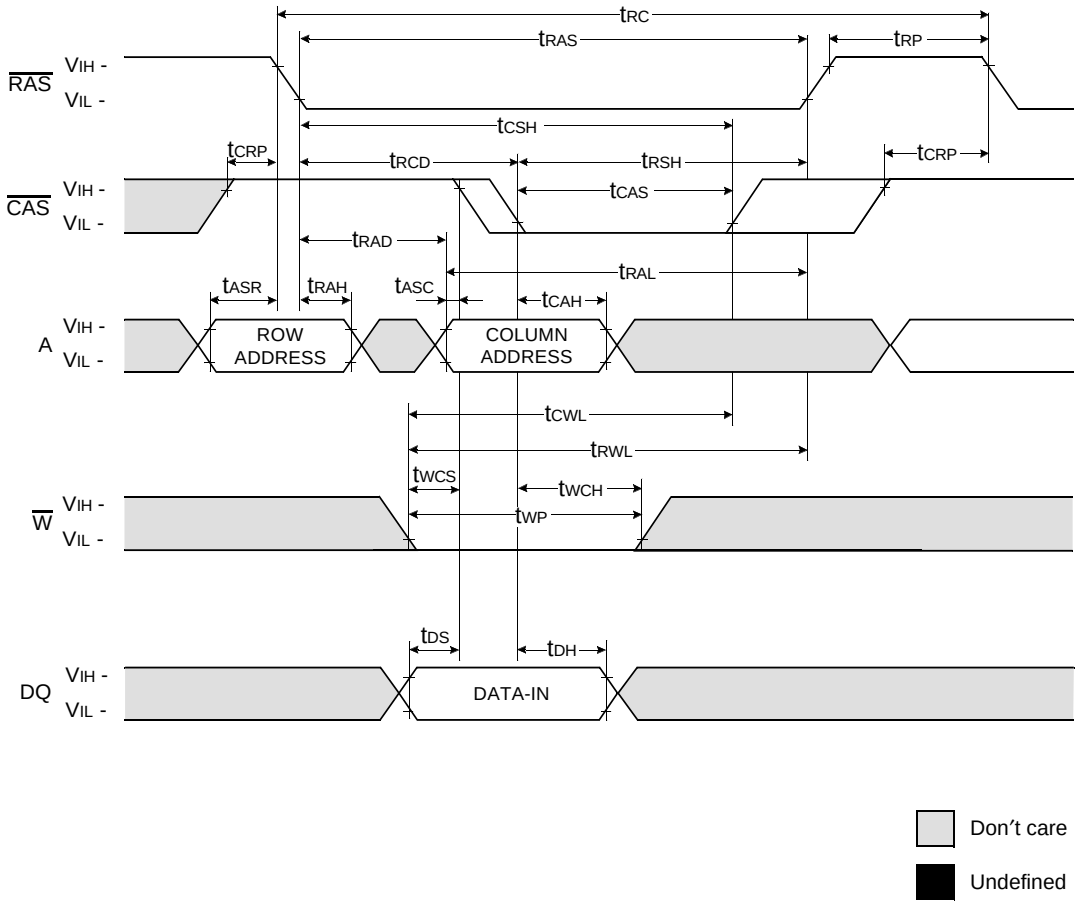
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristic s only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameter are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.
13. $t_{ASC} \geq t_{CP}$ min
14. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter t_{CLCH} must be met.

READ CYCLE

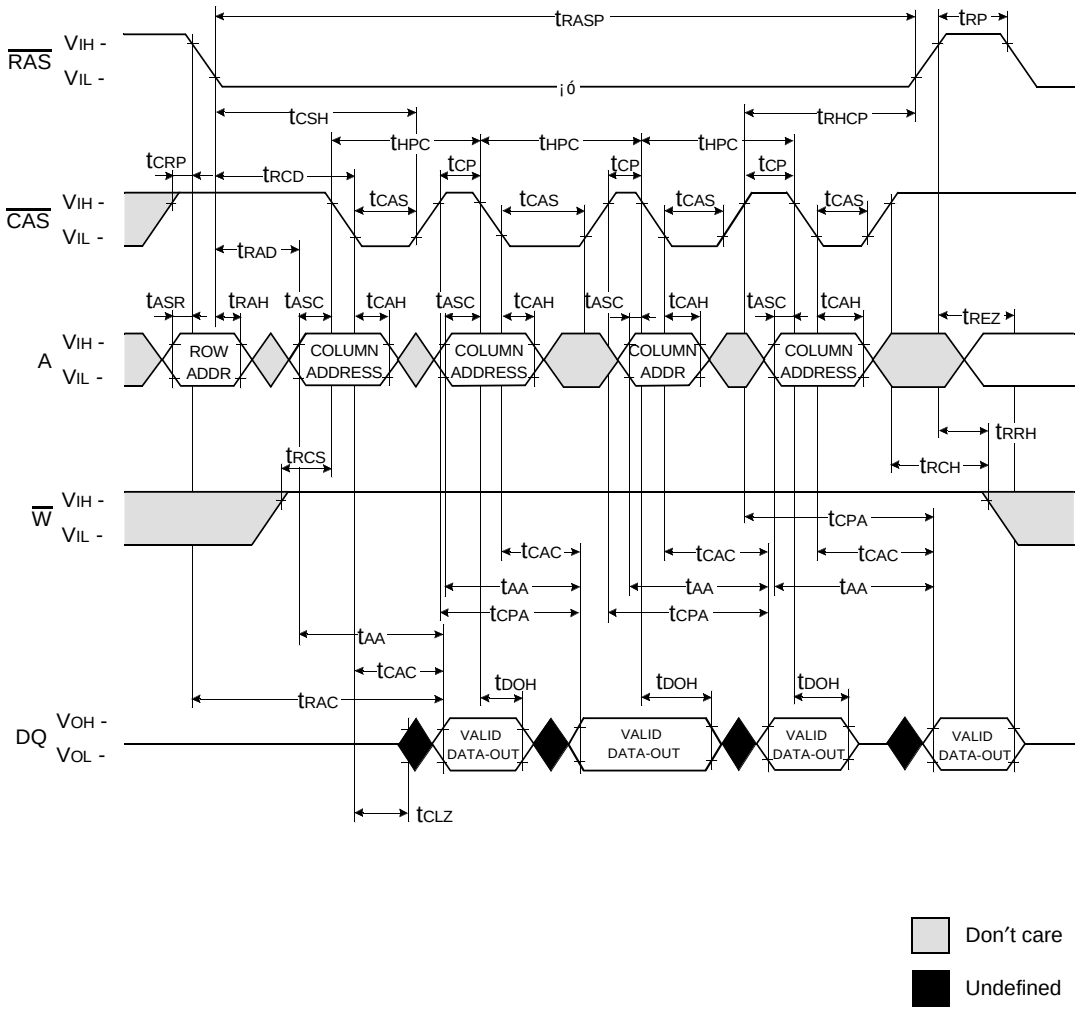


WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

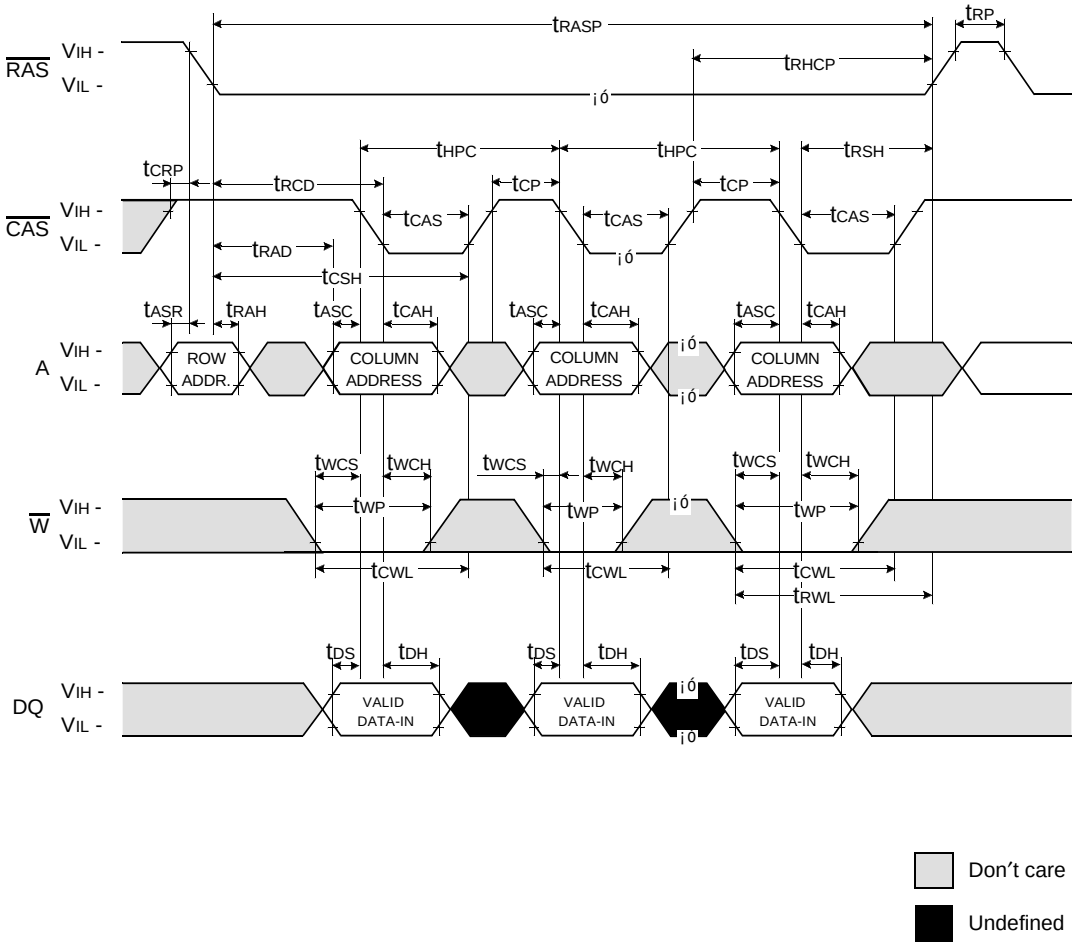


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

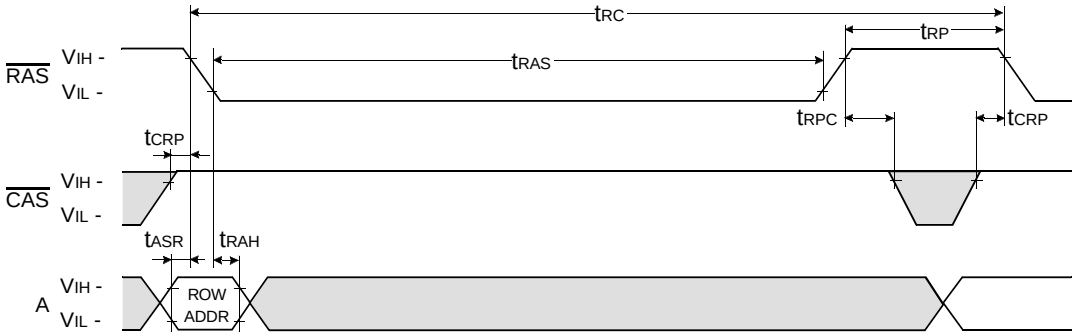
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE*

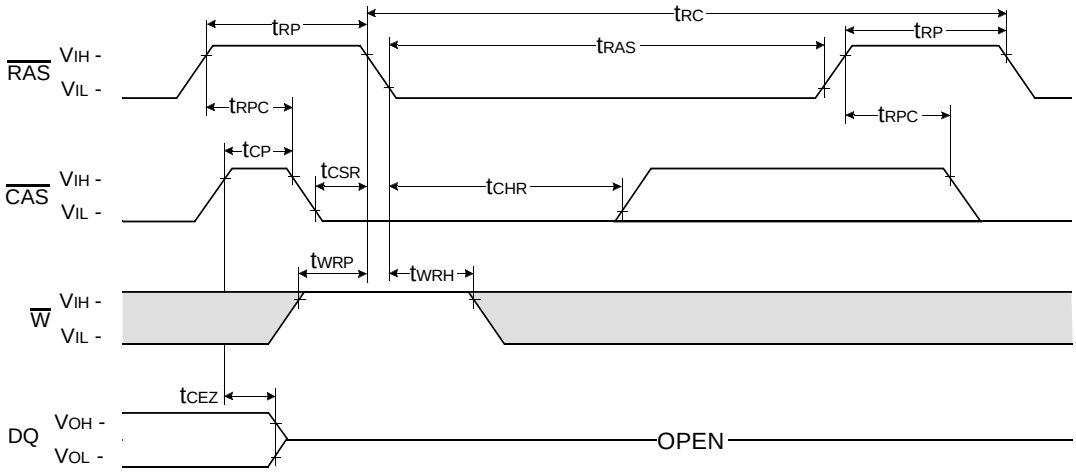
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

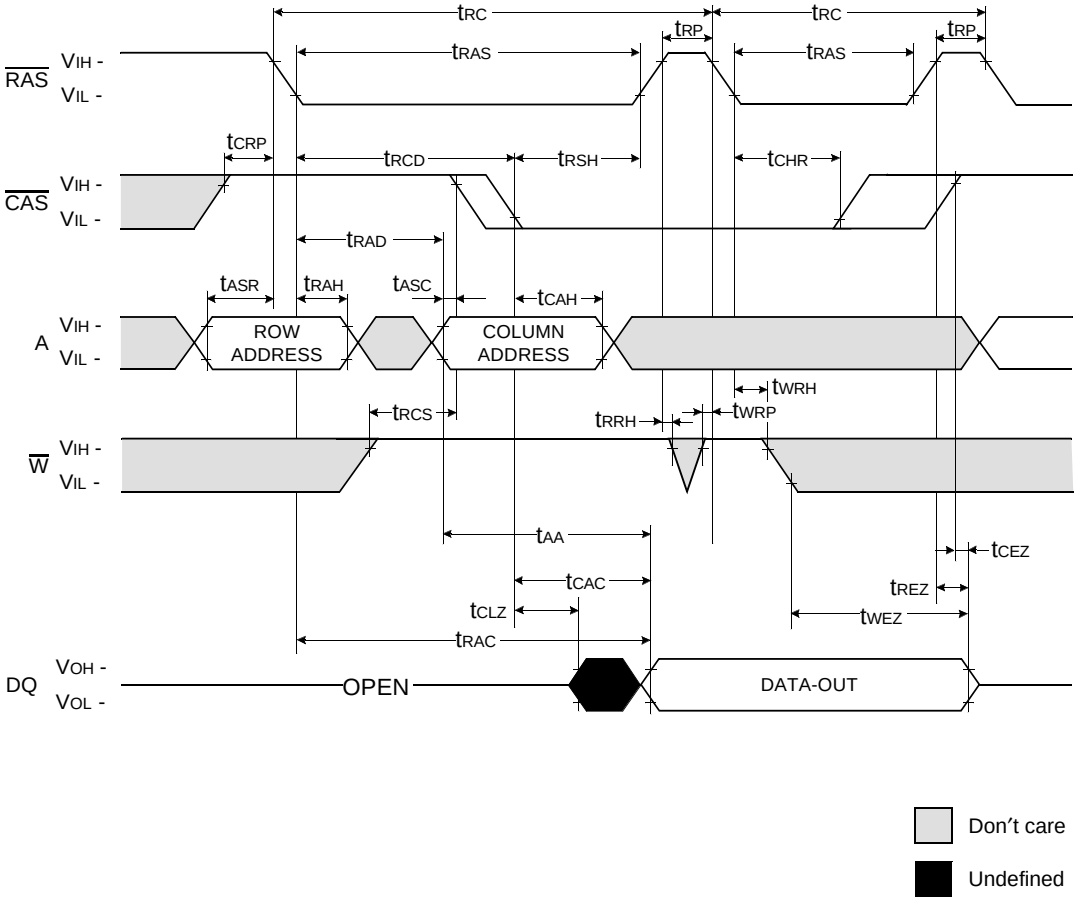


Don't care

Undefined

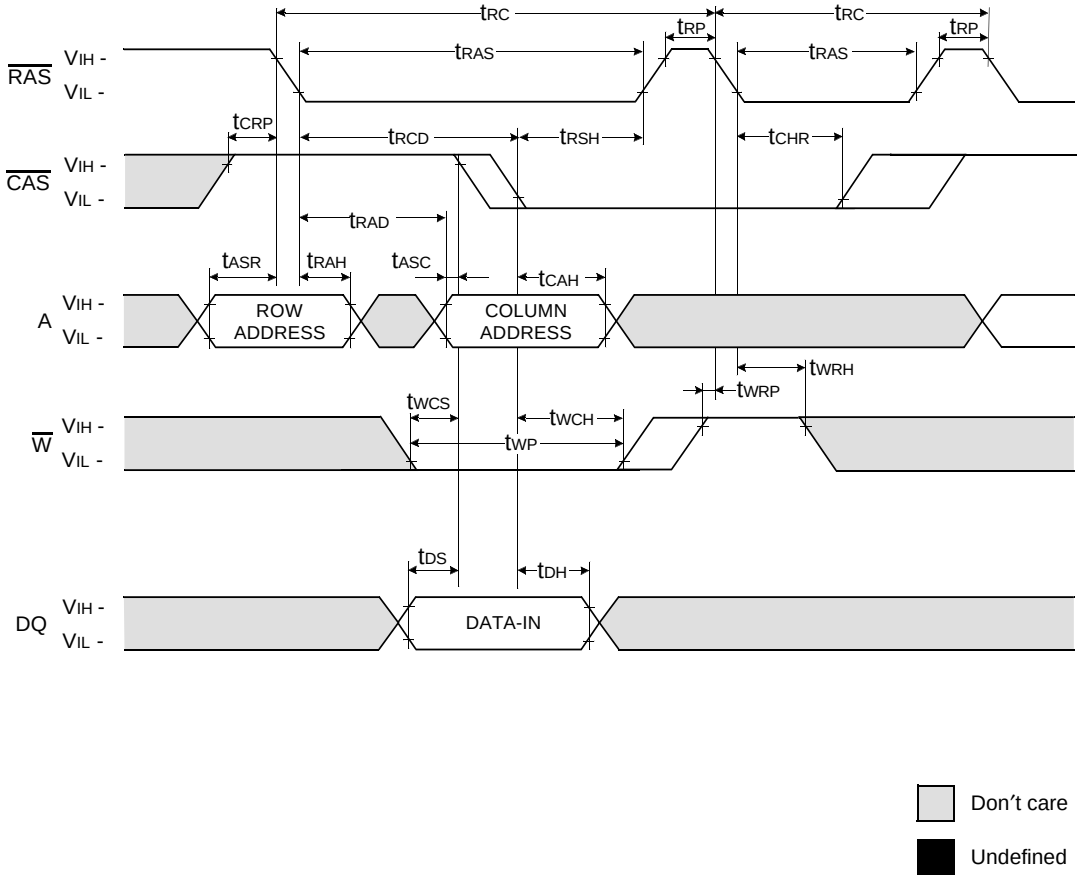
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)

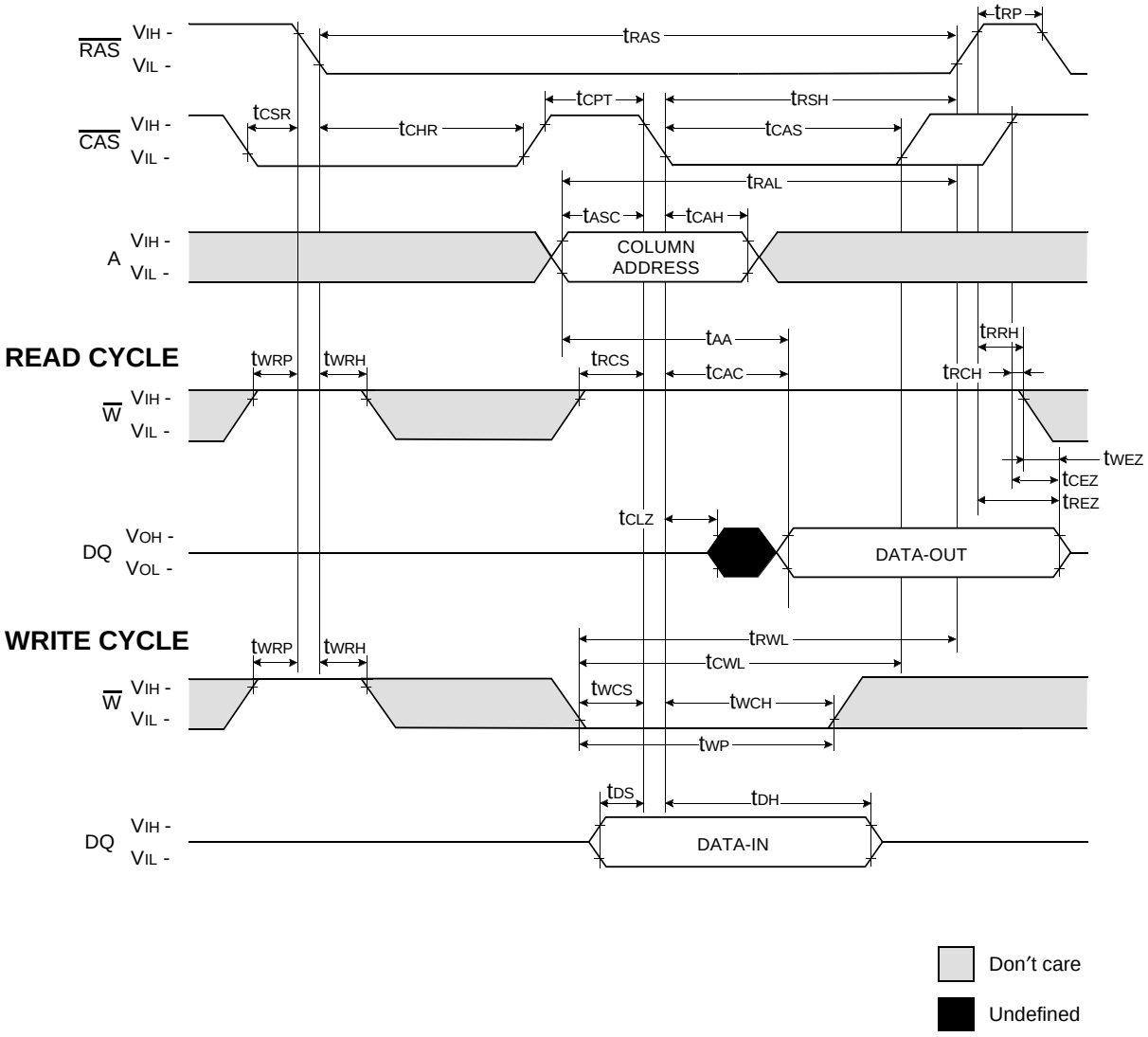


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



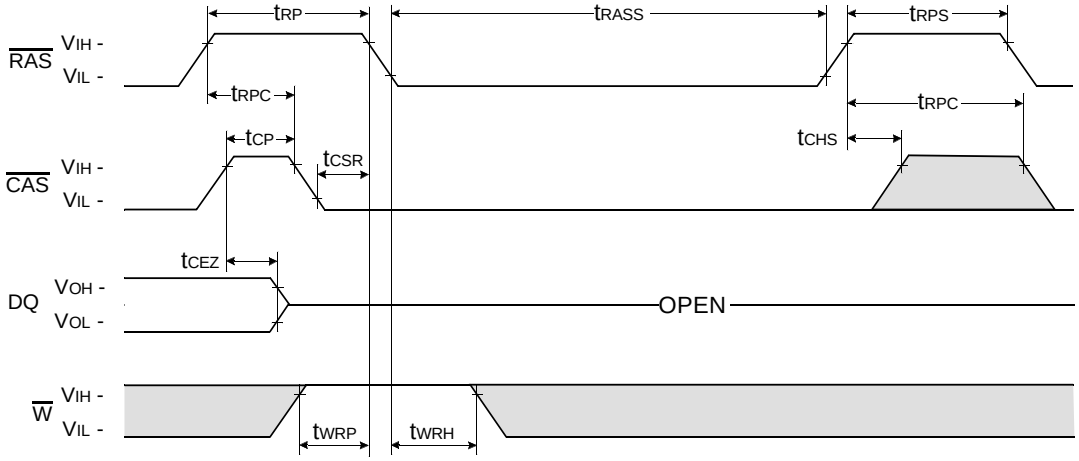
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

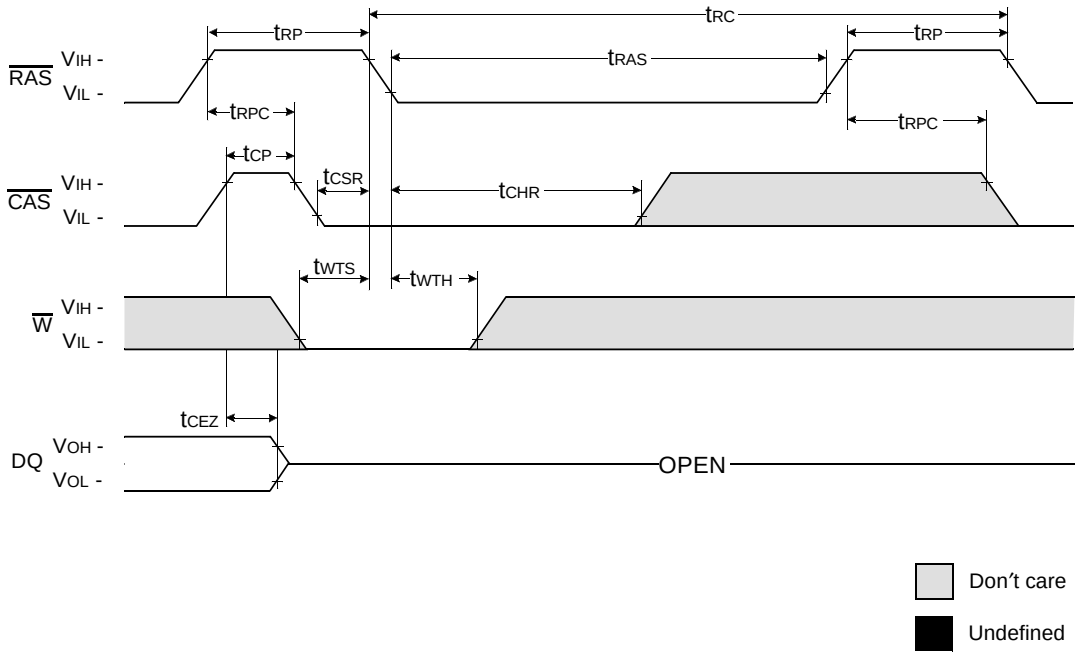
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



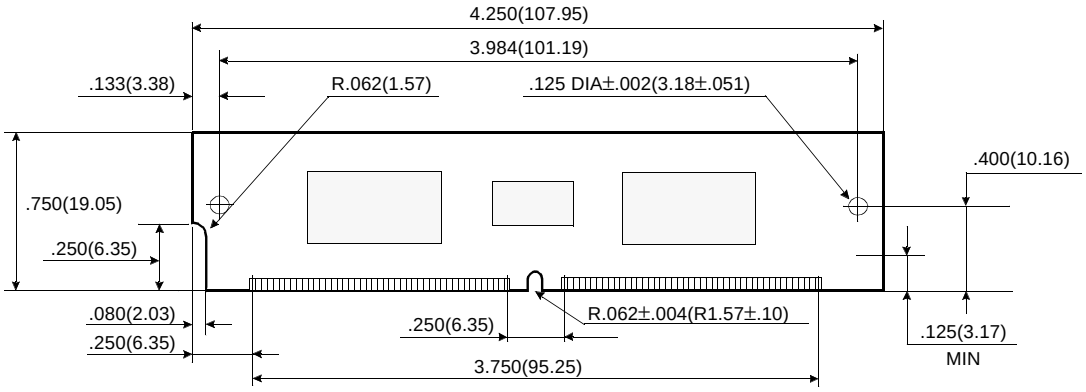
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

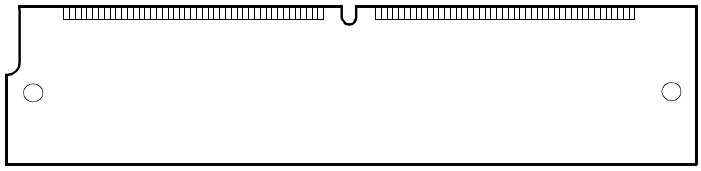


PACKAGE DIMENSIONS

Units : Inches (millimeters)

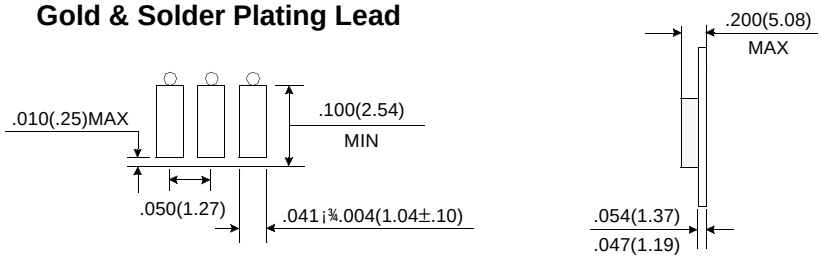


(Front view)



(Back view)

Gold & Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device are 1Mx16 EDO DRAM and 1Mx4 Quad CAS with EDO DRAM, TSOP

DRAM Part No. : KMM5361205C2W/C2WG -- KM416C1204CJ (400 mil)
-- KM44C1005DJ (300 mil)

Revision History
Rev 0.0 : Nov. 1997