

**KMM372V404BS Fast Page Mode**

4M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4 , 4K Refresh, 3.3V

**GENERAL DESCRIPTION**

The Samsung KMM372V404B is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V404B consists of four 4Mx16bits & two 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V404B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

**PERFORMANCE RANGE**

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

**FEATURES**

- Part Identification
- KMM372V404BS(4096cycles/64ms Ref. TSOP II)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except  $\overline{\text{RAS}}$  and DQ
- PCB : Height(1000mil), single sided component

**PIN CONFIGURATIONS**

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>ss</sub>	29	*CAS2	57	DQ22	85	V <sub>ss</sub>	113	*CAS3	141	DQ58
2	DQ0	30	RAS0	58	DQ23	86	DQ38	114	*RAS1	142	DQ59
3	DQ1	31	$\overline{\text{OE0}}$	59	V <sub>cc</sub>	87	DQ37	115	RFU	143	V <sub>cc</sub>
4	DQ2	32	V <sub>ss</sub>	60	DQ24	88	DQ38	116	V <sub>ss</sub>	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	V <sub>cc</sub>	34	A2	62	RFU	90	V <sub>cc</sub>	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	V <sub>ss</sub>	40	V <sub>cc</sub>	68	V <sub>ss</sub>	96	V <sub>ss</sub>	124	V <sub>cc</sub>	152	V <sub>ss</sub>
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	V <sub>ss</sub>	71	DQ30	99	DQ47	127	V <sub>ss</sub>	155	DQ66
16	DQ12	44	$\overline{\text{OE2}}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	RAS2	73	V <sub>cc</sub>	101	DQ49	129	*RAS3	157	V <sub>cc</sub>
18	V <sub>cc</sub>	46	CAS4	74	DQ32	102	V <sub>cc</sub>	130	*CAS5	158	DQ68
19	DQ14	47	*CAS6	75	DQ33	103	DQ50	131	*CAS7	159	DQ69
20	DQ15	48	W2	76	DQ34	104	DQ51	132	PDE	160	DQ70
21	DQ16	49	V <sub>cc</sub>	77	DQ35	105	DQ52	133	V <sub>cc</sub>	161	DQ71
22	DQ17	50	RSVD	78	V <sub>ss</sub>	106	DQ53	134	RSVD	162	V <sub>ss</sub>
23	V <sub>ss</sub>	51	RSVD	79	PD1	107	V <sub>ss</sub>	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	V <sub>cc</sub>	54	V <sub>ss</sub>	82	PD7	110	V <sub>cc</sub>	138	V <sub>ss</sub>	166	PD8
27	W0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	CAS0	56	DQ21	84	V <sub>cc</sub>	112	*CAS1	140	DQ57	168	V <sub>cc</sub>

**PIN NAMES**

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RAS0, RAS2	Row Address Strobe
CAS0, CAS4	Column Address Strobe
V <sub>cc</sub>	Power(+3.3V)
V <sub>ss</sub>	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked "\*" are not used in this module.

**PD & ID Table**

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD Note :PD & ID Terminals must each be pulled up through a register to V<sub>cc</sub> at the next higher level assembly. PDs will be either open (NC) or driven to V<sub>ss</sub> via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to V<sub>ss</sub> without a buffer.

PD : 0 for Vol of Drive IC & 1 for N.C

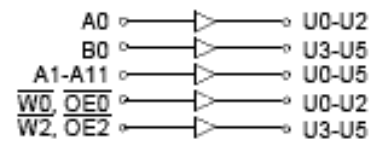
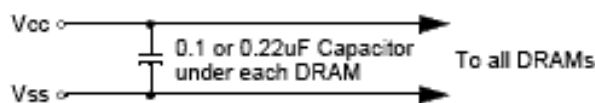
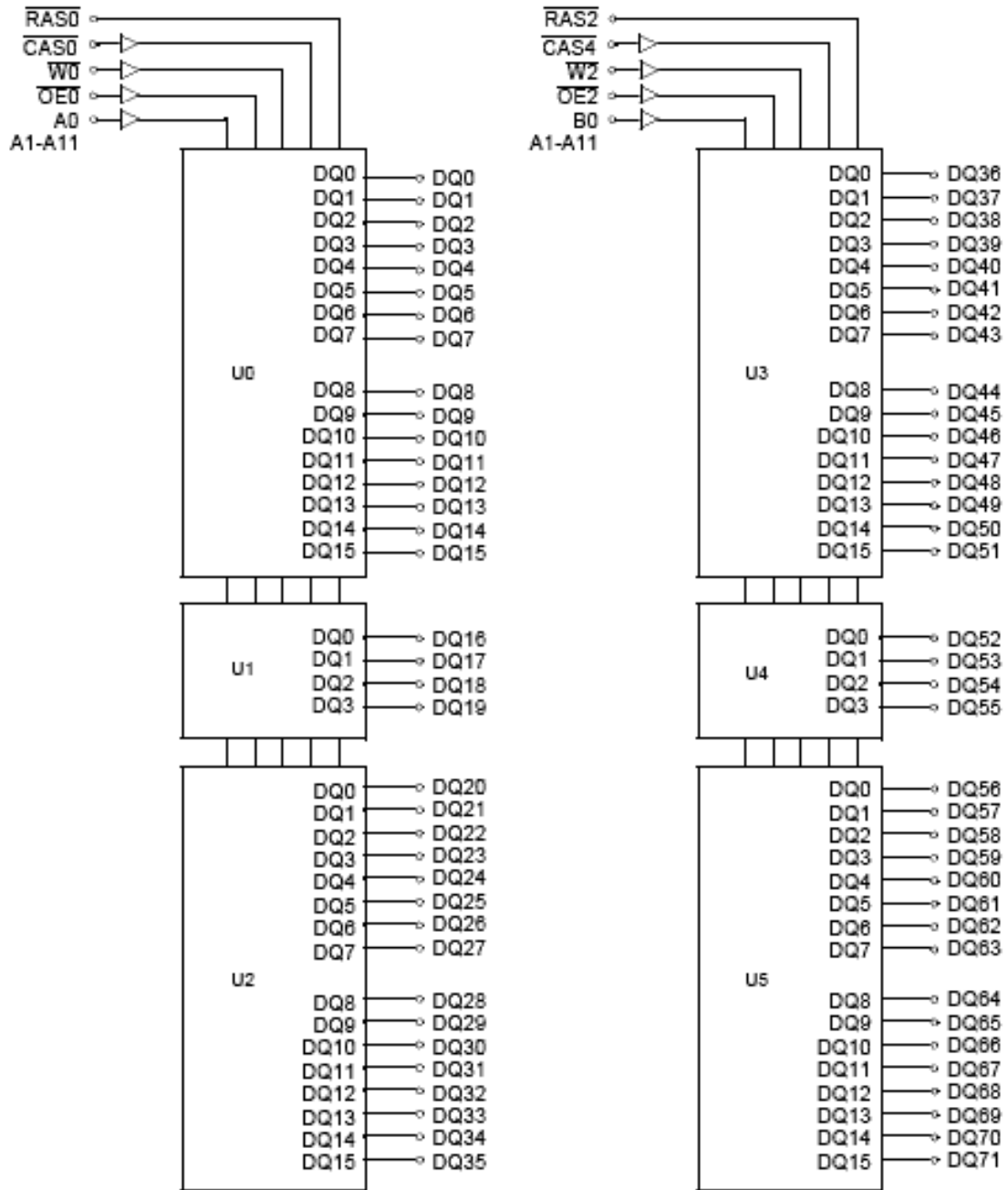
ID : 0 for V<sub>ss</sub> & 1 for N.C



# DRAM MODULE

# KMM372V404BS

## FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	VIN, VOUT	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +125	°C
Power Dissipation	PD	6	W
Short Circuit Output Current	Ios	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to VSS, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.0	-	Vcc+0.3*1	V
Input Low Voltage	VIL	-0.3*2	-	0.8	V

\*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.

\*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V404BS		Unit
		Min	Max	
Icc1	-5	-	660	mA
	-6	-	600	mA
Icc2	Don't care	-	100	mA
Icc3	-5	-	660	mA
	-6	-	600	mA
Icc4	-5	-	440	mA
	-6	-	380	mA
Icc5	Don't care	-	30	mA
Icc6	-5	-	660	mA
	-6	-	600	mA
II(L)	Don't care	-10	10	uA
IO(L)		-5	5	uA
VOH	Don't care	2.4	-	V
VOL		-	0.4	V

Icc1\* : Operating Current \* ( $\overline{RAS}$ ,  $\overline{CAS}$ , Address cycling @trc=min)

Icc2 : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

Icc3\* :  $\overline{RAS}$  Only Refresh Current \* ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$  cycling @trc=min)

Icc4\* : Fast Page Mode Current \* ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$  cycling : tPC=min)

Icc5 : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{cc}-0.2V$ )

Icc6\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current \* ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min)

II(L) : Input Leakage Current (Any input  $0 \leq V_{IN} \leq V_{cc}+0.3V$ , all other pins not under test=0 V)

IO(L) : Output Leakage Current(Data Out is disabled,  $0V \leq V_{OUT} \leq V_{cc}$ )

VOH : Output High Voltage Level (IOH = -2mA)

VOL : Output Low Voltage Level (IOL = 2mA)

\* **NOTE** : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In Icc4, address can be changed maximum once within one Fast Page mode cycle time, tPC.



# DRAM MODULE

# KMM372V404BS

## CAPACITANCE (TA = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	CIN1	-	20	pF
Input capacitance[W0, W2, OE0, OE2]	CIN2	-	20	pF
Input capacitance[RAS0, RAS2]	CIN3	-	31	pF
Input capacitance[CAS0, CAS4]	CIN4	-	20	pF
Input/Output capacitance[DQ0 - 71]	CDQ	-	17	pF

## AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	133		155		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		18		20	ns	3,4,5,11
Access time from column address	tAA		30		35	ns	3,10,11
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	5		5		ns	3,11
Output buffer turn-off delay	tOFF	5	18	5	20	ns	6,11
Transition time(rise and fall)	tT	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		ns	11
$\overline{\text{CAS}}$ hold time	tCSH	48		58		ns	11
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	18	32	18	40	ns	4,11
$\overline{\text{RAS}}$ to column address delay time	tRAD	13	20	13	25	ns	10,11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	10		10		ns	11
Row address set-up time	tASR	5		5		ns	11
Row address hold time	tRAH	8		8		ns	11
Column address set-up time	tASC	0		0		ns	12
Column address hold time	tCAH	10		10		ns	12
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		ns	11
Read command set-up time	tRCS	0		0		ns	
Read command hold referencde to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	-2		-2		ns	8,11
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	20		20		ns	11
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		ns	15
Data in set-up time	tDS	-2		-2		ns	9,11
Data in hold time	tDH	15		15		ns	9,11
Refresh period	tREF		64		64	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		ns	7,14
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		ns	7
$\overline{\text{CAS}}$ prechange to $\overline{\text{W}}$ delay time	tCPWD	53		60		ns	7



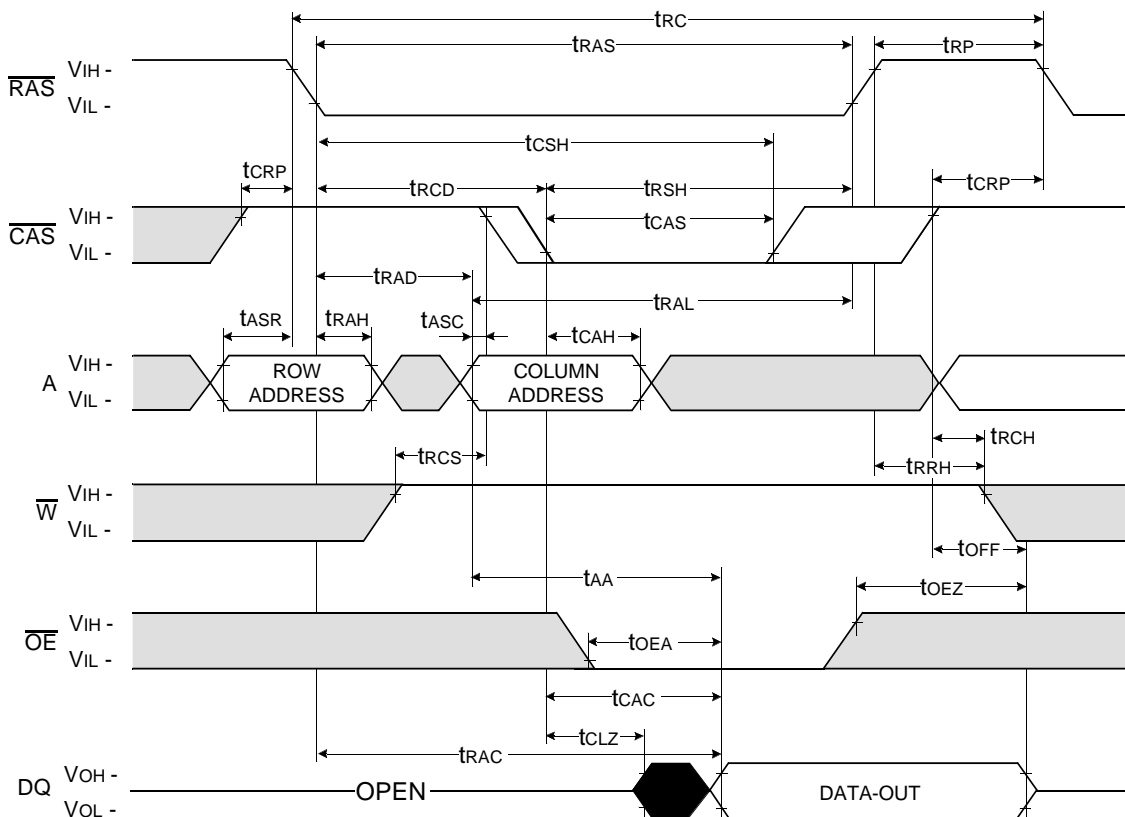
**AC CHARACTERISTICS** (0°C ≤ TA ≤ 70°C, VCC = 3.3V ± 0.3V. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRWD	71		83		ns	7,11
$\overline{\text{CAS}}$ setup time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		ns	11,16
$\overline{\text{CAS}}$ hold time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	8		8		ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	3		3		ns	11
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40	ns	3,11
Fast page mode cycle time	tPC	35		40		ns	
Fast page mode read-modify-write cycle time	tPRWC	76		85		ns	
$\overline{\text{CAS}}$ precharge time(Fast page cycle)	tCP	10		10		ns	13
$\overline{\text{RAS}}$ pulse width(Fast page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	tWRP	15		15		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)	tWRH	8		8		ns	11
$\overline{\text{OE}}$ access time	tOEA		18		20	ns	11
$\overline{\text{OE}}$ to data delay	tOED	18		20		ns	11
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	5	18	5	20	ns	11
$\overline{\text{OE}}$ command hold time	tOEH	13		15		ns	
<b>Present Detect Read Cycle</b>							
$\overline{\text{PDE}}$ to Valid PD bit	tPD		10		10	ns	
$\overline{\text{PDE}}$ to PD bit Inactive	tPDOFF	2	7	2	7	ns	

## NOTES

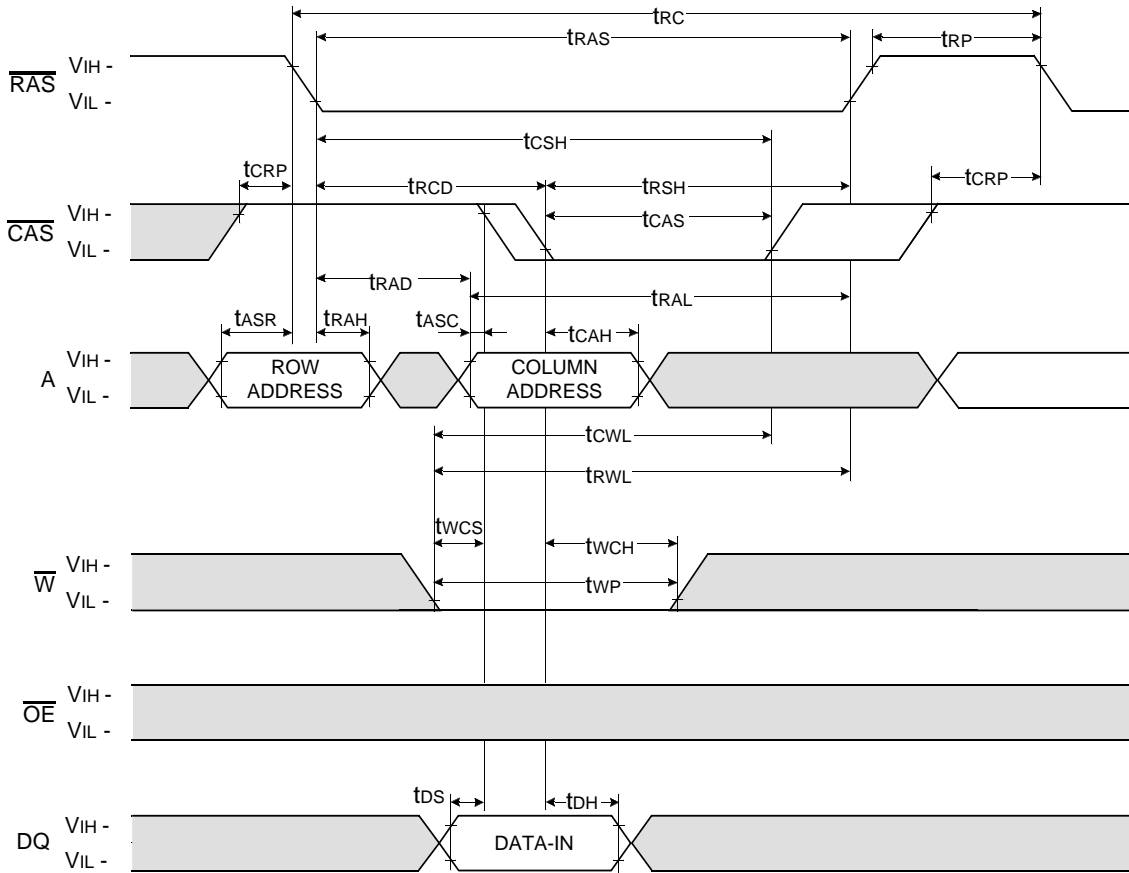
1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2. Input voltage levels are  $V_{ih}/V_{il}$ .  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPWD}}$  are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ . The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles.
10. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.
12.  $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$  are referenced to the earlier  $\overline{\text{CAS}}$  falling edge.
13.  $t_{\text{CP}}$  is specified from the last  $\overline{\text{CAS}}$  rising edge in the previous cycle to the first  $\overline{\text{CAS}}$  falling edge in the next cycle.
14.  $t_{\text{CWD}}$  is referenced to the later  $\overline{\text{CAS}}$  falling edge at word read-modify-write cycle.
15.  $t_{\text{CWL}}$  is specified from  $\overline{\text{W}}$  falling edge to the earlier  $\overline{\text{CAS}}$  rising edge.
16.  $t_{\text{CSR}}$  is referenced to earlier  $\overline{\text{CAS}}$  falling low before  $\overline{\text{RAS}}$  transition low.

READ CYCLE



WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

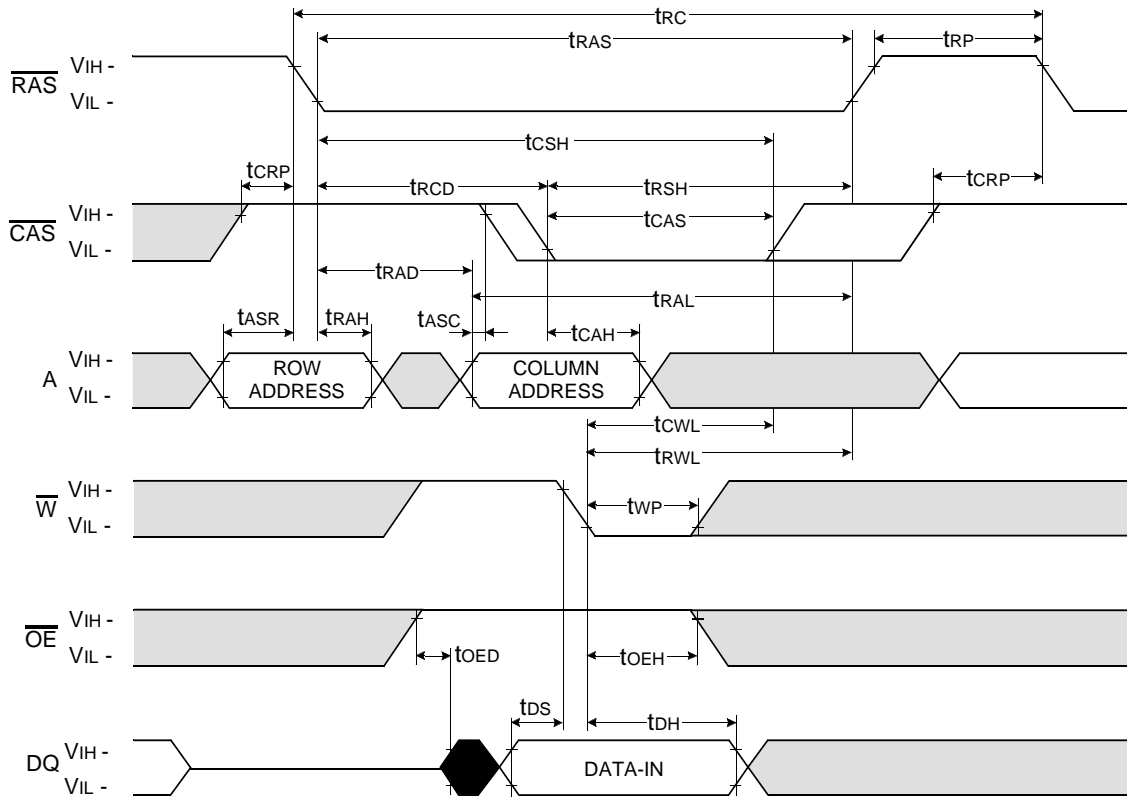


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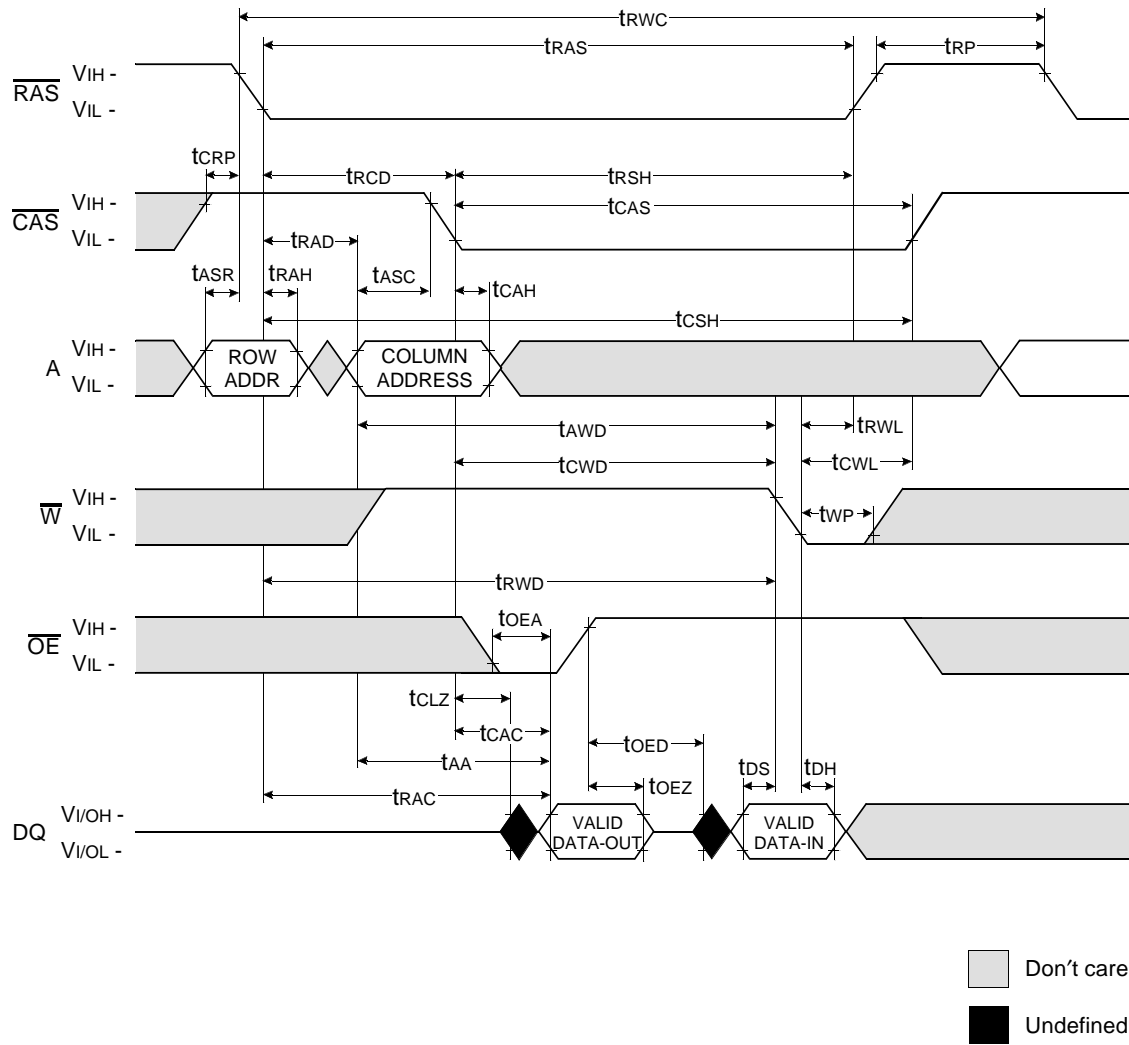
WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN



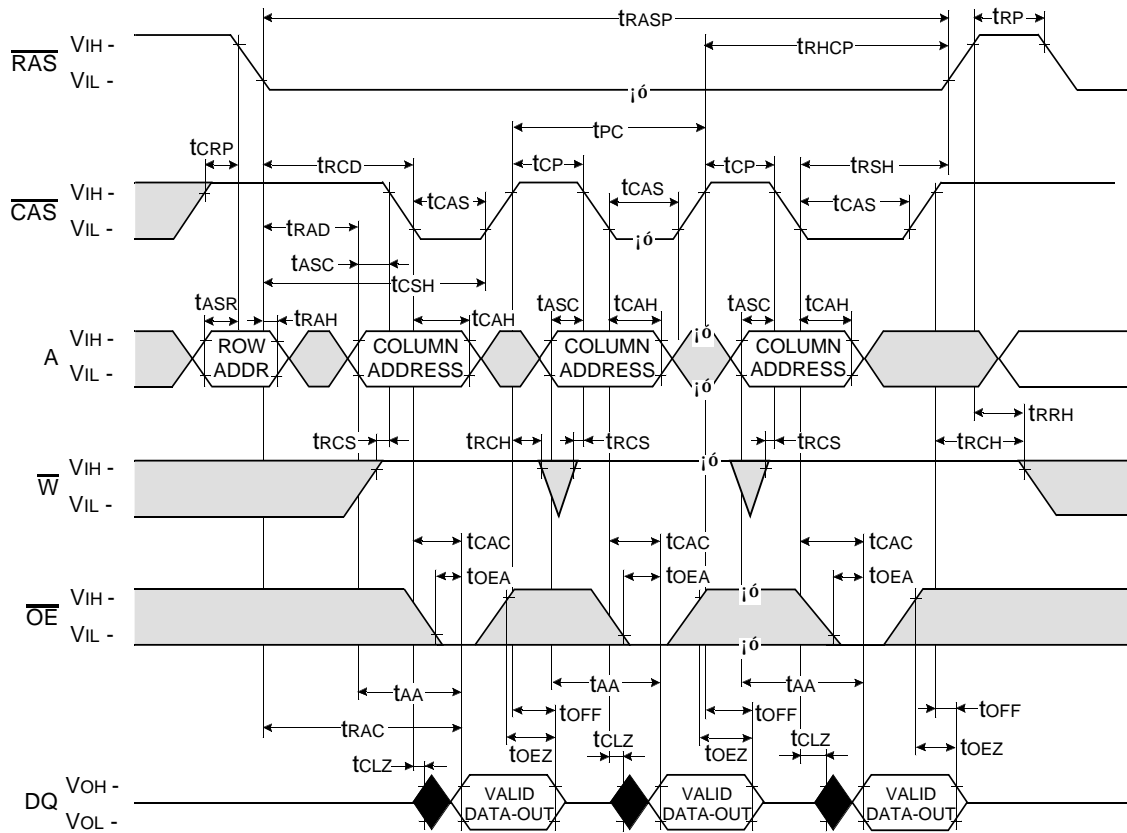
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READ - MODIFY - WRTIE CYCLE



FAST PAGE READ CYCLE

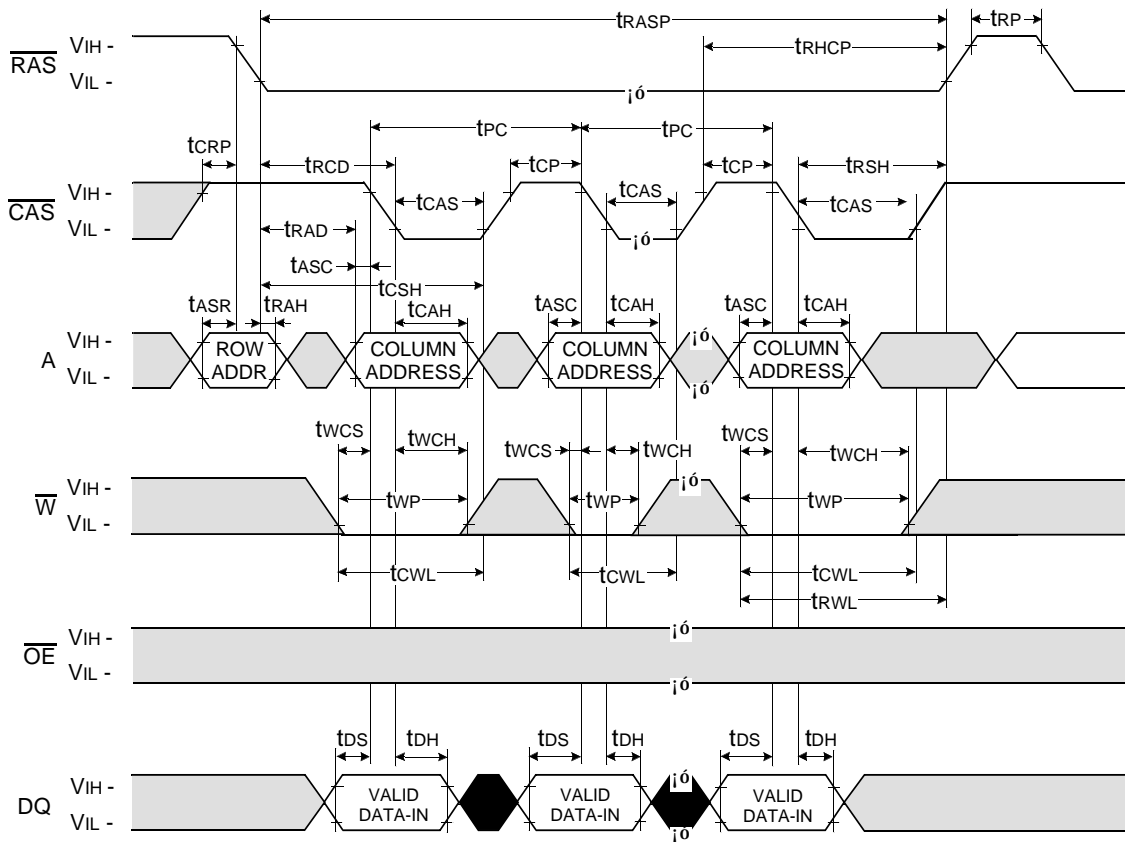
NOTE : DOUT = OPEN



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FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



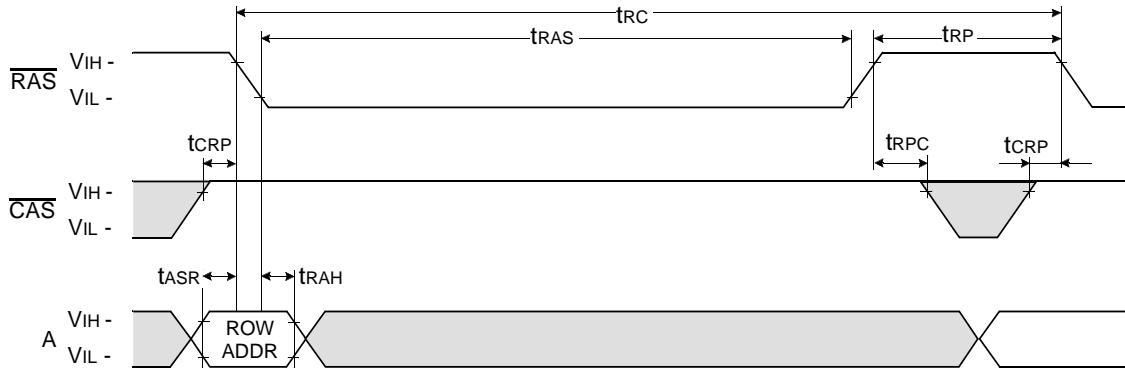
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**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE**

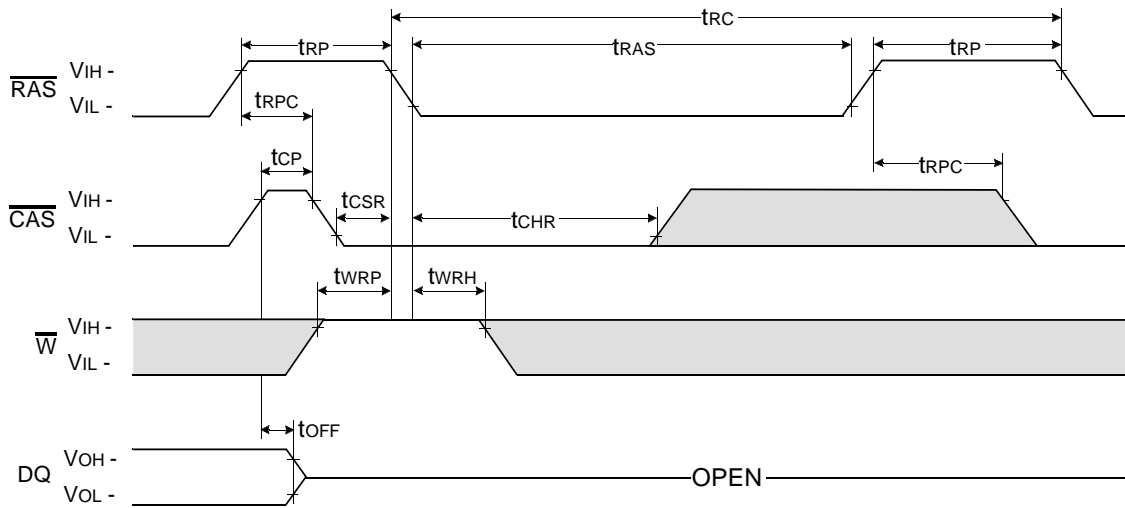
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ ,  $\text{DIN}$  = Don't care

$\text{DOUT}$  = OPEN



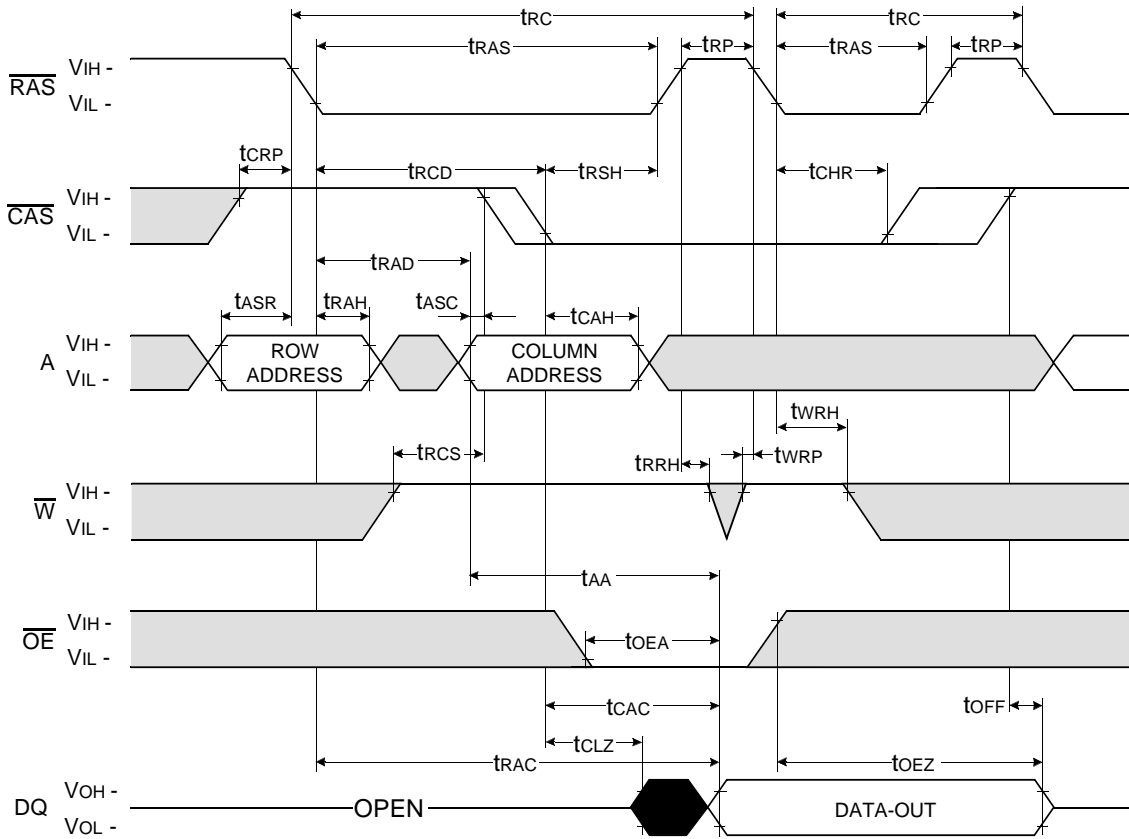
**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ ,  $\text{A}$  = Don't care



Don't care  
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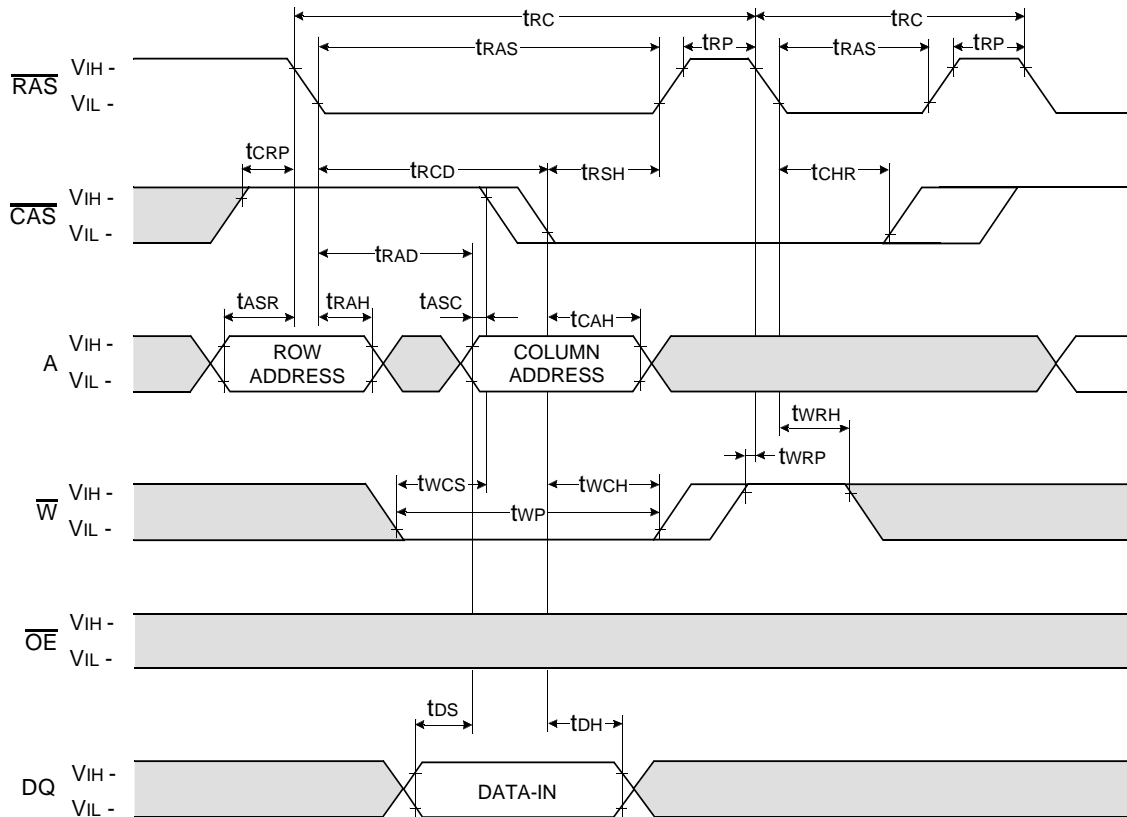
HIDDEN REFRESH CYCLE ( READ )



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**HIDDEN REFRESH CYCLE ( WRITE )**

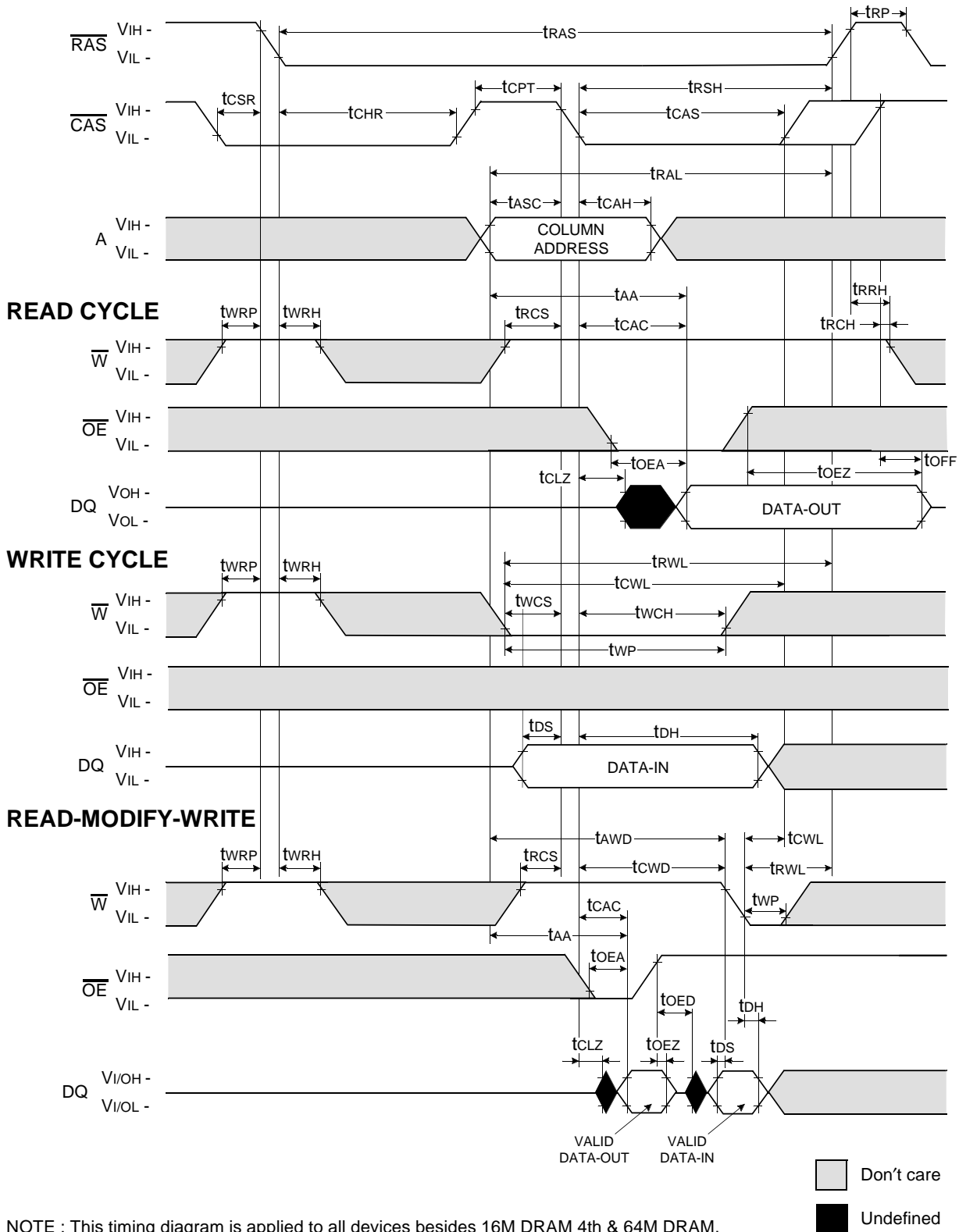
NOTE : DOUT = OPEN



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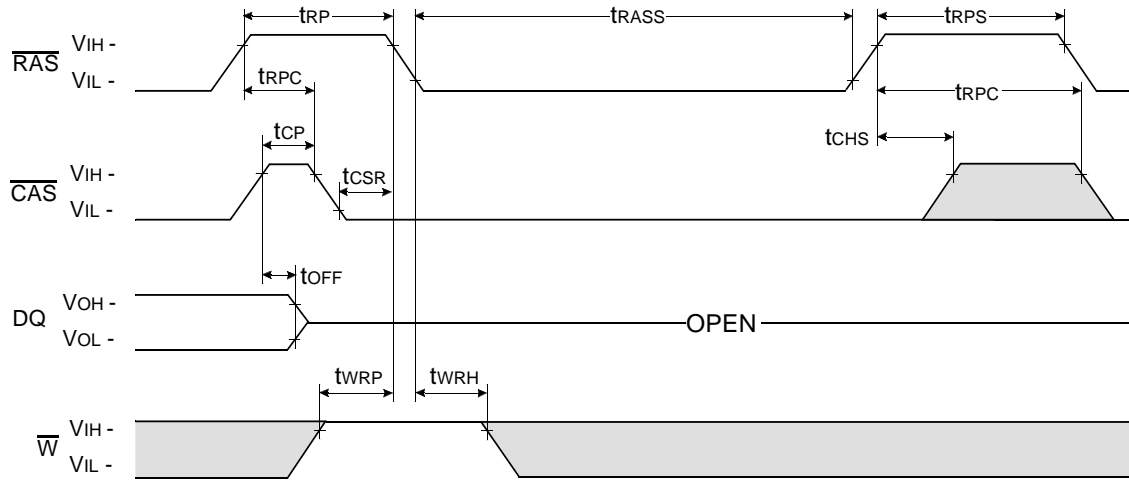
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

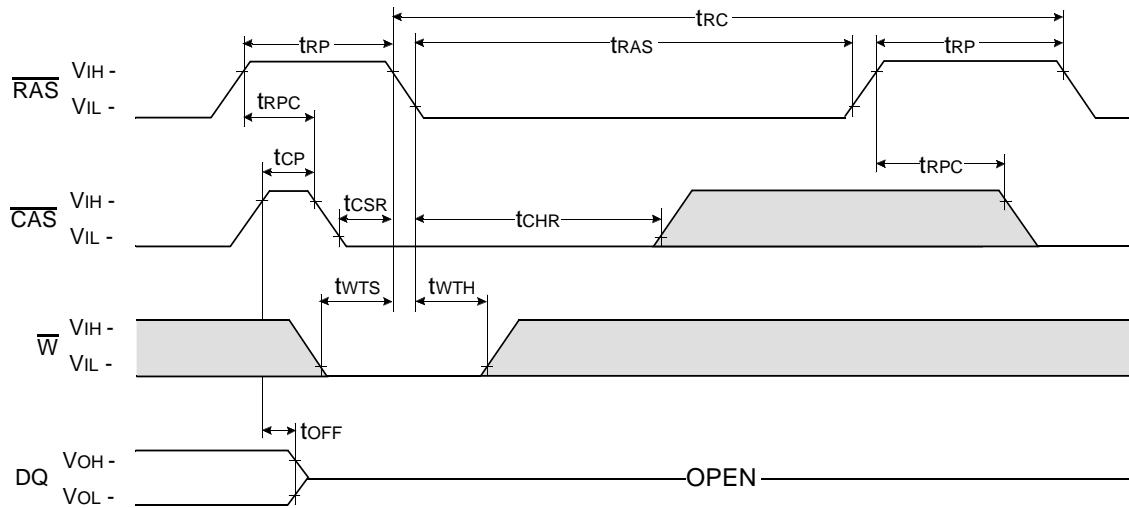
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



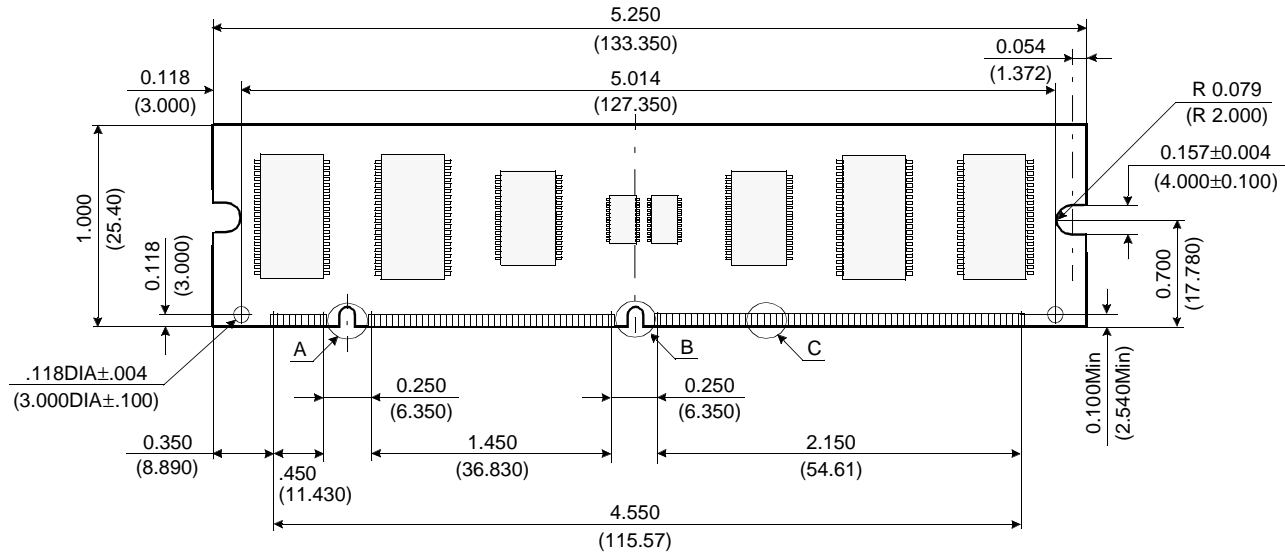
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# DRAM MODULE

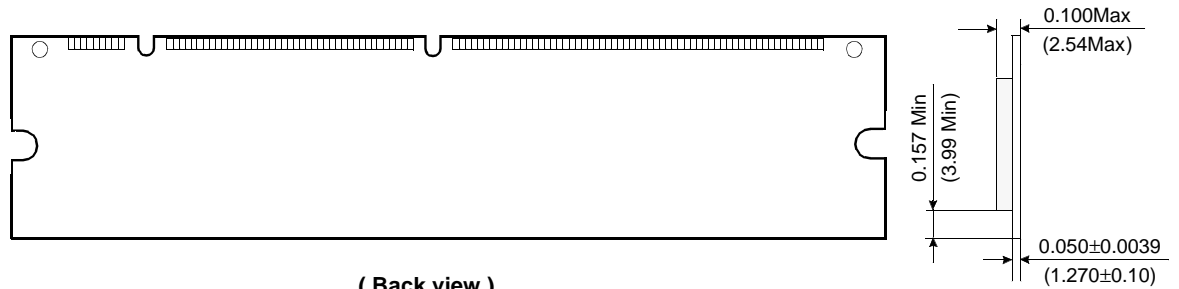
# KMM372V404BS

## PACKAGE DIMENSIONS

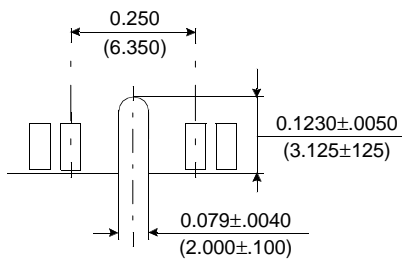
Units : Inches (millimeters)



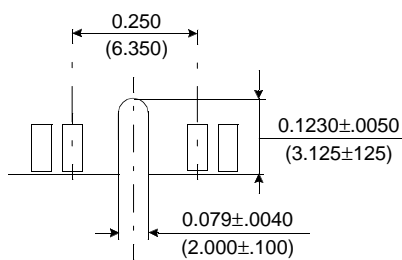
( Front view )



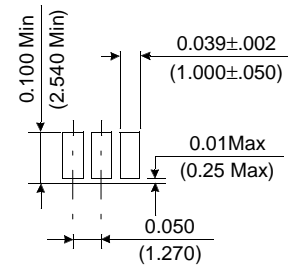
( Back view )



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with Fast Page mode, TSOP II.  
 DRAM Part No. : KMM372V404BS -KM416V4100BS & KM44V4000CS

