

KMM372F804BS EDO Mode

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F804B is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F804B consists of eight 4Mx16bits & four 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F804B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | tRAC | tCAC | tRC | tHFC |
|-------|------|------|-------|------|
| -5 | 50ns | 18ns | 84ns | 20ns |
| -6 | 60ns | 20ns | 104ns | 25ns |

FEATURES

- Part Identification
 - KMM372F804BS(4096cycles/64ms Ref. TSOP II)
- Extended Data Out Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{\text{RAS}}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | V _{ss} | 29 | *CAS2 | 57 | DQ22 | 85 | V _{ss} | 113 | *CAS3 | 141 | DQ58 |
| 2 | DQ0 | 30 | RAS0 | 58 | DQ23 | 86 | DQ36 | 114 | RAST | 142 | DQ59 |
| 3 | DQ1 | 31 | OE0 | 59 | V _{cc} | 87 | DQ37 | 115 | RFU | 143 | V _{cc} |
| 4 | DQ2 | 32 | V _{ss} | 60 | DQ24 | 88 | DQ38 | 116 | V _{ss} | 144 | DQ60 |
| 5 | DQ3 | 33 | A0 | 61 | RFU | 89 | DQ39 | 117 | A1 | 145 | RFU |
| 6 | V _{cc} | 34 | A2 | 62 | RFU | 90 | V _{cc} | 118 | A3 | 146 | RFU |
| 7 | DQ4 | 35 | A4 | 63 | RFU | 91 | DQ40 | 119 | A5 | 147 | RFU |
| 8 | DQ5 | 36 | A6 | 64 | RFU | 92 | DQ41 | 120 | A7 | 148 | RFU |
| 9 | DQ6 | 37 | A8 | 65 | DQ25 | 93 | DQ42 | 121 | A9 | 149 | DQ61 |
| 10 | DQ7 | 38 | A10 | 66 | DQ26 | 94 | DQ43 | 122 | A11 | 150 | DQ62 |
| 11 | DQ8 | 39 | A12 | 67 | DQ27 | 95 | DQ44 | 123 | *A13 | 151 | DQ63 |
| 12 | V _{ss} | 40 | V _{cc} | 68 | V _{ss} | 96 | V _{ss} | 124 | V _{cc} | 152 | V _{ss} |
| 13 | DQ9 | 41 | RFU | 69 | DQ28 | 97 | DQ45 | 125 | RFU | 153 | DQ64 |
| 14 | DQ10 | 42 | RFU | 70 | DQ29 | 98 | DQ46 | 126 | B0 | 154 | DQ65 |
| 15 | DQ11 | 43 | V _{ss} | 71 | DQ30 | 99 | DQ47 | 127 | V _{ss} | 155 | DQ66 |
| 16 | DQ12 | 44 | OE2 | 72 | DQ31 | 100 | DQ48 | 128 | RFU | 156 | DQ67 |
| 17 | DQ13 | 45 | RAS2 | 73 | V _{cc} | 101 | DQ49 | 129 | RAS3 | 157 | V _{cc} |
| 18 | V _{cc} | 46 | CAS4 | 74 | DQ32 | 102 | V _{cc} | 130 | CAS5 | 158 | DQ68 |
| 19 | DQ14 | 47 | *CAS6 | 75 | DQ33 | 103 | DQ50 | 131 | *CAS7 | 159 | DQ69 |
| 20 | DQ15 | 48 | W2 | 76 | DQ34 | 104 | DQ51 | 132 | PDE | 160 | DQ70 |
| 21 | DQ16 | 49 | V _{cc} | 77 | DQ35 | 105 | DQ52 | 133 | V _{cc} | 161 | DQ71 |
| 22 | DQ17 | 50 | RSVD | 78 | V _{ss} | 106 | DQ53 | 134 | RSVD | 162 | V _{ss} |
| 23 | V _{ss} | 51 | RSVD | 79 | PD1 | 107 | V _{ss} | 135 | RSVD | 163 | PD2 |
| 24 | RSVD | 52 | DQ18 | 80 | PD3 | 108 | RSVD | 136 | DQ54 | 164 | PD4 |
| 25 | RSVD | 53 | DQ19 | 81 | PD5 | 109 | RSVD | 137 | DQ55 | 165 | PD6 |
| 26 | V _{cc} | 54 | V _{ss} | 82 | PD7 | 110 | V _{cc} | 138 | V _{ss} | 166 | PD8 |
| 27 | W0 | 55 | DQ20 | 83 | ID0 | 111 | RFU | 139 | DQ56 | 167 | ID1 |
| 28 | CAS0 | 56 | DQ21 | 84 | V _{cc} | 112 | CAS1 | 140 | DQ57 | 168 | V _{cc} |

PIN NAMES

| Pin Names | Function |
|------------------|-------------------------|
| A0, B0, A1 - A11 | Address Input(4K ref.) |
| DQ0 - DQ71 | Data In/Out |
| W0, W2 | Read/Write Enable |
| OE0, OE2 | Output Enable |
| RAS0 - RAS3 | Row Address Strobe |
| CAS0, 1,4,5 | Column Address Strobe |
| V _{cc} | Power(+3.3V) |
| V _{ss} | Ground |
| NC | No Connection |
| PDE | Presence Detect Enable |
| PD1 - 8 | Presence Detect |
| ID0 - 1 | ID bit |
| RSVD | Reserved Use |
| RFU | Reserved for Future Use |

Pins marked "*" are not used in this module.

PD & ID Table

| Pin | 50NS | 60NS |
|-----|------|------|
| PD1 | 0 | 0 |
| PD2 | 0 | 0 |
| PD3 | 1 | 1 |
| PD4 | 1 | 1 |
| PD5 | 1 | 1 |
| PD6 | 0 | 1 |
| PD7 | 0 | 1 |
| PD8 | 0 | 0 |
| ID0 | 0 | 0 |
| ID1 | 0 | 0 |

PD Note :PD & ID Terminals must each be pulled up through a register to V_{cc} at the next higher level assembly. PDs will be either open (NC) or driven to V_{ss} via on-board buffer circuits.
 ID Note : IDs will be either open (NC) or connected directly to V_{ss} without a buffer.

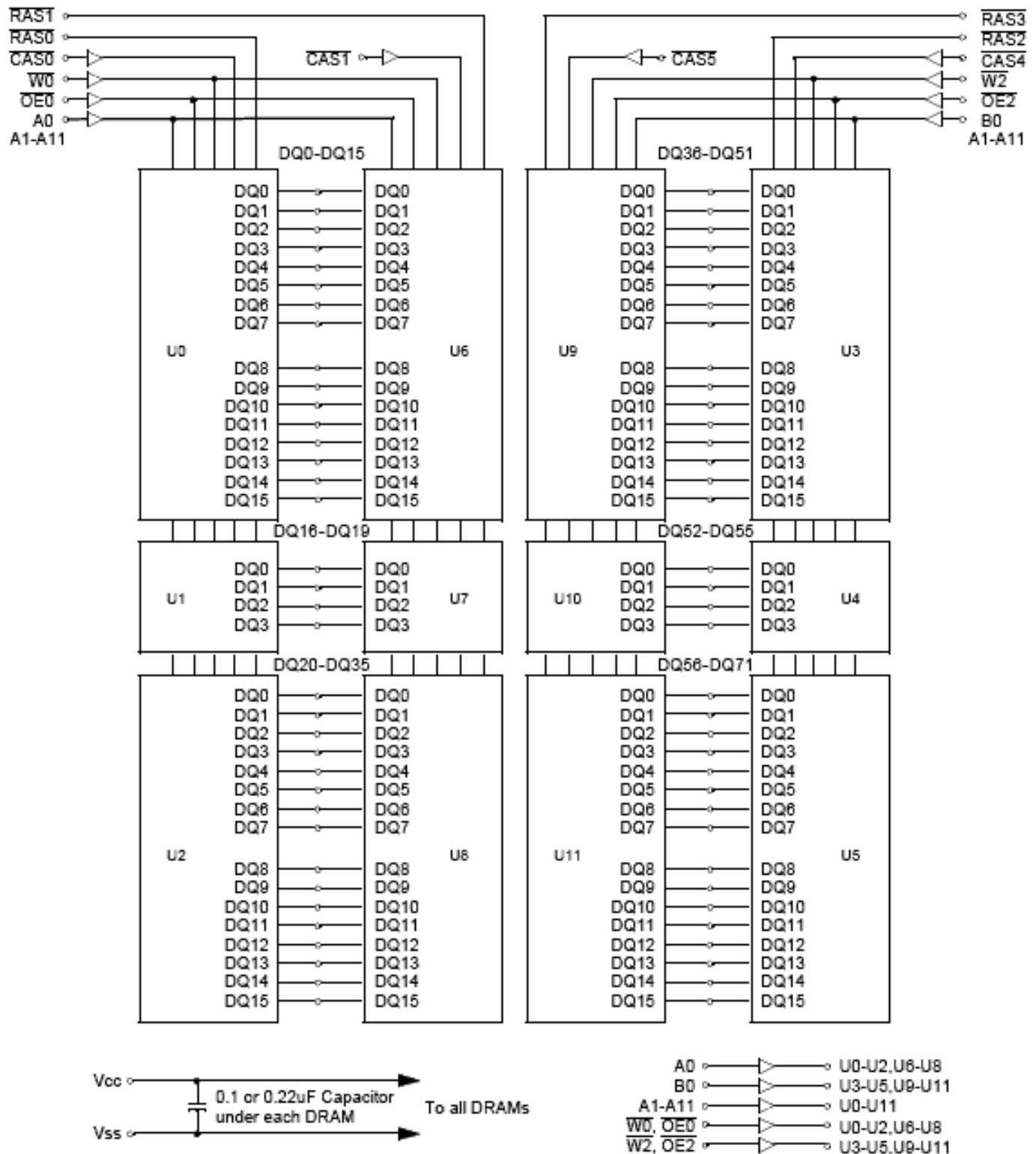
PD : 0 for Vol of Drive IC & 1 for N.C
 ID : 0 for V_{ss} & 1 for N.C



DRAM MODULE

KMM372F804BS

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|-----------|--------------|------|
| Voltage on any pin relative Vss | VIN, VOUT | -0.5 to +4.6 | V |
| Voltage on Vcc supply relative to Vss | VCC | -0.5 to +4.6 | V |
| Storage Temperature | Tstg | -55 to +125 | °C |
| Power Dissipation | PD | 12 | W |
| Short Circuit Output Current | Ios | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to VSS, TA = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|--------|--------|-----|-----------|------|
| Supply Voltage | VCC | 3.0 | 3.3 | 3.6 | V |
| Ground | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.0 | - | VCC+0.3*1 | V |
| Input Low Voltage | VIL | -0.3*2 | - | 0.8 | V |

*1 : VCC+1.3V at pulse width≤15ns, which is measured at VCC.

*2 : -1.3V at pulse width≤15ns, which is measured at VSS.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | KMM372F804BS | | Unit |
|--------|------------|--------------|-----|------|
| | | Min | Max | |
| Icc1 | -5 | - | 760 | mA |
| | -6 | - | 700 | mA |
| Icc2 | Don't care | - | 100 | mA |
| Icc3 | -5 | - | 760 | mA |
| | -6 | - | 700 | mA |
| Icc4 | -5 | - | 700 | mA |
| | -6 | - | 640 | mA |
| Icc5 | Don't care | - | 30 | mA |
| Icc6 | -5 | - | 760 | mA |
| | -6 | - | 700 | mA |
| II(L) | Don't care | -10 | 10 | uA |
| IO(L) | | -10 | 10 | uA |
| VOH | Don't care | 2.4 | - | V |
| VOL | | - | 0.4 | V |

Icc1* : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

Icc2 : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

Icc3* : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

Icc4* : Extended Data Out Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : tHPC=min)

Icc5 : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

Icc6* : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I(IL) : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.3V$, all other pins not under test=0 V)

I(OL) : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

VOH : Output High Voltage Level (IOH = -2mA)

VOL : Output Low Voltage Level (IOL = 2mA)

* **NOTE** : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In Icc4, address can be changed maximum once within one EDO mode cycle time, tHPC.



DRAM MODULE

KMM372F804BS

CAPACITANCE (TA = 25°C, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|-------------------------------------|--------|-----|-----|------|
| Input capacitance[A0, B0, A1 - A11] | CIN1 | - | 20 | pF |
| Input capacitance[W0, W2, OE0, OE2] | CIN2 | - | 20 | pF |
| Input capacitance[RAS0 - RAS3] | CIN3 | - | 31 | pF |
| Input capacitance[CAS0, 1,4,5] | CIN4 | - | 20 | pF |
| Input/Output capacitance[DQ0 - 71] | CDQ | - | 24 | pF |

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|---|--------|-----|-----|-----|-----|------|----------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 84 | | 104 | | ns | |
| Read-modify-write cycle time | tRWC | 128 | | 153 | | ns | |
| Access time from $\overline{\text{RAS}}$ | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from $\overline{\text{CAS}}$ | tCAC | | 18 | | 20 | ns | 3,4,5,13 |
| Access time from column address | tAA | | 30 | | 35 | ns | 3,10,13 |
| $\overline{\text{CAS}}$ to output in Low-Z | tCLZ | 8 | | 8 | | ns | 3,13 |
| $\overline{\text{OE}}$ to output in Low-Z | tOLZ | 8 | | 8 | | ns | 3,13 |
| Output buffer turn-off delay from $\overline{\text{CAS}}$ | tCEZ | 8 | 18 | 8 | 18 | ns | 6,11,13 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| $\overline{\text{RAS}}$ precharge time | tRP | 30 | | 40 | | ns | |
| $\overline{\text{RAS}}$ pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| $\overline{\text{RAS}}$ hold time | tRSH | 13 | | 15 | | ns | 13 |
| $\overline{\text{CAS}}$ hold time | tCSH | 36 | | 38 | | ns | 13 |
| $\overline{\text{CAS}}$ pulse width | tCAS | 8 | 10K | 10 | 10K | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | tRCD | 15 | 32 | 18 | 40 | ns | 4,13 |
| $\overline{\text{RAS}}$ to column address delay time | tRAD | 10 | 20 | 13 | 25 | ns | 10,13 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | tCRP | 10 | | 10 | | ns | 13 |
| Row address set-up time | tASR | 5 | | 5 | | ns | 13 |
| Row address hold time | tRAH | 5 | | 8 | | ns | 13 |
| Column address set-up time | tASC | 0 | | 0 | | ns | 14 |
| Column address hold time | tCAH | 7 | | 10 | | ns | 14 |
| Column address to $\overline{\text{RAS}}$ lead time | tRAL | 30 | | 35 | | ns | 13 |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to $\overline{\text{CAS}}$ | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to $\overline{\text{RAS}}$ | tRRH | -2 | | -2 | | ns | 8,13 |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| Write command hold time | tWCH | 7 | | 10 | | ns | |
| Write command pulse width | tWP | 7 | | 10 | | ns | |
| Write command to $\overline{\text{RAS}}$ lead time | tRWL | 13 | | 15 | | ns | 13 |
| Write command to $\overline{\text{CAS}}$ lead time | tCWL | 7 | | 10 | | ns | 17 |
| Data set-up time | tDS | -2 | | -2 | | ns | 9,13 |
| Data hold time | tDH | 13 | | 15 | | ns | 9,13 |
| Refresh period | tREF | | 64 | | 64 | ms | |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time | tCWD | 33 | | 38 | | ns | 7,16 |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time | tRWD | 68 | | 82 | | ns | 7,13 |



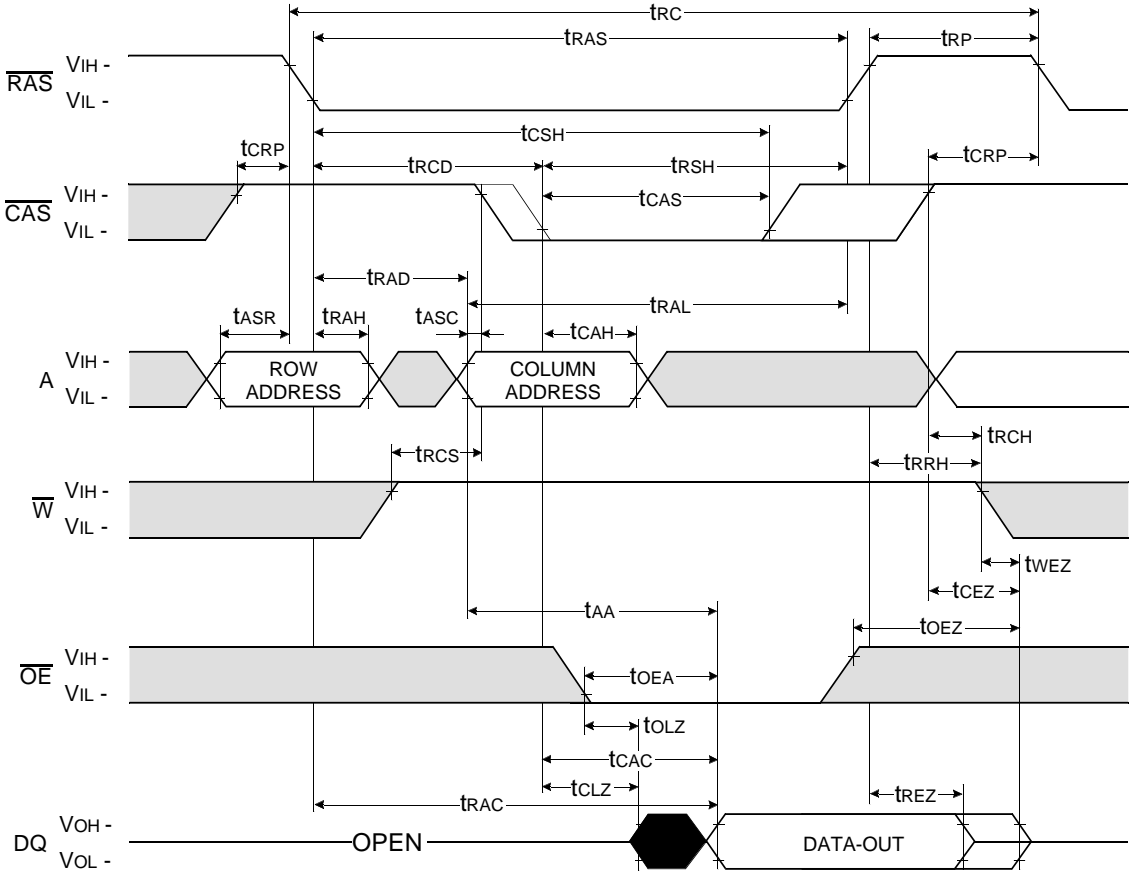
AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3V ± 0.3V. See notes 1,2.)

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|--|---------------------|-----|------|-----|------|------|-------|
| | | Min | Max | Min | Max | | |
| Column address to \overline{W} delay time | t _{AWD} | 45 | | 53 | | ns | 7 |
| \overline{CAS} precharge time to \overline{W} delay time | t _{CPWD} | 47 | | 58 | | ns | |
| \overline{CAS} setup time(\overline{CAS} -before- \overline{RAS} refresh) | t _{CSR} | 10 | | 10 | | ns | 13,18 |
| \overline{CAS} hold time(\overline{CAS} -before- \overline{RAS} refresh) | t _{CHR} | 8 | | 8 | | ns | 13 |
| \overline{RAS} to \overline{CAS} precharge time | t _{RPC} | 3 | | 3 | | ns | 13 |
| Access time from \overline{CAS} precharge | t _{CPA} | | 33 | | 40 | ns | 3,13 |
| Hyper page cycle time | t _{HPC} | 20 | | 25 | | ns | 12 |
| Hyper page read-modify-write cycle time | t _{HPRWC} | 70 | | 77 | | ns | 12 |
| \overline{CAS} precharge time(Hyper page cycle) | t _{CP} | 7 | | 10 | | ns | 15 |
| \overline{RAS} pulse width (Hyper page cycle) | t _{RASP} | 50 | 200K | 60 | 200K | ns | |
| \overline{RAS} hold time from \overline{CAS} precharge | t _{RHCP} | 35 | | 40 | | ns | 13 |
| \overline{W} to \overline{RAS} precharge time(C-B-R refresh) | t _{WRP} | 15 | | 15 | | ns | 13 |
| \overline{W} to \overline{RAS} hold time(C-B-R refresh) | t _{WRH} | 8 | | 8 | | ns | 13 |
| \overline{OE} access time | t _{OEA} | | 18 | | 20 | ns | 13 |
| \overline{OE} to data delay | t _{OED} | 15 | | 18 | | ns | 13 |
| Output buffer turn off delay time from \overline{OE} | t _{OEZ} | 8 | 18 | 8 | 18 | ns | 13 |
| \overline{OE} command hold time | t _{OEH} | 5 | | 5 | | ns | |
| Output data hold time(\overline{C} -B- \overline{R} refresh) | t _{DOH} | 10 | | 10 | | ns | 13 |
| Output buffer turn off delay time from \overline{RAS} | t _{REZ} | 3 | 13 | 3 | 13 | ns | 6,11 |
| Output buffer turn off delay time from \overline{W} | t _{WEZ} | 8 | 18 | 8 | 18 | ns | 6,13 |
| \overline{W} to data delay | t _{WED} | 20 | | 20 | | ns | 13 |
| \overline{OE} to \overline{CAS} hold time | t _{OCH} | 5 | | 5 | | ns | |
| \overline{CAS} hold time to \overline{OE} | t _{CHO} | 5 | | 5 | | ns | |
| \overline{OE} precharge time | t _{OEP} | 5 | | 5 | | ns | |
| \overline{W} pulse width (Hyper page cycle) | t _{WPE} | 5 | | 5 | | ns | |
| Present Detect Read Cycle | | | | | | | |
| \overline{PDE} to Valid PD bit | t _{PD} | | 10 | | 10 | ns | |
| \overline{PDE} to PD bit Inactive | t _{PD OFF} | 2 | 7 | 2 | 7 | ns | |

NOTES

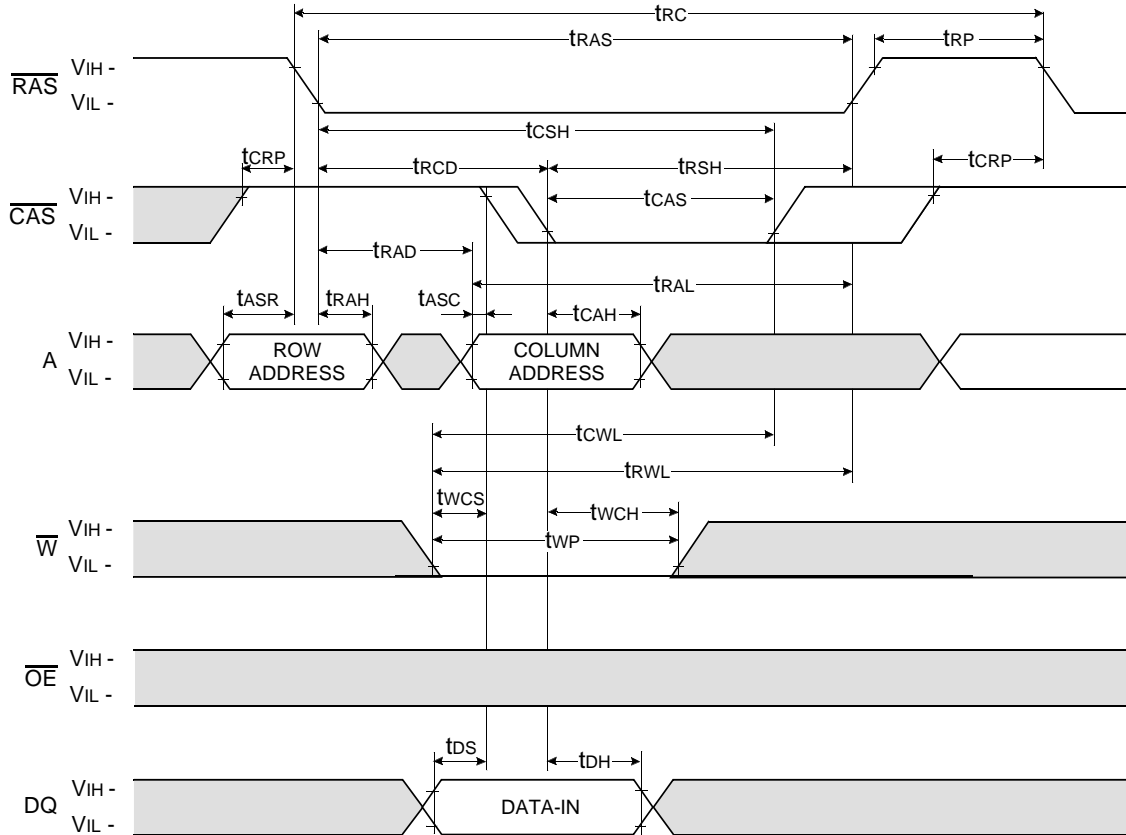
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWd} , t_{CWd} , t_{AWd} and t_{CPWd} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{\text{RWd}} \geq t_{\text{RWd}}(\text{min})$, $t_{\text{CWd}} \geq t_{\text{CWd}}(\text{min})$, $t_{\text{AWd}} \geq t_{\text{AWd}}(\text{min})$ and $t_{\text{CPWd}} \geq t_{\text{CPWd}}(\text{min})$. The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
12. $t_{\text{ASC}} \geq 6\text{ns}$.
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.
14. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
15. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
16. t_{CWd} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
17. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
18. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

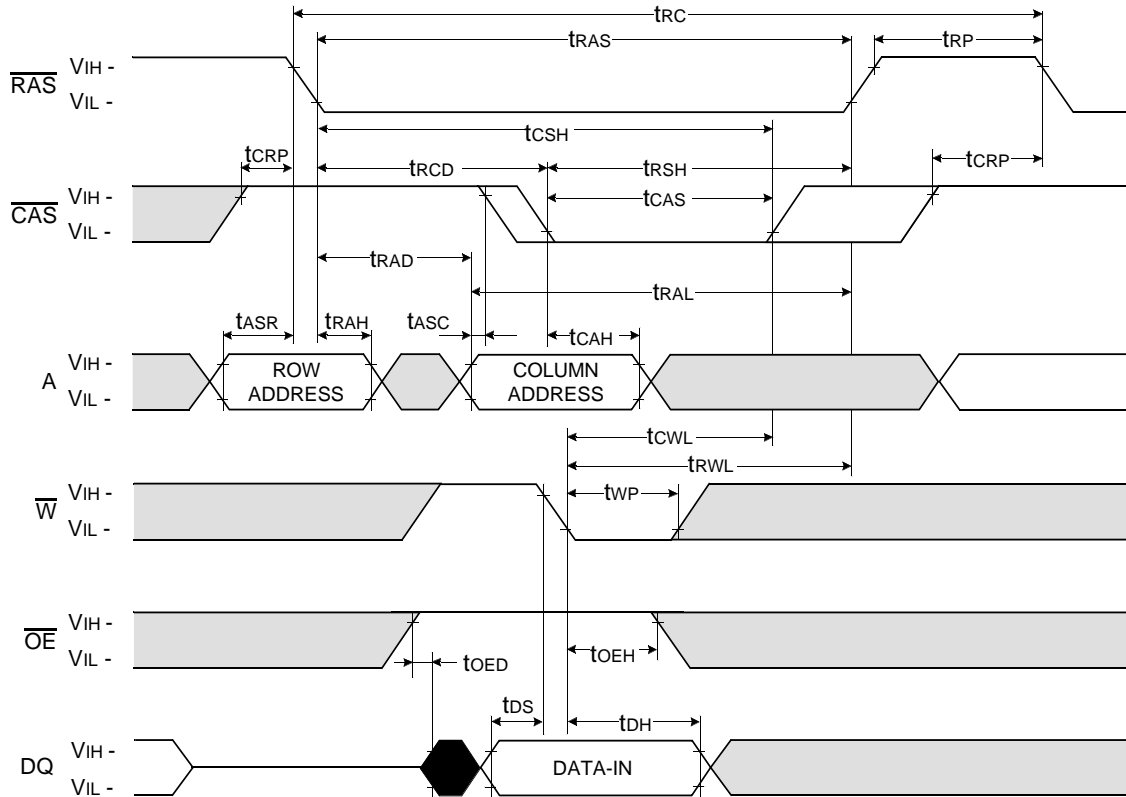
NOTE : DOUT = OPEN



Don't care
 Undefined

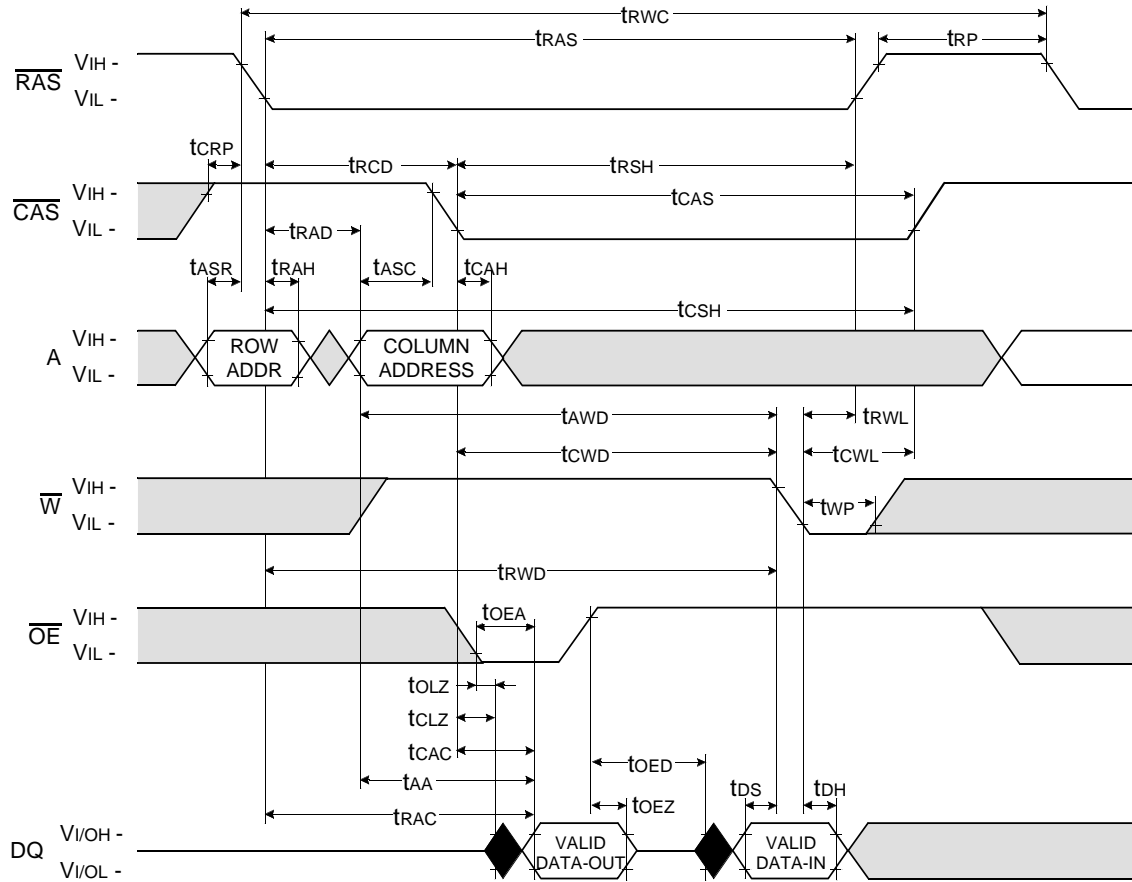
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN

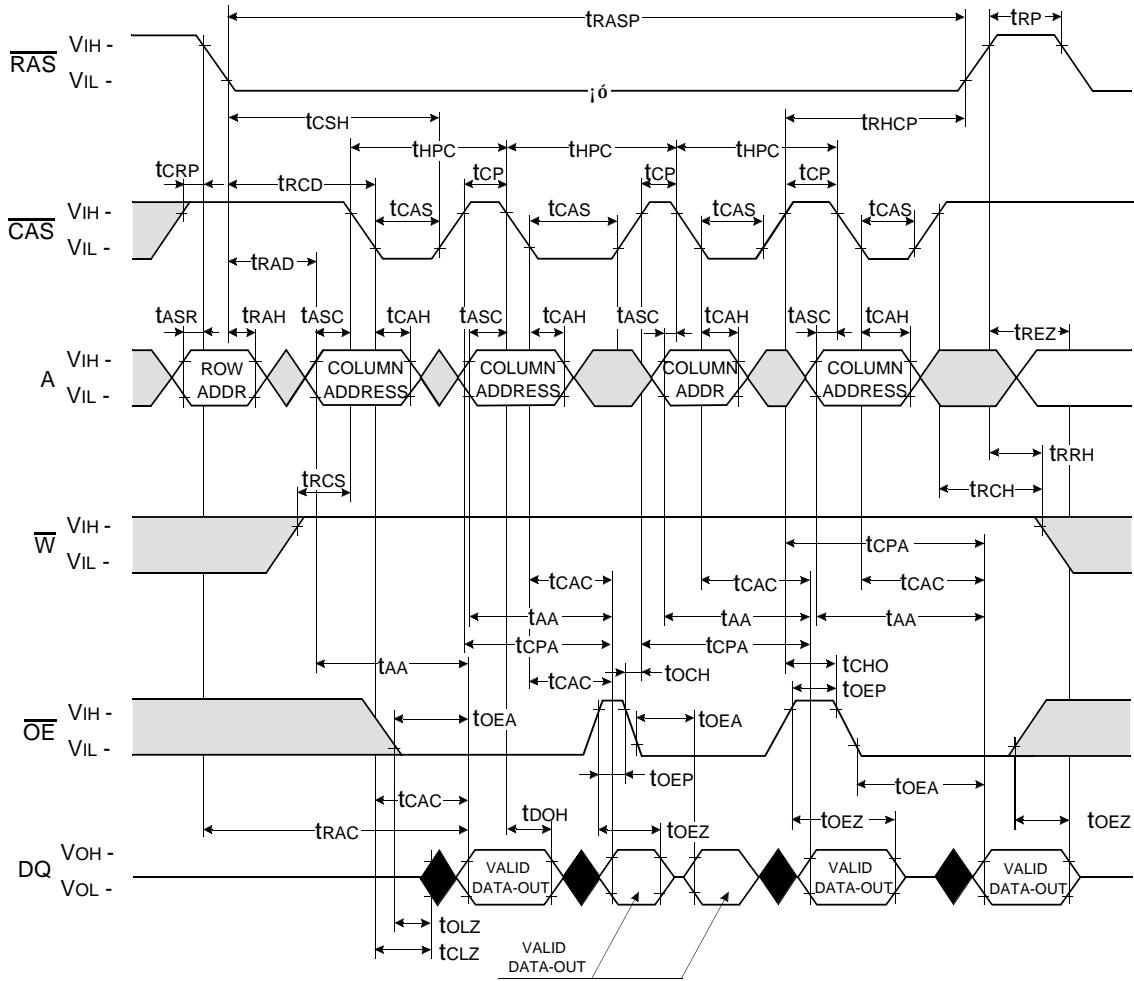


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READ - MODIFY - WRITE CYCLE



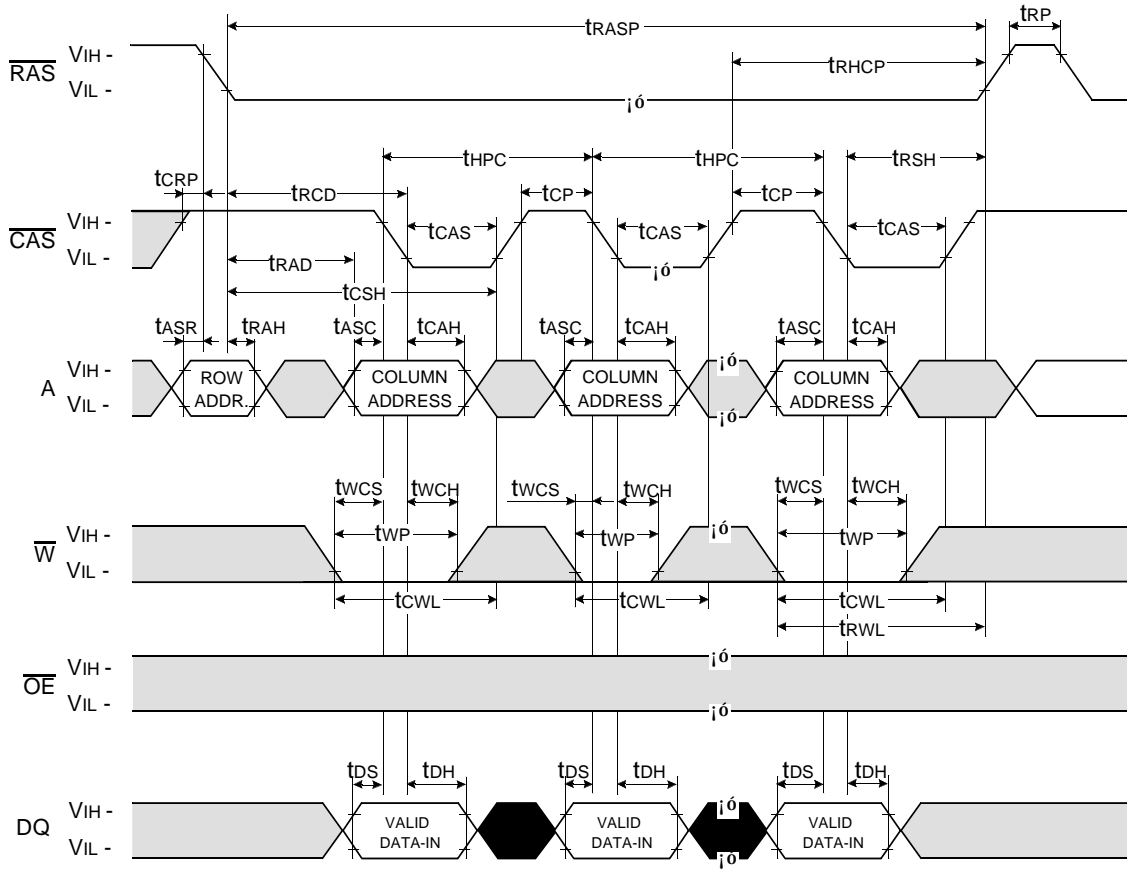
HYPER PAGE READ CYCLE



Don't care
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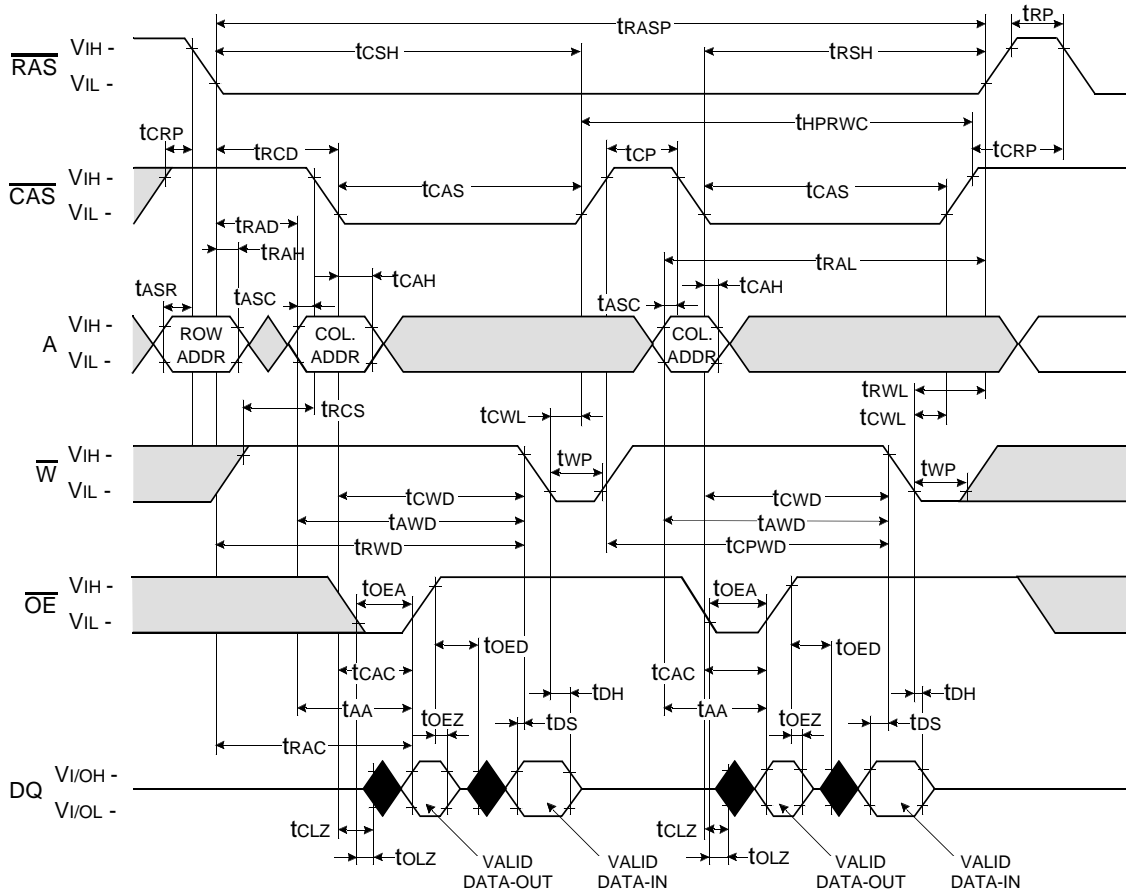
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



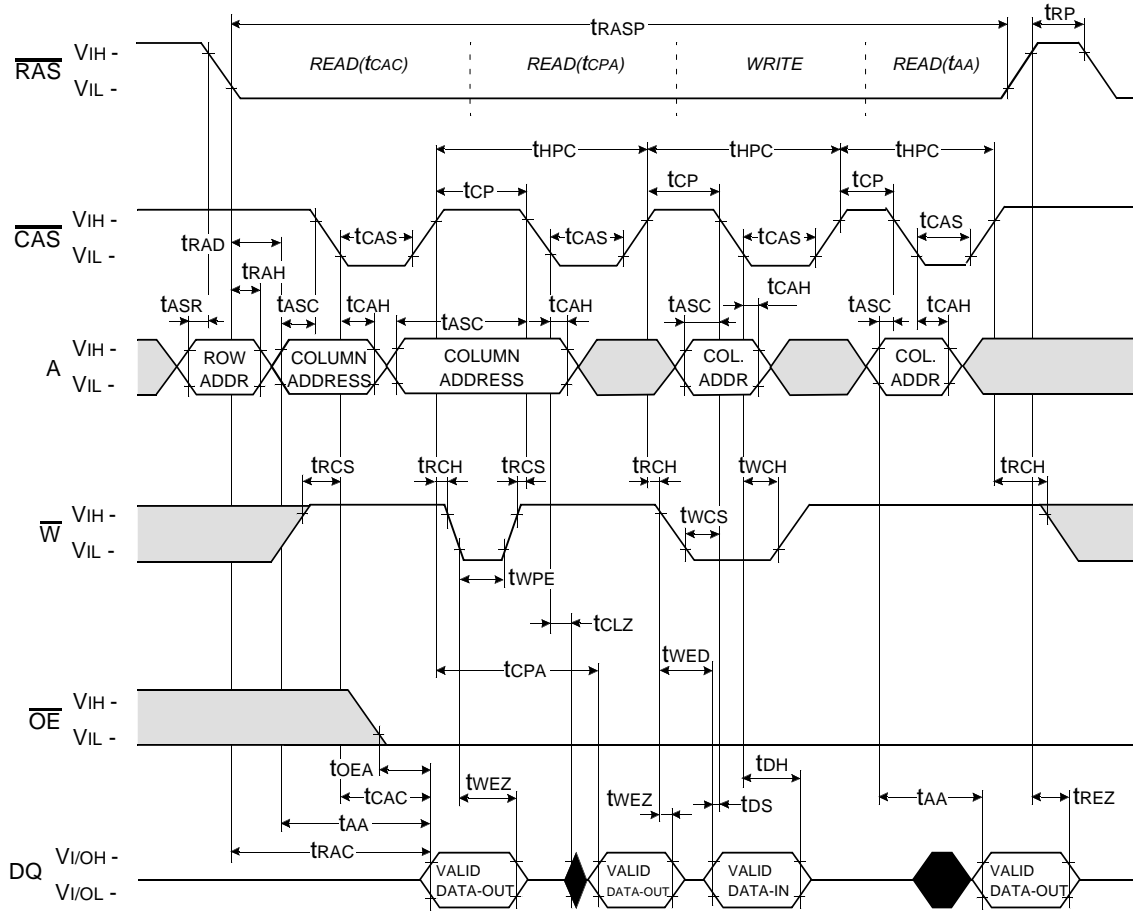
Don't care
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HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
 Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

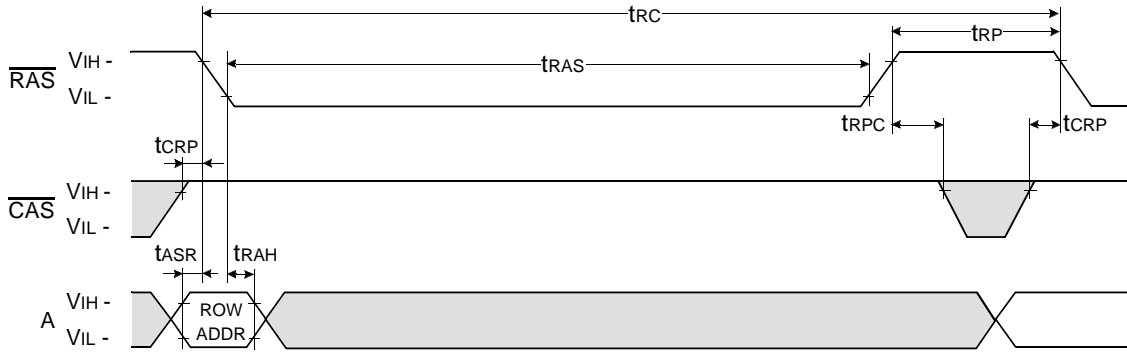


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RAS - ONLY REFRESH CYCLE*

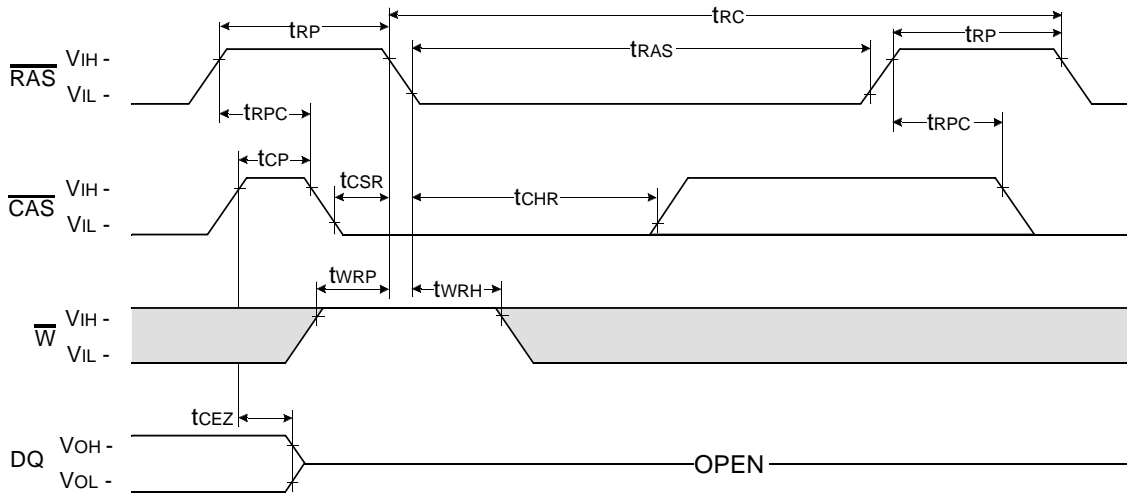
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

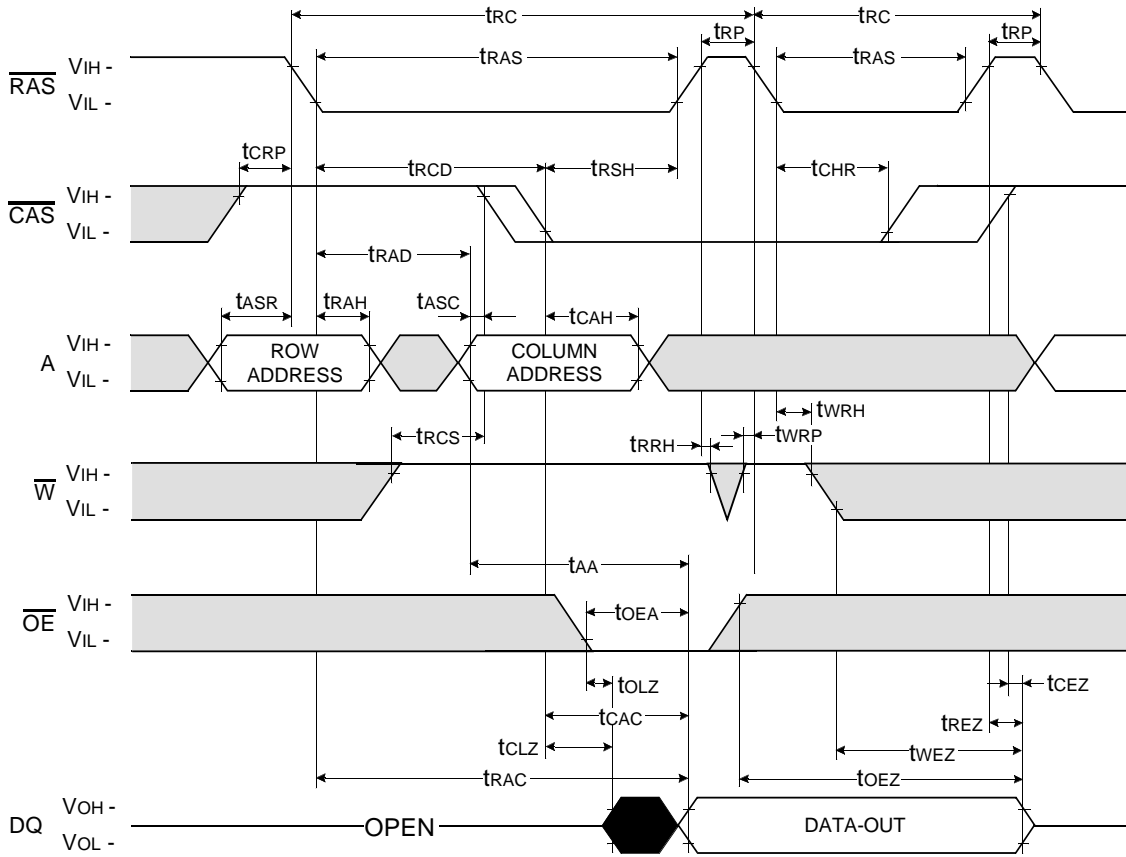
NOTE : \overline{OE} , A = Don't care



Don't care
 Undefined

* In RAS-only refresh cycle of 64Mb A-die & B-die, when \overline{CAS} signal transits from Low to High, the valid data may be cut off.

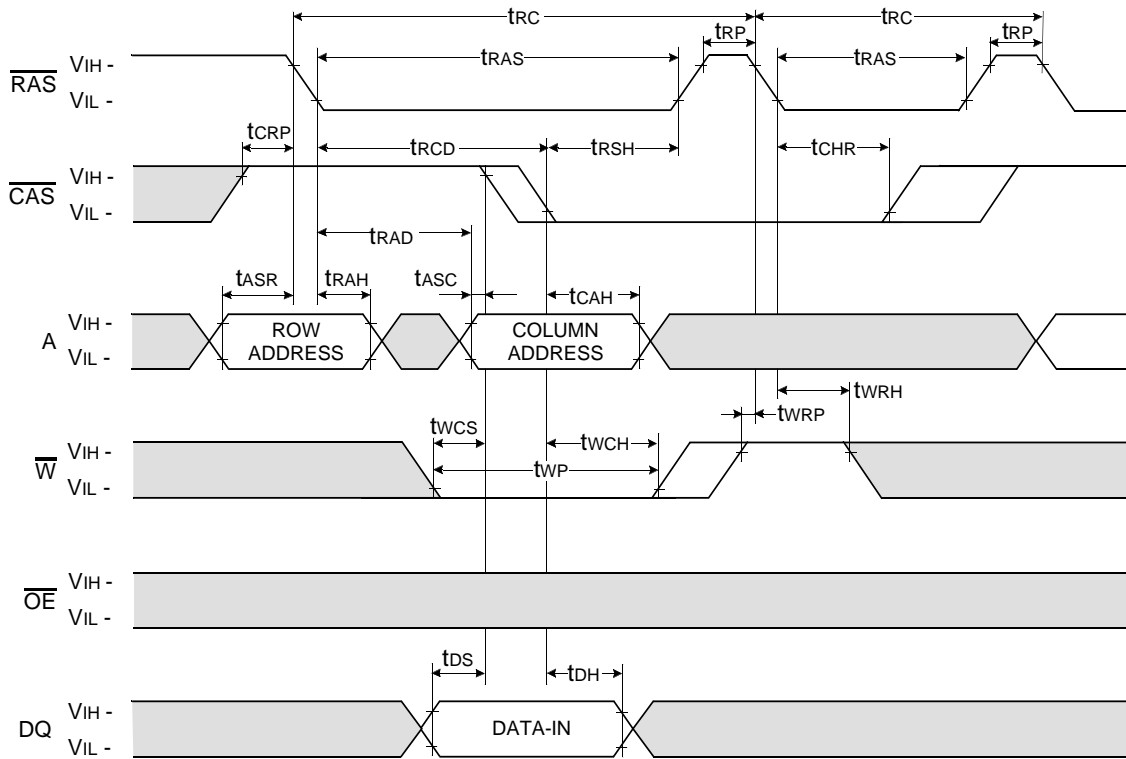
HIDDEN REFRESH CYCLE (READ)



Don't care
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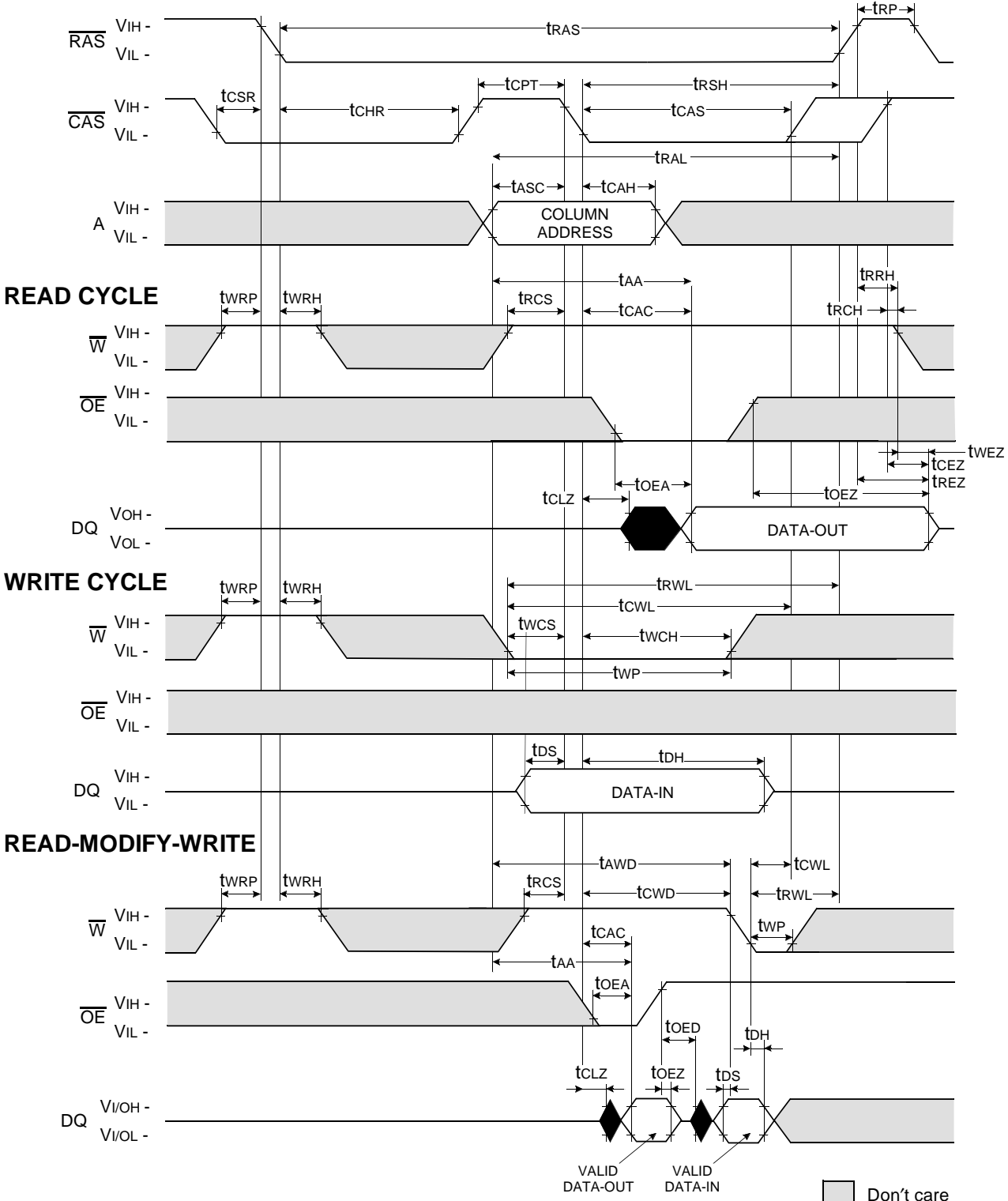
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

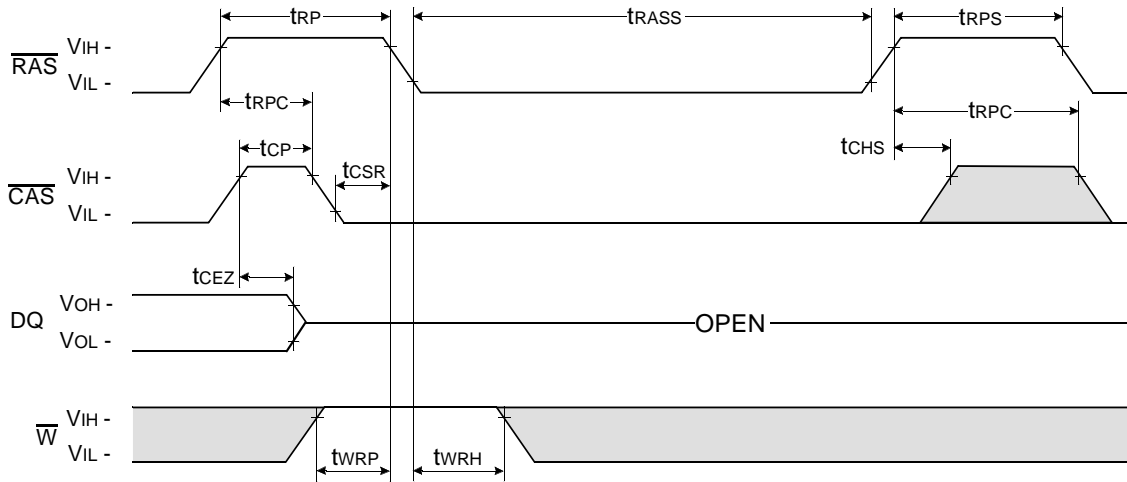
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

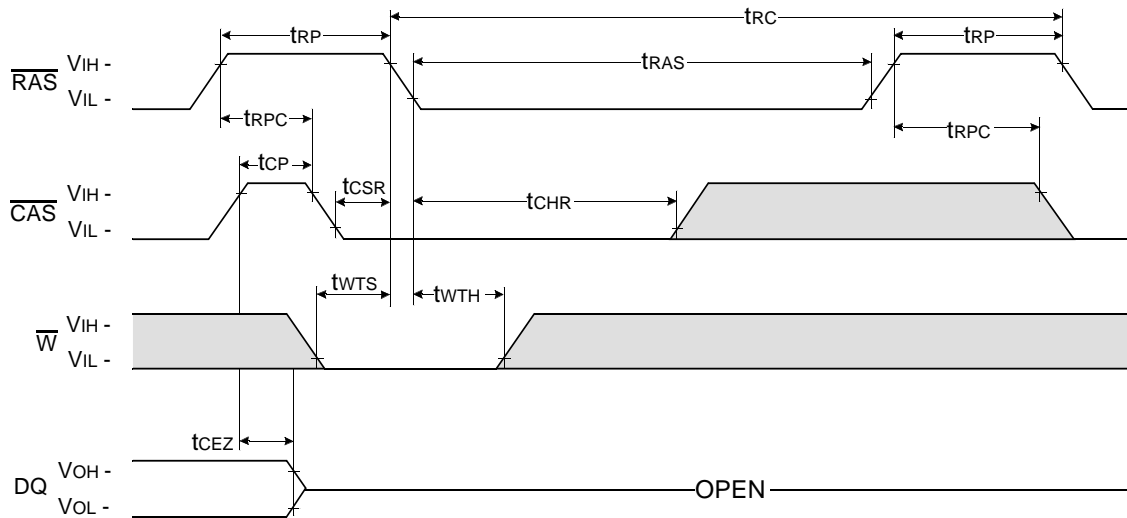
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



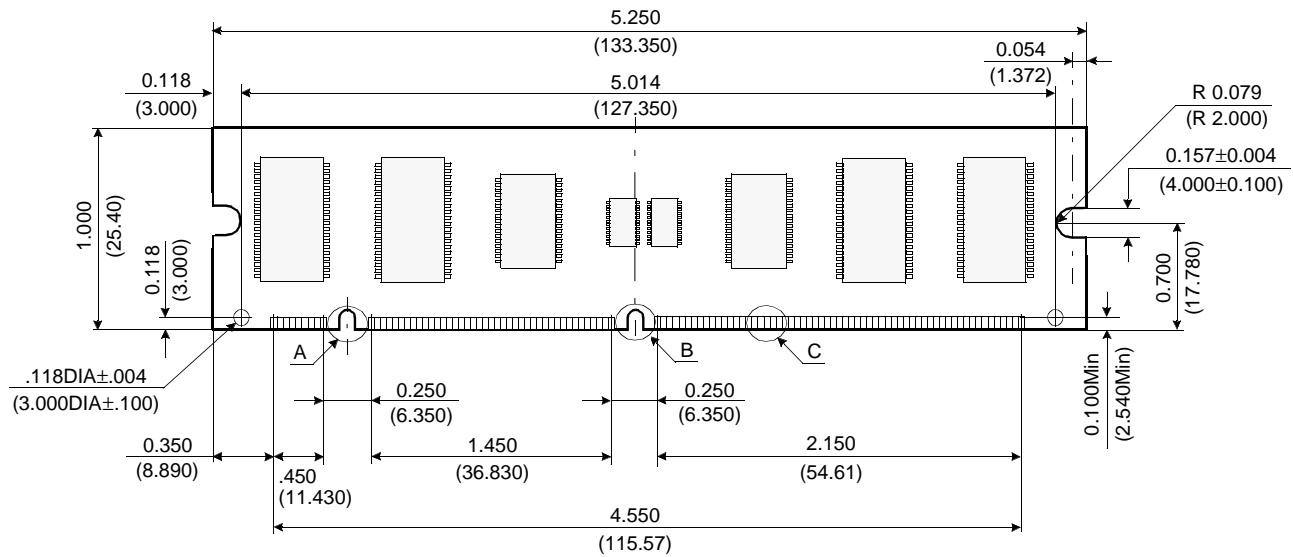
Don't care
 Undefined

DRAM MODULE

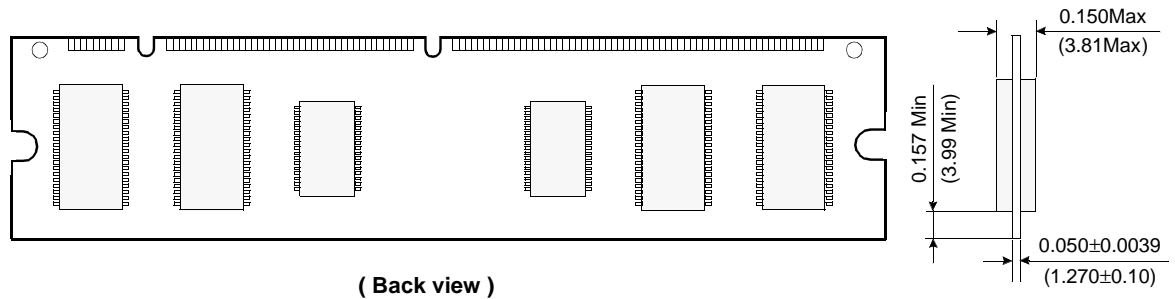
KMM372F804BS

PACKAGE DIMENSIONS

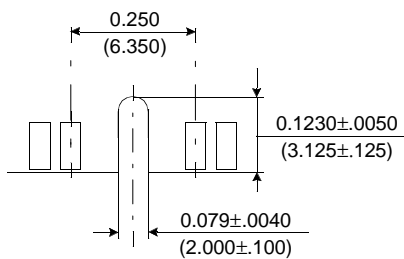
Units : Inches (millimeters)



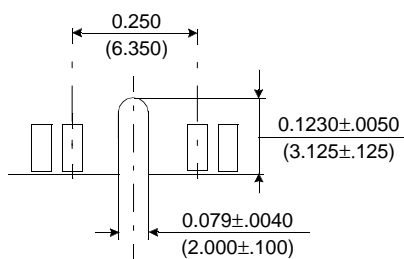
(Front view)



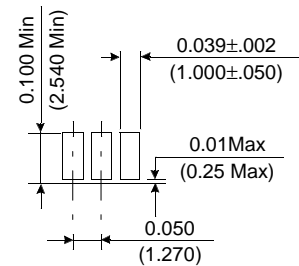
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372F804BS -KM416V4104BS & KM44V4004CS

