

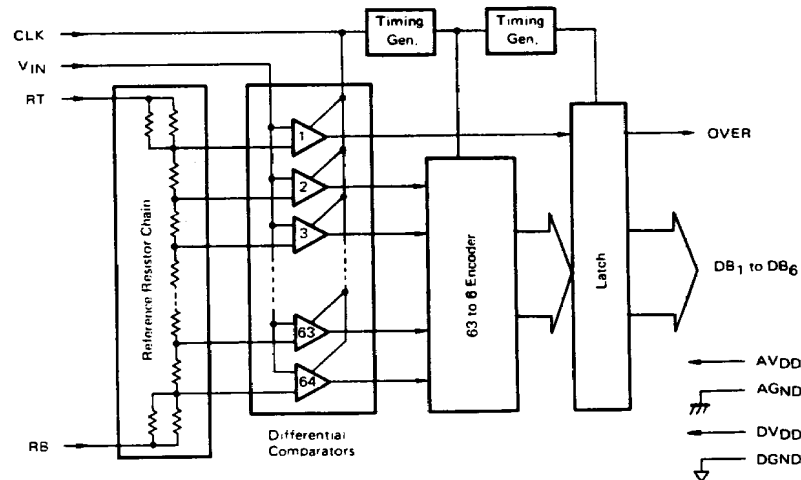
**6 BIT D/A CONVERTER FOR VIDEO SIGNAL PROCESSING**  
**CMOS LSI**

The  $\mu$ PD6951 is an 6 bit A/D converter designed for use in video applications. The high-speed CMOS processing technology and full-parallel conversion technics adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msp/s can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and high-speed facsimile.

**FEATURES**

- Resolution : 6 bits
- Conversion rate : 20 Msp/s
- Linearity :  $\pm 0.5$  LSB MAX.
- Reference voltage : 2.5 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (125 mW TYP.)
- TTL compatible (Digital output)
- 18 pin plastic DIP, and 20 pin plastic SOP (375 mil)

**BLOCK DIAGRAM**



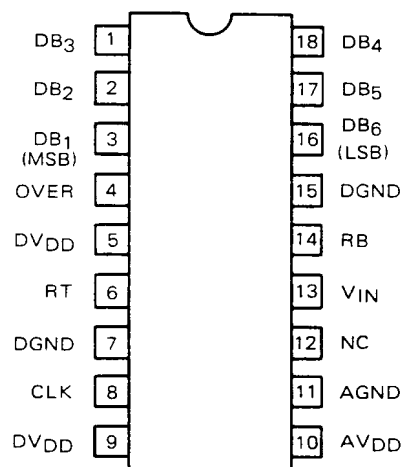
**ORDERING INFORMATION**

Ordering Name	Package
$\mu$ PD6951C	18 pin plastic DIP (300 mil)
$\mu$ PD6951G	20 pin plastic SOP (375 mil)

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The \* mark outside the columns denotes major points where revisions or additions are made in this edition.

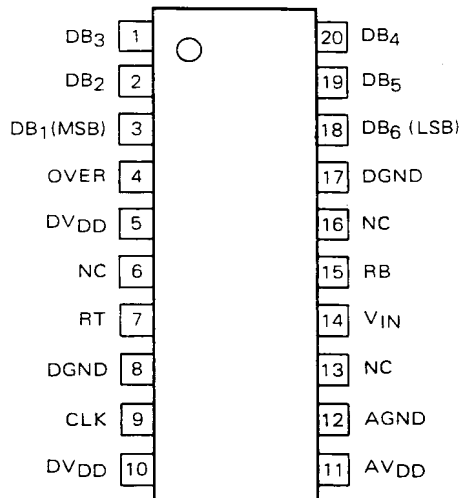
CONNECTION DIAGRAM (Top View)

μPD6951C



- 1 DB<sub>3</sub> Digital output (3rd)
- 2 DB<sub>2</sub> Digital output (2nd)
- 3 DB<sub>1</sub> Digital output (MSB)
- 4 OVER Over range
- 5 DV<sub>DD</sub> Digital power supply
- 6 RT Reference voltage (high voltage side)
- 7 DGND Digital GND
- 8 CLK Clock input
- 9 DV<sub>DD</sub> Digital power supply
- 10 AV<sub>DD</sub> Analog power supply
- 11 AGND Analog GND
- 12 NC No connection
- 13 V<sub>IN</sub> Analog input
- 14 RB Reference voltage (low level side)
- 15 DGND Digital GND
- 16 DB<sub>6</sub> Digital input (LSB)
- 17 DB<sub>5</sub> Digital input (5th)
- 18 DB<sub>4</sub> Digital input (4th)

μPD6951G



1	DB <sub>3</sub>	Digital output (3rd)
2	DB <sub>2</sub>	Digital output (2nd)
3	DB <sub>1</sub>	Digital output (MSB)
4	OVER	Over range
5	DV <sub>DD</sub>	Digital power supply
6	NC	No connection
7	RT	Reference voltage (high voltage side)
8	DGND	Digital GND
9	CLK	Clock input
10	DV <sub>DD</sub>	Digital power supply
11	AV <sub>DD</sub>	Analog power supply
12	AGND	Analog GND
13	NC	No connection
14	V <sub>IN</sub>	Analog input
15	RB	Reference voltage (low level side)
16	NC	No connection
17	DGND	Digital GND
18	DB <sub>6</sub>	Digital input (LSB)
19	DB <sub>5</sub>	Digital input (5th)
20	DB <sub>4</sub>	Digital input (4th)

**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = 25 °C)**

Power supply voltage	-0.3 to +7.0	V
Input terminal voltage	-0.3 to V <sub>DD</sub> +0.3	V
Output terminal voltage	-0.3 to V <sub>DD</sub> +0.3	V
Analog power supply voltage	DV <sub>DD</sub> -0.3 to DV <sub>DD</sub> +0.3	V
Analog GND voltage	DGND-0.3 to DGND+0.3	V
Operating temperature range	-20 to +75	°C
Storage temperature range	-40 to +125	°C

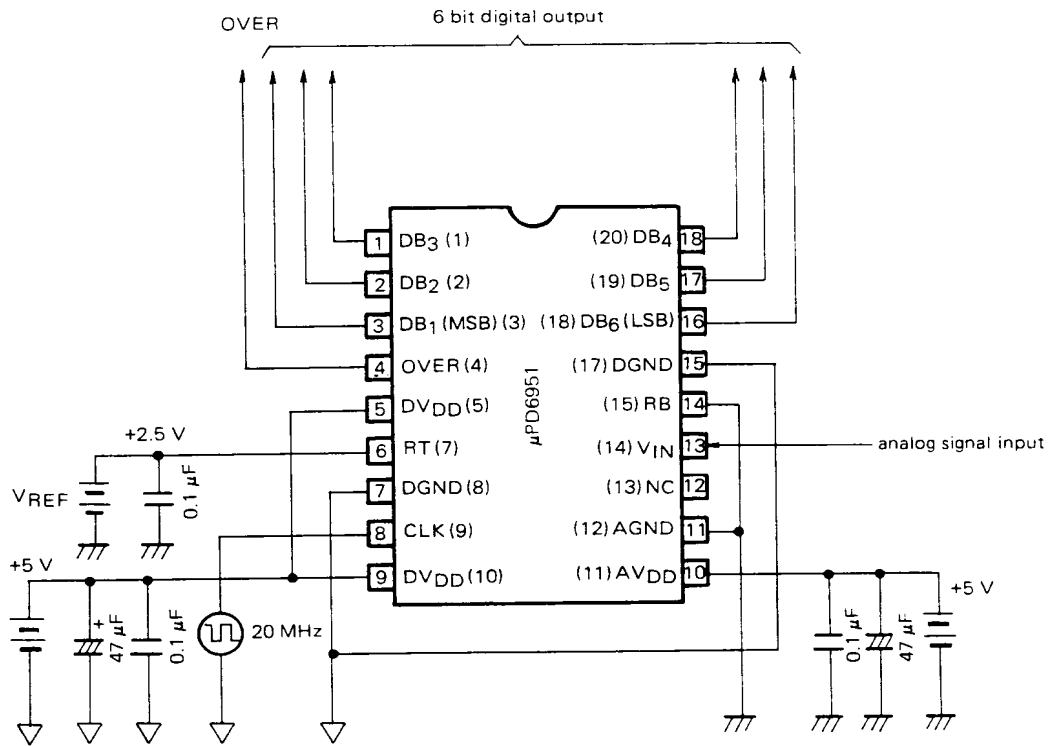
**RECOMMENDED OPERATING CONDITION (T<sub>a</sub> = -20 to +75 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	AV <sub>DD</sub> , DV <sub>DD</sub>	4.5	5.0	5.5	V	AGND=DGND=0 V
Reference voltage	V <sub>REF</sub>	2.0	2.5	3.6	V	V <sub>REF</sub> =V <sub>RT</sub> -V <sub>RB</sub>
RT input voltage	V <sub>RT</sub>	2.0	2.5	3.6	V	
RB input voltage	V <sub>RB</sub>	0		1.6	V	
Sampling clock	f <sub>samp</sub>	0.01		20	MHz	
Sampling clock low level pulse width	t <sub>PWL</sub>	25			ns	
Sampling clock high level pulse width	t <sub>PWH</sub>	25			ns	
CLK input high level	V <sub>IH</sub>	2.7			V	
CLK input low level	V <sub>IL</sub>			0.6	V	
Analog input voltage	V <sub>AIN</sub>	0		AV <sub>DD</sub>	V	

**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = -20 to +75 °C, V<sub>DD</sub> = AV<sub>DD</sub> = DV<sub>DD</sub> = 5 V ±0.5 V, f<sub>samp</sub> = 20 MHz)**

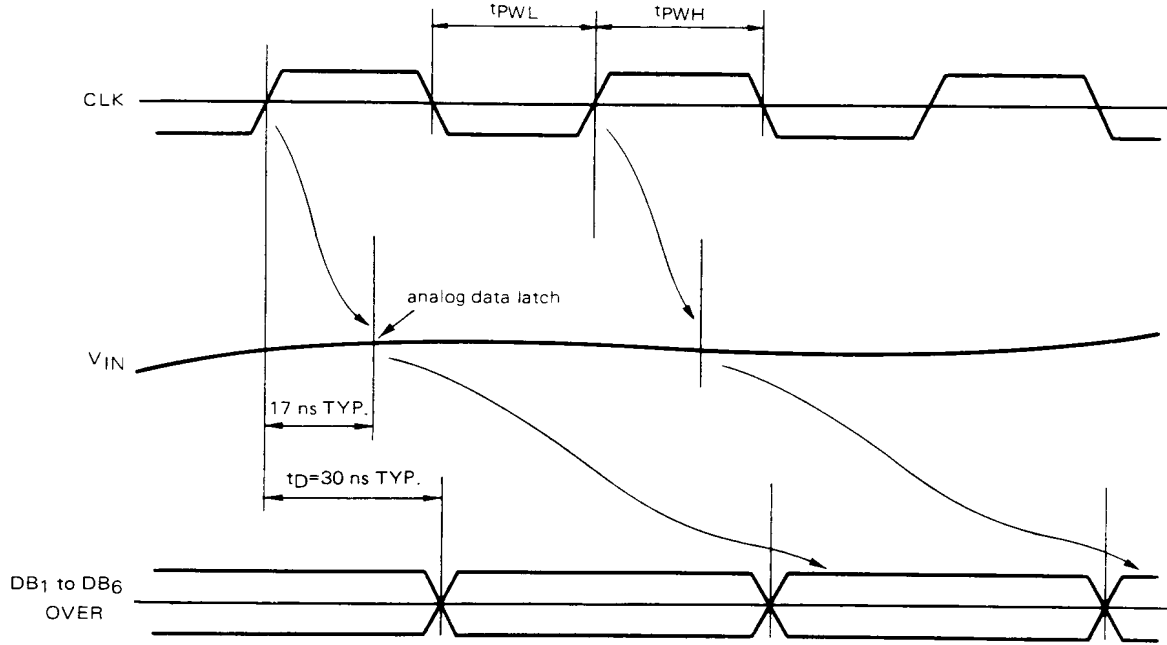
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I <sub>DD</sub>		25	35	mA	I <sub>DD</sub> =A <sub>1DD</sub> +D <sub>1DD</sub> , AV <sub>DD</sub> =DV <sub>DD</sub> =5.0 V
Resolution	RES		6		bit	
Non-linearity	NL		±0.3	±0.5	LSB	V <sub>DD</sub> =5.0±0.25 V, V <sub>REF</sub> =2.5 V, T <sub>a</sub> =0 to 60 °C
Differential non-linearity	DNL		±0.3	±0.5	LSB	V <sub>DD</sub> =5.0±0.25 V, V <sub>REF</sub> =2.5 V, T <sub>a</sub> =0 to 60 °C
Data output delay time	t <sub>D</sub>	20	30	40	ns	CLK ↑ → DB <sub>1</sub> to 6, OVER
Data output high level voltage	V <sub>OH</sub>	2.8			V	I <sub>OH</sub> =-1.0 mA
Data output low level voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> =1.8 mA
Reference resistance	R <sub>REF</sub>		1.3		kΩ	Between RT and RB
Analog input resistance	R <sub>IN</sub>		1		MΩ	
Analog input capacitance	C <sub>IN</sub>		50		pF	
CLK input current	I <sub>IN</sub>			20	μA	V <sub>IN</sub> =GND or DV <sub>DD</sub>

TEST CIRCUIT



( ) shows pins number of μPD6951G. μPD6951G has two more NC terminals, pin 6 and pin 16. There is no necessity to connect.

**TIMING CHART**



**PIN DESCRIPTIONS**

( / ) shows pins number. Right one is μPD6951G's and left one is μPD6951C's terminal number.

- DGND (Pins 7, 15/8, 17) Digital system ground
- AGND (Pin 11/12) Analog system ground
- DV<sub>DD</sub> (Pins 5, 9/5, 10) Digital system power supply (+5 V)
- AV<sub>DD</sub> (Pin 10/11) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.1 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6951C pins. Supply the digital system power from the analog power line through the low path filter to prevent from lurch up.

- RT (Pin 6/7) Reference voltage input pin (high voltage side)
- RB (Pin 14/15) Reference voltage input pin (low voltage side)

These pins are the reference voltage V<sub>REF</sub> input pins.

- V<sub>IN</sub> (Pin 13/14) Analog input pin

The input analog signal applied to this pin is latched synchronized with the rising edge of the sampling clock and is subsequently obtained as an 6 bit digital signal from pins DB<sub>1</sub> thru DB<sub>6</sub>.

Note: Since the electrostatic resistivity of the analog input pin is a little lower than other pins to achieve the required input characteristics, this input should be handled with extra care.

- DB<sub>1</sub> to DB<sub>6</sub> (Pins 1 to 3, and 16 to 18/1 to 3, and 18 to 20) Digital data output pins

DB<sub>1</sub> to DB<sub>6</sub> are the 6 bit digital data output pins. The code format is binary, and the output voltage level is TTL compatible.

The analog signal applied to the analog input pin is latched at the rising edge of the sampling clock, converted to digital data, and then obtained as the output at the next rising edge of the sampling clock.

analog input	digital output						
	OVER	DB <sub>1</sub> (MSB)	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub> (LSB)
0 V (RB) to 1/2 LSB	0	0	0	0	0	0	0
1/2 LSB to (1+1/2) LSB	0	0	0	0	0	0	1
(62+1/2) LSB to (63+1/2) LSB	0	1	1	1	1	1	1
(63+1/2) LSB to 2.5 V (RT)	1	1	1	1	1	1	1
2.5 V (RT) to V <sub>DD</sub>	1	1	1	1	1	1	1

$$LSB = \frac{VRT - VRB}{64}$$

- OVER (Pin 4/4) Over range output pin

This output signal indicates analog signal overflow. A high level output is generated if the input voltage level of the analog input V<sub>IN</sub> exceeds (63+1/2). LSB where LSB is (VRT – VRB)/64.

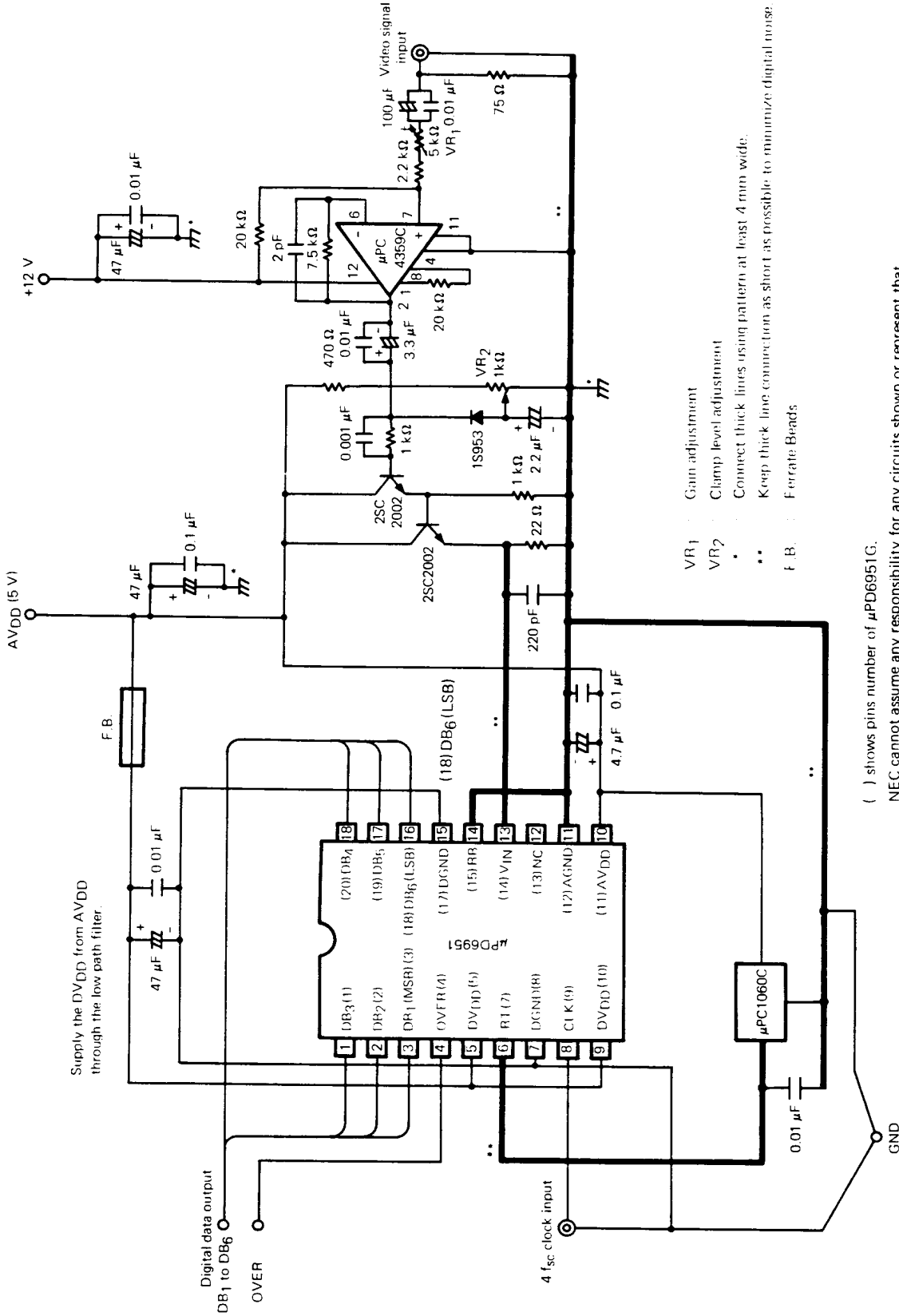
- CLK (Pin 8/9) Sampling clock input pin

The analog signal is latched by the rising edge of the clock signal applied to the A/D converter sampling clock input pin. The complete sequence of events involved in A/D conversion (comparison, encoding, latching, data output) is synchronized with this clock signal. The maximum clock frequency is 20 MHz.

- NC (Pin 12/6, 13, 16) No connection pin

These pins may be connected to analog ground.

APPLICATION CIRCUIT

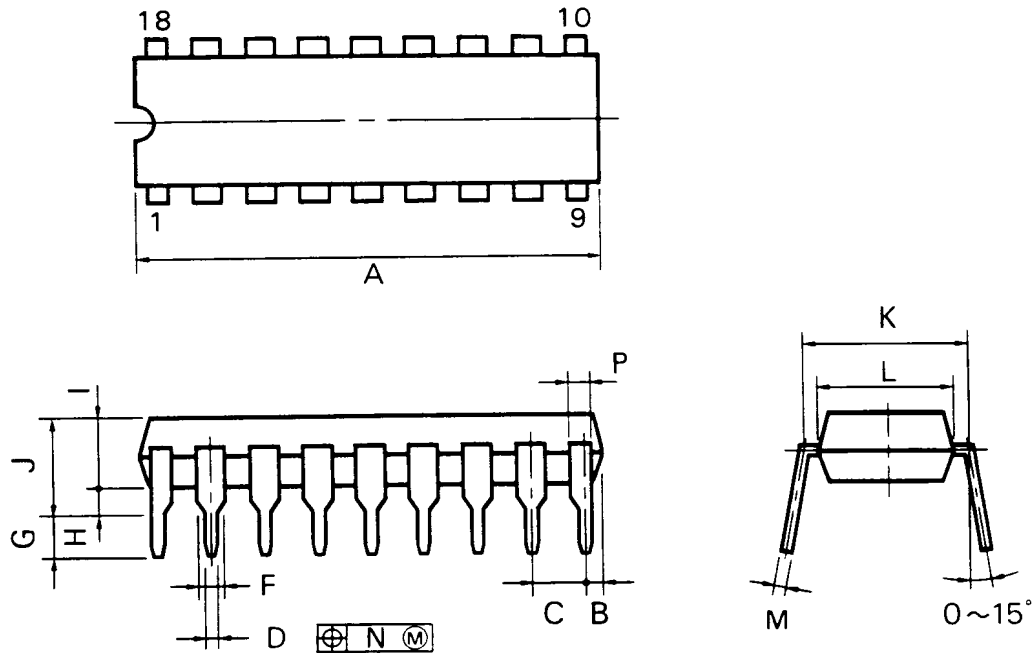


- VR1 Gain adjustment
- VR2 Clamp level adjustment
- Connect thick lines using pattern at least 4 mm wide.
- Keep thick line connection as short as possible to minimize digital noise.
- F.B. Ferrite Beads

( ) shows pins number of μPD6951G.  
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 NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.



18PIN PLASTIC DIP (300 mil)



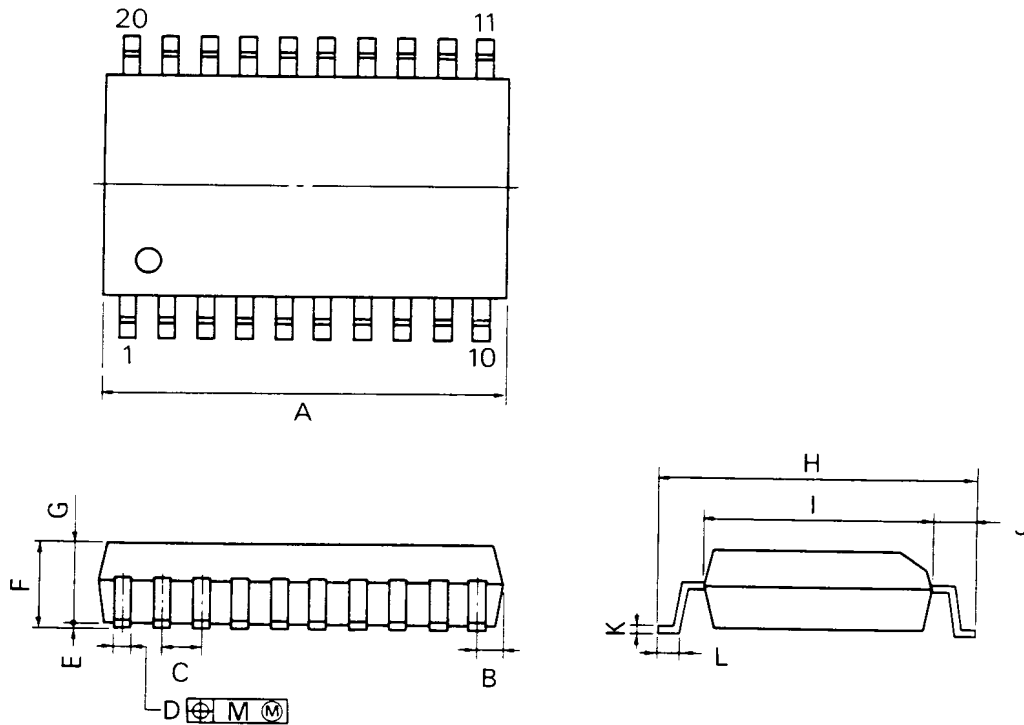
P18C-100-300A.C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>+0.10</sup>	0.020 <sup>+0.004</sup>
F	1.2 MIN.	0.047 MIN.
G	3.5 <sup>+0.3</sup>	0.138 <sup>+0.012</sup>
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 <sup>+0.05</sup>	0.010 <sup>+0.004</sup>
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

20PIN PLASTIC SOP (375 mil)



P20GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 <sup>-0.10</sup> / <sub>0.05</sub>	0.016 <sup>-0.004</sup> / <sub>0.003</sub>
E	0.1 <sup>-0.2</sup> / <sub>0.1</sub>	0.004 <sup>-0.008</sup> / <sub>0.004</sub>
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 <sup>-0.3</sup>	0.406 <sup>-0.013</sup> / <sub>0.013</sub>
I	7.2	0.283
J	1.6	0.063
K	0.15 <sup>-0.10</sup> / <sub>0.05</sub>	0.006 <sup>-0.004</sup> / <sub>0.002</sub>
L	0.8 <sup>-0.2</sup>	0.031 <sup>-0.009</sup> / <sub>0.008</sub>
M	0.12	0.005

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