Direct RDRAM Product Guide

Version 1.9
June 2009

A. Direct RDRAM Component Product Guide

Change History

Version 1.0 (Mar. '03)
First Copy

Version 1.1 (May '03)
Add 576Mb base RIMM® Module

Version 1.2 (July '03)
Add 128Mb F-die , Add 576Mb base 32bit RIMM Module

Version 1.3 (Oct '03)
Add 256Mb E-die , Add 576Mb base SO-RIMM™ & NexMod Module

Version 1.4 (Jan. '04)
Add 288Mb E-die , Add 288Mb E-die base Modules

Version 1.5 (May. '04)
Change the availability of 288Mb D-die/E-die base Modules, etc.

Version 1.6 (Sep. '05)
Add 128Mb H-die , Change the availability of 576Mb A-die & A-die base Modules

Version 1.7 (Mar. '06)
Delete 128Mb E-die, 256/288Mb D-die, 256Mb E-die, etc.

Version 1.8 (Aug. '06)
Add 288Mb I-die, Delete 16bit RIMM based 576Mb A-die, 32bit RIMM, 32d RIMM, SO-RIMM based 576Mb A-die, NexMod based 576Mb A-die

Version 1.9 (Jun. '09)
Delete 128Mb F-die, 128Mb H-die, 256Mb E-die, 288Mb E-die, 576Mb A-die
Delete all of RDRAM module line-up

A. Direct RDRAM Component Product Guide

Density	Org.*1	Part Number	Speed*3	Power(V)	Refresh	Package Type*2	Availability
288Mb(I-die)	512Kx18*32s	K4R881869I-DC	T9	2.5±0.13V	16K/32ms	92ball FBGA	Now

*1 **Bank description**
- 32s :32 banks with a “spilt” architecture

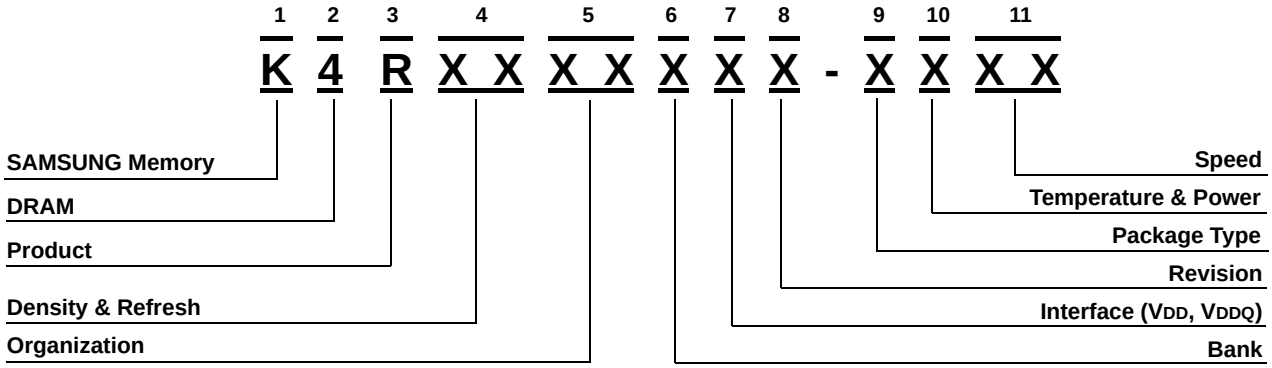
*2 **Package Type**

Code	Description
F	WBGA
G	WBGA, Lead free
H	WBGA, Lead free for SO-RIMM™ module
T	54ball WBGA, Lead free
R	54ball WBGA
D	FBGA, Lead free

*3 **Speed (Freq. & tRAC)**

Data frequency	Application	Code	Description (t_{CYCLE}. t_{RAC}, t_{RC})
1200Mbps	Long channel	N1	600MHz(1.667ns), -32, 32clks
1066Mbps	Long channel	T9	533MHz (1.875ns), -32P, 28clks
		N9	533MHz (1.875ns), -32, 28clks
		M9	533MHz (1.875ns), -35, 32clks
	Short channel	S9	533MHz (1.875ns), -35, 32clks
800Mbps	Long channel	M8	400MHz (2.5ns), -40, 28clks
		K8	400MHz (2.5ns), -45, 28clks
	Short channel	S8	400MHz (2.5ns), -45, 28clks

B. Direct RDRAM Component Ordering Information



1. SAMSUNG Memory : K

2. DRAM : 4

3. Product

R : RDRAM®

4. Density & Refresh

27 : 128M, 16K/32ms(1.95us)
44 : 144M, 16K/32ms(1.95us)
57 : 256M, 16K/32ms(1.95us)
88 : 288M, 16K/32ms(1.95us)
52 : 512M, 32K/32ms(0.98us)
76 : 576M, 32K/32ms(0.98us)

5. Organization

16 : x16
18 : x18

6. Bank

6 : 32 Banks

7. Interface (VDD, VDDQ)

9 : RSL (2.5V)

8. Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
H : 9th Gen.
I : 10th Gen.

9. Package Type

M : * uBGA" package for Mirrored Package
N : * uBGA" package for Normal Package
S : * uBGA" package for Consumer Package
F : WBGA
G : WBGA lead free
H : WBGA lead free for SO-RIMM Module
T : Consumer WBGA(54ball) & Lead free
R : Consumer WBGA(54ball)
D : FBGA & Lead free

10. Temperature & Power

C : Commercial, Normal
L : Commercial, Low
I : Industrial, Normal

11. Speed (t_{CYCLE}. t_{RAC}, t_{RC})

DS : for Daisy chain Sample
N1 : 600MHz (1.667 ns), - 32, 32clks, for Long channel
T9 : 533MHz (1.875 ns), - 32P, 28clks, for Long channel
N9 : 533MHz (1.875 ns), - 32, 28clks, for Long channel
M9 : 533MHz (1.875 ns), - 35, 32clks, for Long channel
S9 : 533MHz (1.875 ns), - 35, 32clks, for Short channel

M8 : 400MHz (2.5 ns), - 40, 28clks, for Long channel
K8 : 400MHz (2.5 ns), - 45, 28clks, for Long channel
S8 : 400MHz (2.5 ns), - 45, 28clks, for Short channel

K7 : 356MHz (2.81 ns), - 45, 28clks, for Long channel
G6 : 300MHz (3.33 ns), - 53.3, 28clks, for Long channel
S6 : 300MHz (3.33 ns), - 53.3, 28clks, for Short channel

* uBGA and micro BGA are registered trademarks of Tessera, Inc.