

Description

The μ PD6307 can directly drive any multiplexed LCD organized with up to 32 rows. It is easily cascaded to 128 rows.

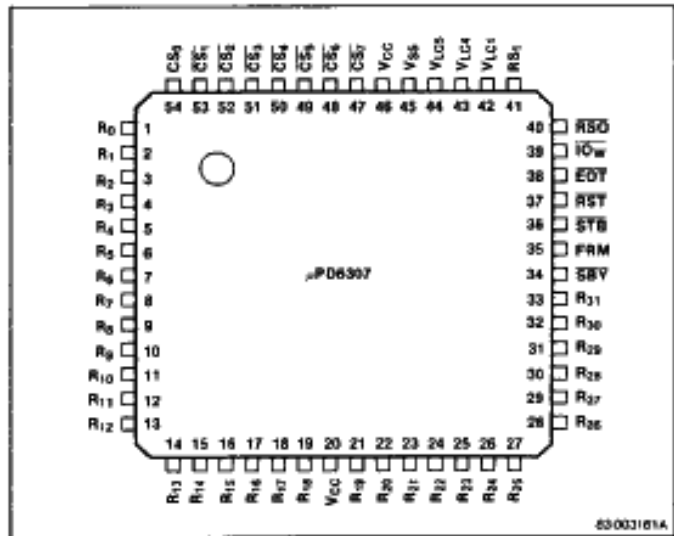
Features

- High voltage output 21 V maximum
- Directly controllable by the μ PD72030
- CMOS technology
- Single 5 V \pm 10% power supply

Ordering Information

Part Number	Package Type
μ PD6307G-F	54-pin plastic miniflat
μ PD6307G-R	54-pin plastic miniflat (inverted leads)

Pin Configuration



Pin Identification

No.	Symbol	Function
1-19, 21-23	R_0 - R_{31}	Row drive output
20	V_{CC}	Positive power supply
34	SBY	Standby input
35	FRM	Frame input
36	STB	Strobe input
37	RST	Reset input
38	EOT	End of transfer input
39	IOW	I/O write input
40, 41	RS_0 , RS_1	Row select input
42-44	V_{LC1} , V_{LC4} , V_{LC5}	LCD drive supply
45	V_{SS}	Ground
46	V_{CC} ($= V_{LC0}$)	Positive power supply and LCD drive supply
47-54	CS_7 - CS_0	Chip select output

Pin Functions

R₀-R₃₁ (Row Drive Output)

LCD row drive output.

\overline{CS}_0 - \overline{CS}_7 (Chip Select)

Column driver chip select. These outputs are generated by the CS counter and RS₀-RS₁.

V_{LC1}, V_{LC4}, V_{LC5} (LCD Drive Supply)

Reference voltages used to drive R₀-R₃₁.

RS₀, RS₁ (Row Select)

This input selects the row driver cascade connection. It enables expansion to 128 row drive outputs and 32 \overline{CS} outputs, as shown in table 1.

FRM (Frame)

A high level input to this pin displays a positive frame and a low level input displays a negative frame. At the falling or rising edge of the signal, the row counter is cleared and the row driver is started from R₀.

STB (Strobe)

Row drive strobe input. One STB pulse input at the timing interval causes the display of the next row.

\overline{IOW} (I/O Write)

This input increments the CS counter signal following 10 low level \overline{IOW} pulses.

\overline{EOT} (End of Transfer)

This input clears the CS counter when it goes active low.

\overline{RST} (Reset)

This is the row driver reset input. A low input clears the internal counter and row outputs R₀-R₃₁, and sets the \overline{CS}_0 - \overline{CS}_7 outputs to a high level.

\overline{SBY} (Standby)

This is the standby input. A low level input to this pin sets the row outputs R₀-R₃₁ to V_{LC0}. Before entering standby mode, set all column driver display data to high level.

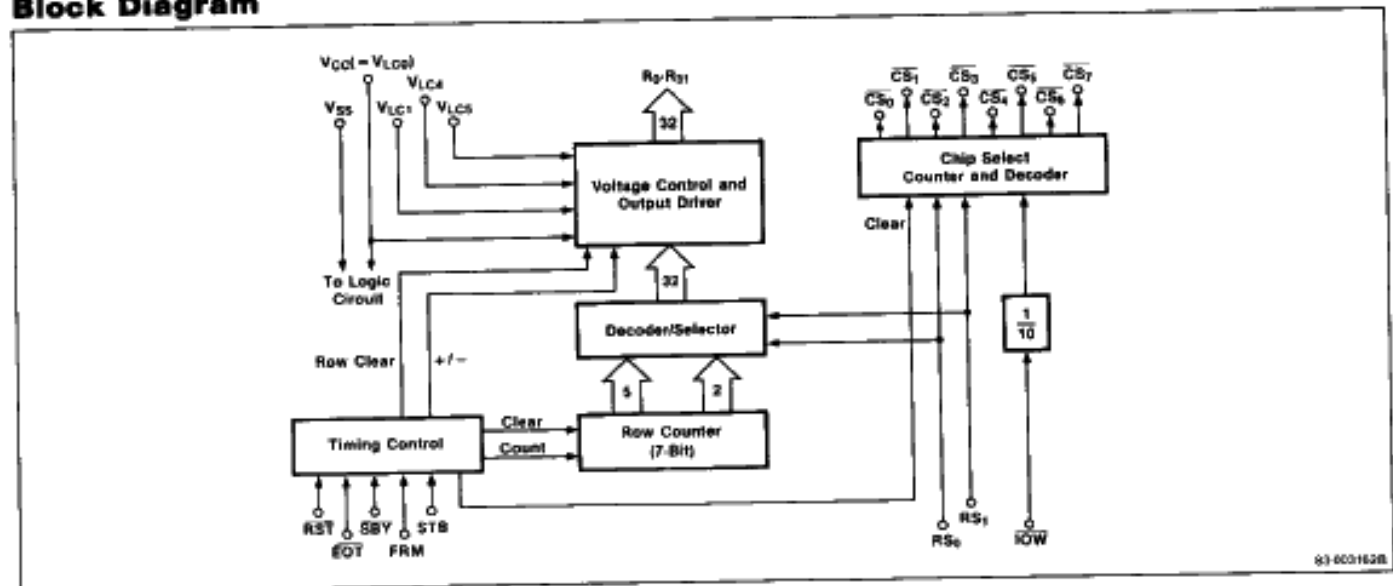
V_{CC} (= V_{LC0}) (Power Supply and LCD Drive Supply)

Connect the 5 V power supply between V_{CC} and V_{SS} for logic circuit operation. This pin is also used for the row drive voltage output.

V_{SS} (Ground)

Ground.

Block Diagram



83-00162B

Functional Description

Timing Control Circuit

This circuit controls the timing for each internal block. FRM, RS₀, RS₁, \overline{RST} , and \overline{SBY} are sampled at the leading edge of STB, and then supplied to other internal circuits.

Row Counter Decoder/Select Circuit

As shown in figure 1, this circuit consists of a 7-bit counter, a comparator, and a 5 to 32 decoder. The 7-bit counter can accommodate 128 rows. The comparator acts to clear R₀-R₃₁ if the upper two bits of the counter do not match RS₀ and RS₁. If they match, one of R₀-R₃₁, indicated by the lower five bits of the row counter, is selected and the rest are cleared. RS₀ and RS₁ allow for cascading as shown in table 1. Table 2 shows the row select logic.

Figure 1. Row Counter Decoder/Select Circuit

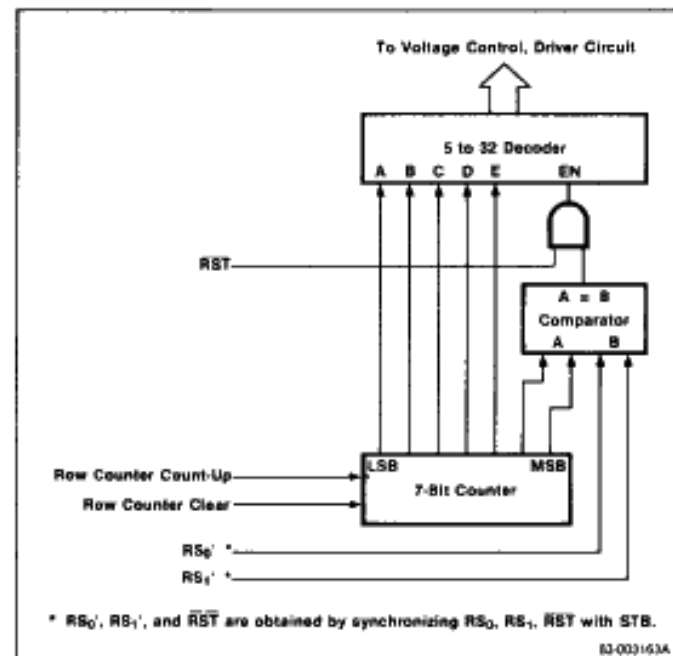


Table 1. RS₀ and RS₁ Row Cascading

RS ₀	RS ₁	Row Signal	Chip Select
0	0	R ₀ -R ₃₁	\overline{CS}_0 - \overline{CS}_7
0	1	R ₃₂ -R ₆₃	\overline{CS}_8 - \overline{CS}_{15}
1	0	R ₆₄ -R ₉₅	\overline{CS}_{16} - \overline{CS}_{23}
1	1	R ₉₆ -R ₁₂₇	\overline{CS}_{24} - \overline{CS}_{31}

Table 2. Row Select Logic

EN	E	D	C	B	A	Selected Row Signal
1	0	0	0	0	0	R ₀
1	0	0	0	0	1	R ₁
1	↓	↓	↓	↓	↓	R _n
1	1	1	1	1	0	R ₃₀
1	1	1	1	1	1	R ₃₁
0	X	X	X	X	X	None

Voltage Control Driver Circuit

This circuit generates the row signals for AC drive of the LCD panel. A low level \overline{RST} clears the output. A low level \overline{SBY} sets the output V_{LCO}. Table 2 shows the R₀-R₃₁ output levels.

Table 2. R₀-R₃₁ Outputs Levels

Function	+ (FRM = 1)	- (FRM = 0)
Select	V _{LCS}	V _{LCO}
Clear	V _{LCA}	V _{LCl}

Chip Select Counter/Decoder Circuit

This circuit, shown in figure 2, generates the column driver \overline{CS} signal. This circuit has a 5-bit counter to generate up to 32 \overline{CS} signals. The 5-bit counter is incremented once for every 10 \overline{IOW} (active low) pulses. If the upper two bits of the chip select counter do not match RS₀ and RS₁, all the \overline{CS}_0 - \overline{CS}_7 outputs are set to high level. If they match, one of \overline{CS}_0 - \overline{CS}_7 (indicated by the lower three bits of the chip select counter) goes low. If \overline{RST} is low, \overline{CS}_0 - \overline{CS}_7 become high level. Table 3 shows the chip select logic.

Figure 2. Chip Select Counter/Decoder Circuit

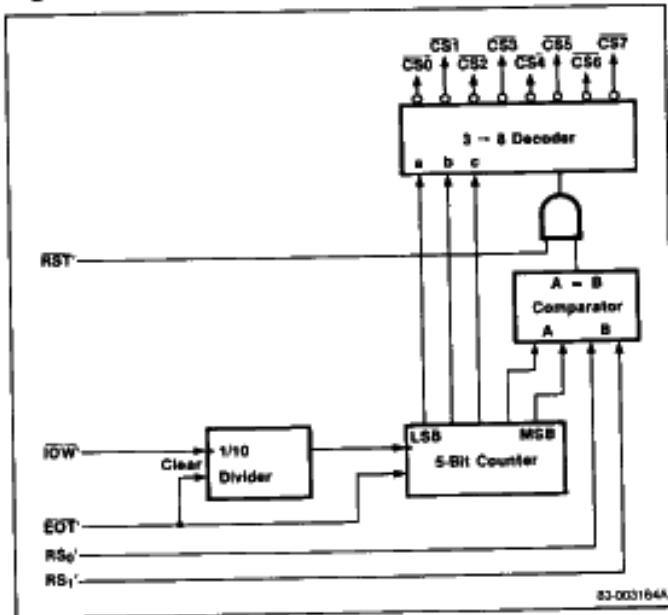


Table 3. Chip Select Logic

EN	c	b	a	Chip Select
1	0	0	0	CS ₀
1	0	0	1	CS ₁
1	0	1	0	CS ₂
1	0	1	1	CS ₃
1	1	0	0	CS ₄
1	1	0	1	CS ₅
1	1	1	0	CS ₆
1	1	1	1	CS ₇
0	X	X	X	Disabled

83-003164A