**BGA**
**Commercial Temp**
**Industrial Temp**

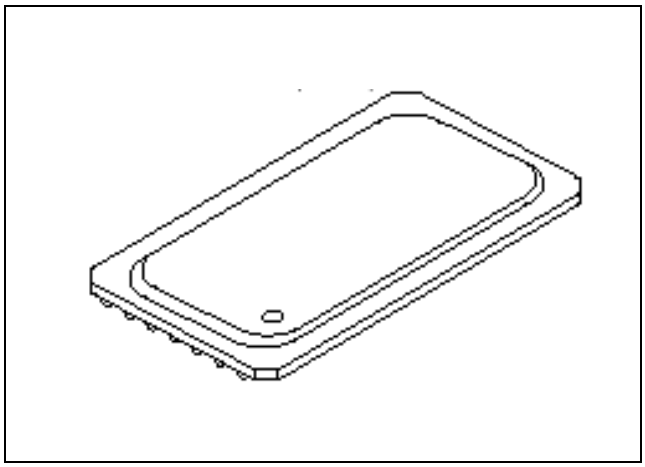
# 128K x 24
# 3Mb Asynchronous SRAM

**10, 12, 15ns**
**3.3V $V_{DD}$**

## Features

- Fast access time: 10, 12, 15ns
- CMOS low power operation: 250/220/180 mA at min. cycle time.
- Single 3.3V ± 0.3V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Industrial Temperature Option: -40 to 85°C
- Package
  B: 14mm x 22mm, 119 bump, 1.27mm pitch BGA

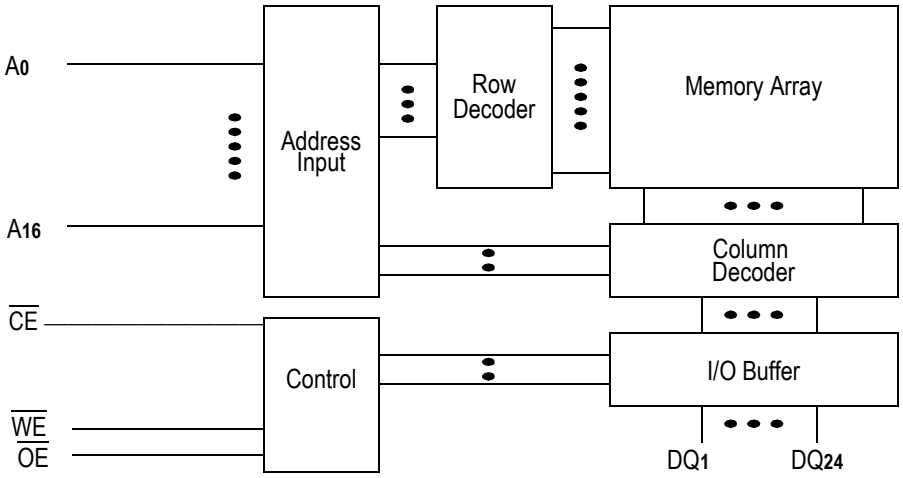
**119 Bump Ball Grid Array Package**



## Description

The GS73024 is a high speed CMOS static RAM organized as 131,072 words by 24 bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS73024 is available in a 119 Bump BGA package.

## Block Diagram




## Pin Descriptions

| Symbol | Description | Symbol | Description |
|---|---|---|---|
| $A_0$ to $A_{16}$ | Address input | $DQ_1$ to $DQ_{24}$ | Data input/output |
| $\overline{WE}$ | Write enable input | $\overline{OE}$ | Output enable input |
| $\overline{CE}$ | Chip enable input | | |
| $V_{DD}$ | +3.3V power supply | $V_{SS}$ | Ground |

## 119 Bump, 1.27mm Pitch BGA Pad Out

### Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | NC | $A_3$ | $A_2$ | $A_{16}$ | $A_1$ | $A_0$ | NC |
| B | NC | $A_7$ | $A_6$ | $\overline{CE}$ | $A_5$ | $A_4$ | NC |
| C | $DQ_{13}$ | NC | $V_{DD}$, NC | NC | $V_{SS}$, NC | NC | $DQ_{12}$ |
| D | $DQ_{14}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_{11}$ |
| E | $DQ_{15}$ | NC | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | NC | $DQ_{10}$ |
| F | $DQ_{16}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_9$ |
| G | $DQ_{17}$ | NC | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | NC | $DQ_8$ |
| H | $DQ_{18}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_7$ |
| J | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ |
| K | $DQ_{19}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_6$ |
| L | $DQ_{20}$ | NC | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | NC | $DQ_5$ |
| M | $DQ_{21}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_4$ |
| N | $DQ_{22}$ | NC | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | NC | $DQ_3$ |
| P | $DQ_{23}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $DQ_2$ |
| R | $DQ_{24}$ | NC | NC | NC | NC | NC | $DQ_1$ |
| T | NC | $A_{11}$ | $A_{10}$ | $\overline{WE}$ | $A_9$ | $A_8$ | NC |
| U | NC | $A_{15}$ | $A_{14}$ | $\overline{OE}$ | $A_{13}$ | $A_{12}$ | NC |

Note: Bumps 3C and 5C are actually NC's but should be wired 3C=$V_{DD}$ and 5C=$V_{SS}$ to assure compatibility with future versions.

### Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | DQ0 to DQ23 | $V_{DD}$ Current |
|---|---|---|---|---|---|
| H | X | X | Not selected | High Z | ISB1, ISB2 |
| L | L | H | Read | Data Out | $I_{DD}$ |
| L | X | L | Write | Data In | |
| L | H | H | Output disable | High Z | |

X: "H" or "L"

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +4.6 | V |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 (≤ 4.6V max.) | V |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DD}$+0.5 (≤ 4.6V max.) | V |
| Allowable BGA power dissipation | PD | 1.5 | W |
| Storage temperature | $T_{STG}$ | -55 to 150 | °C |

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage for -10/12/15 | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{DD}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Ambient Temperature, Commercial Range | $T_{Ac}$ | 0 | - | 70 | °C |
| Ambient Temperature, Industrial Range | $T_{Ai}$ | -40 | - | 85 | °C |

Note:
1. Input overshoot voltage should be less than $V_{DD}$+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

## Capacitance

| Parameter | Symbol | Test Condition | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | 10 | pF |
| I/O Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | 7 | pF |

Notes:
1. Tested at $T_A$=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

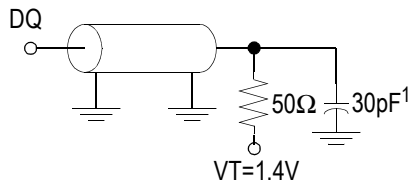
## DC I/O Pin Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0 to $V_{DD}$ | -2uA | 2uA |
| Output Leakage Current | $I_{OL}$ | Output High Z, $V_{OUT}$ = 0 to $V_{DD}$ | -1uA | 1uA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 4mA | 2.4 | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = + 4mA | | 0.4V |

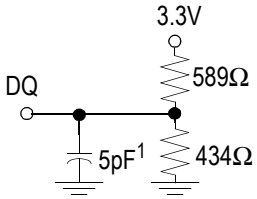
## AC Test Conditions

| Parameter | Conditions |
|---|---|
| Input high level | $V_{IH}$=2.4V |
| Input low level | $V_{IL}$=0.4V |
| Input rise time | tr=1V/ns |
| Input fall time | tf=1V/ns |
| Input reference level | 1.4V |
| Output reference level | 1.4V |
| Output load | Fig. 1& 2 |

Output Load 1




Output Load 2




Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for $t_{LZ}$, $t_{HZ}$, $t_{OLZ}$ and $t_{OHZ}$.

## Power Supply Currents

| Parameter | Symbol | Test Conditions | 0 to 70°C | | | -40 to 85°C | | |
|---|---|---|---|---|---|---|---|---|
| | | | 10ns | 12ns | 15ns | 10ns | 12ns | 15ns |
| Operating Supply Current | $I_{DD}$ | $\overline{CE} \le V_{IL}$<br>All other inputs<br>$\ge V_{IH}$ or $\le V_{IL}$<br>Min. cycle time<br>$I_{OUT}$ = 0 mA | 250mA | 220mA | 180mA | 270mA | 240mA | 200mA |
| Standby Current | $I_{SB1}$ | $\overline{CE} \ge V_{IH}$<br>All other inputs<br>$\ge V_{IH}$ or $\le V_{IL}$<br>Min. cycle time | 100mA | 90mA | 80mA | 120mA | 110mA | 100mA |
| Standby Current | $I_{SB2}$ | $CE \ge V_{DD}$ - 0.2V<br>All other inputs<br>$\ge V_{DD}$ - 0.2V or $\le$ 0.2V | 30mA | | | 50mA | | |

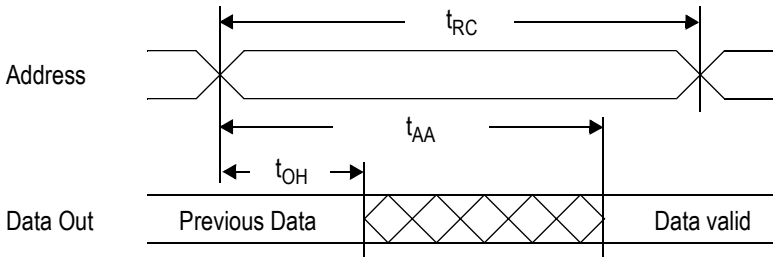
## AC Characteristics

### Read Cycle

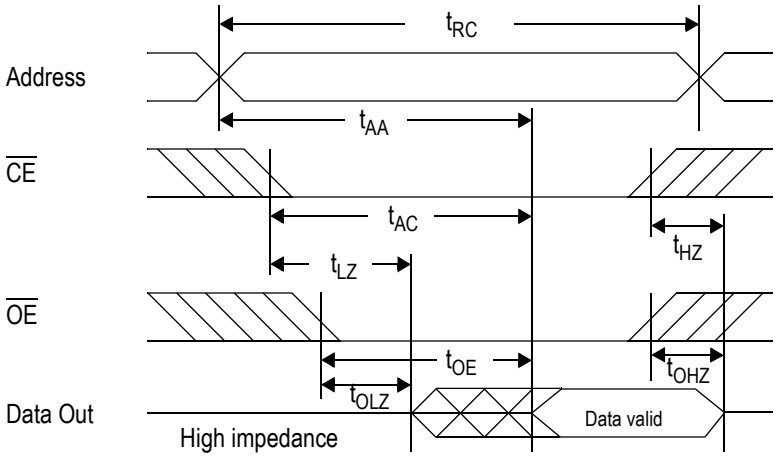
| Parameter | Symbol | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Read cycle time | $t_{RC}$ | 10 | --- | 12 | --- | 15 | --- | ns |
| Address access time | $t_{AA}$ | --- | 10 | --- | 12 | --- | 15 | ns |
| Chip enable access time ($\overline{CE}$) | $t_{AC}$ | --- | 10 | --- | 12 | --- | 15 | ns |
| Output enable to output valid ($\overline{OE}$) | $t_{OE}$ | --- | 5 | --- | 6 | --- | 7 | ns |
| Output hold from address change | $t_{OH}$ | 3 | --- | 3 | --- | 3 | --- | ns |
| Chip enable to output in low Z ($\overline{CE}$) | $t_{LZ}$* | 3 | --- | 3 | --- | 3 | --- | ns |
| Output enable to output in low Z ($\overline{OE}$) | $t_{OLZ}$* | 0 | --- | 0 | --- | 0 | --- | ns |
| Chip disable to output in High Z ($\overline{CE}$) | $t_{HZ}$* | --- | 5 | --- | 6 | --- | 7 | ns |
| Output disable to output in High Z ($\overline{OE}$) | $t_{OHZ}$* | --- | 5 | --- | 6 | --- | 7 | ns |

* These parameters are sampled and are not 100% tested

## Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$




## Read Cycle 2: $\overline{WE}$ = $V_{IH}$



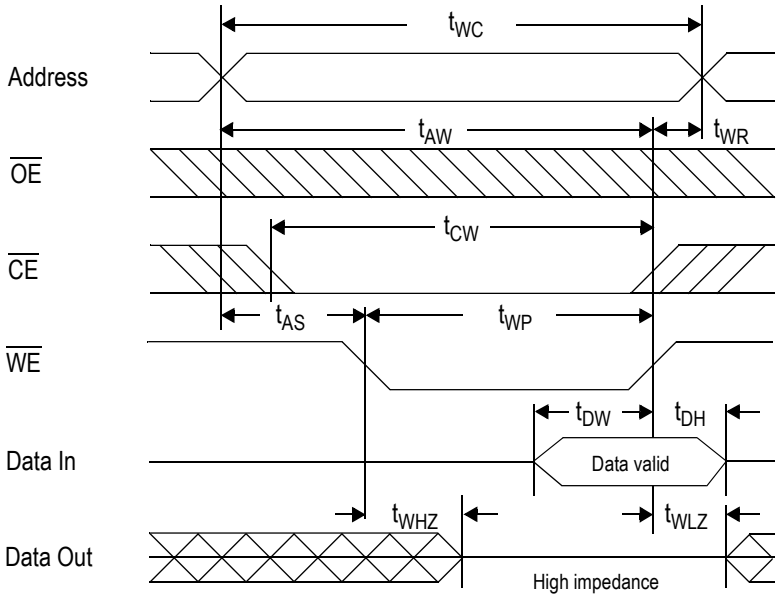

  

## Write Cycle

| Parameter | Symbol | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Write cycle time | $t_{WC}$ | 10 | --- | 12 | --- | 15 | --- | ns |
| Address valid to end of write | $t_{AW}$ | 7 | --- | 8 | --- | 10 | --- | ns |
| Chip enable to end of write ($\overline{CE}$) | $t_{CW}$ | 7 | --- | 8 | --- | 10 | --- | ns |
| Data set up time | $t_{DW}$ | 5 | --- | 6 | --- | 7 | --- | ns |
| Data hold time | $t_{DH}$ | 0 | --- | 0 | --- | 0 | --- | ns |
| Write pulse width | $t_{WP}$ | 7 | --- | 8 | --- | 10 | --- | ns |
| Address set up time | $t_{AS}$ | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time ($\overline{WE}$) | $t_{WR}$ | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time ( $\overline{CE}$ ) | $t_{WR1}$ | 0 | --- | 0 | --- | 0 | --- | ns |
| Output Low Z from end of write | $t_{WLZ}$* | 3 | --- | 3 | --- | 3 | --- | ns |
| Write to output in High Z | $t_{WHZ}$* | --- | 5 | --- | 6 | --- | 7 | ns |

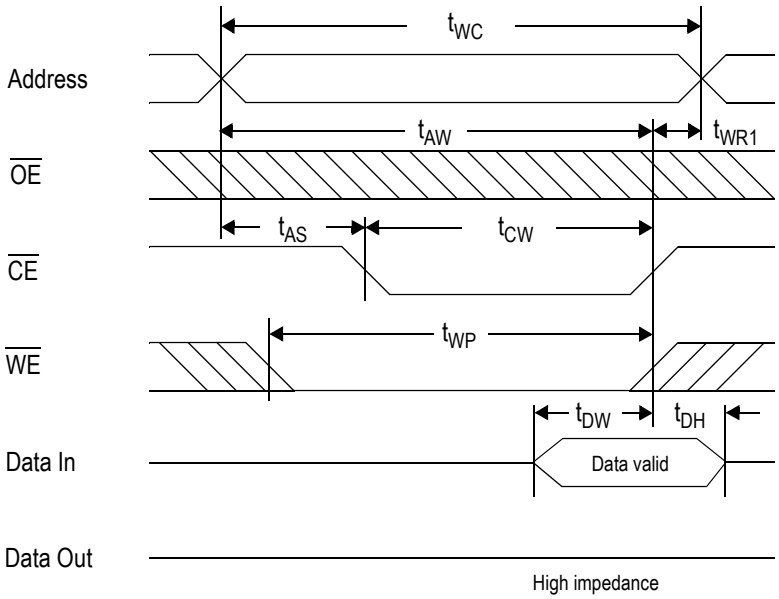
* These parameters are sampled and are not 100% tested

## Write Cycle 1: $\overline{WE}$ control



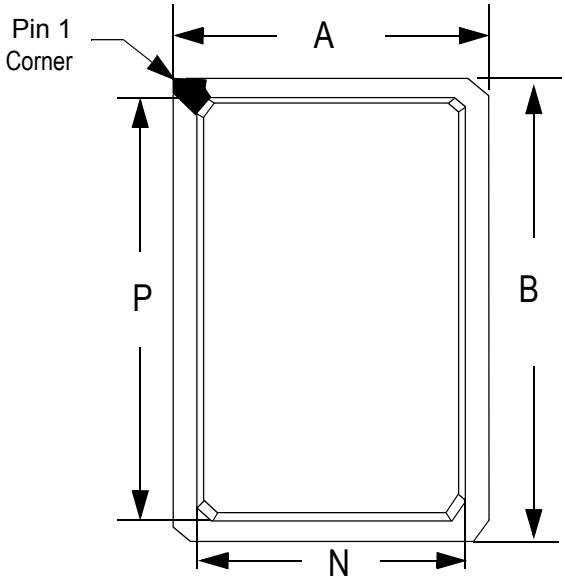

 
 

## Write Cycle 2: $\overline{CE}$ control

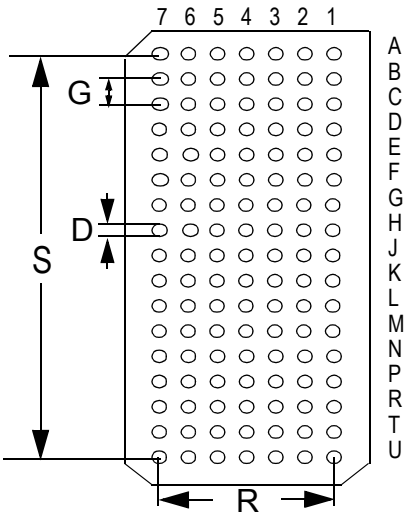


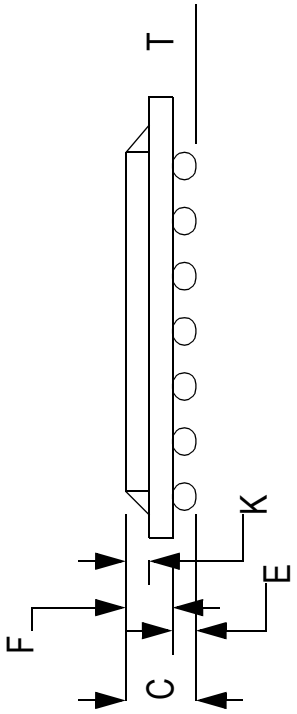
## Package Dimensions - 119 Pin PBGA




Top View




Bottom View




Side View

### Package Admissions - 119 Pin PBGA

| Symbol | Description | Min. | Nom. | Max |
|---|---|---|---|---|
| A | Width | 13.8 | 14.0 | 14.2 |
| B | Length | 21.8 | 22.0 | 22.2 |
| C | Package Height (including ball) | - | | 2.40 |
| D | Ball Size | 0.60 | 0.75 | 0.90 |
| E | Ball Height | 0.50 | 0.60 | 0.70 |
| F | Package Height (excluding balls) | | 1.46 | 1.70 |
| G | Width between Balls | | 1.27 | |
| K | Package Height above board | 0.80 | 0.90 | 1.00 |
| N | Cut-out Package Width | | 12.00 | |
| P | Foot Length | | 19.50 | |
| R | Width of package between balls | | 7.62 | |
| S | Length of package between balls | | 20.32 | |
| T | Variance of Ball Height | | 0.15 | |

Unit: mm

BPR 1999.05.18

## Ordering Information

| Part Number | Package | Access Time | Temp. Range | Status |
|---|---|---|---|---|
| GS73024B-10 | 119 Bump BGA | 10 ns | Commercial | |
| GS73024B-12 | 119 Bump BGA | 12 ns | Commercial | |
| GS73024B-15 | 119 Bump BGA | 15 ns | Commercial | |
| GS73024B-10I | 119 Bump BGA | 10 ns | Industrial | |
| GS73024B-12I | 119 Bump BGA | 12 ns | Industrial | |
| GS73024B-15I | 119 Bump BGA | 15 ns | Industrial | |

* Customers requiring Tape and Reel should add the character "T" to the end of the part number. For example: GS73024B-12T

## Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page/Revisions/Reason |
|---|---|---|
| GS73024Rev 2:17pm, 4/8/1999; 1.00a5/1999 | Format/Typos | • Document Changed subscripts to small caps.<br>• Document/Replaced "micro" with "fine pitch". |
| | Content | • Ordering Information/Added Tape and Reel Note/Enhancement<br>• Pin Description/Changed A0 - A14 to A0 - A16/Correction<br>•<br>• Page 1/Took out "Byte Control" from Features/Correction<br>• Document/Removed 8n version from Datasheet/Product not offered.<br>• Package Diagram/Added "n" to Dimensions. |
| GS73024Rev1.01a5/ 1999C;Rev1.012/2000D | Format | • GSI Logo |