

Commercial Temp
Industrial Temp

Asynchronous SRAM

ns
3.3 V V_{DD}
 V_{DD} and V_{SS}

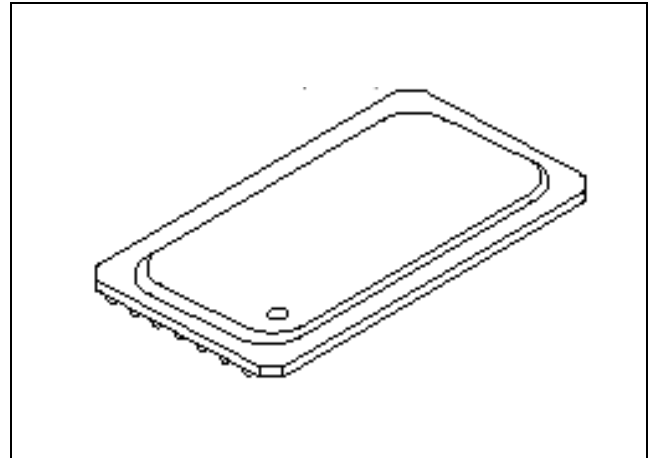
Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 250/200/170 mA at minimum cycle time
- Single 3.3 V \pm 0.3V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: -40 to 85°C
- Package
 - B: 14 mm x 22 mm, 119-bump, 1.27mm pitch BGA

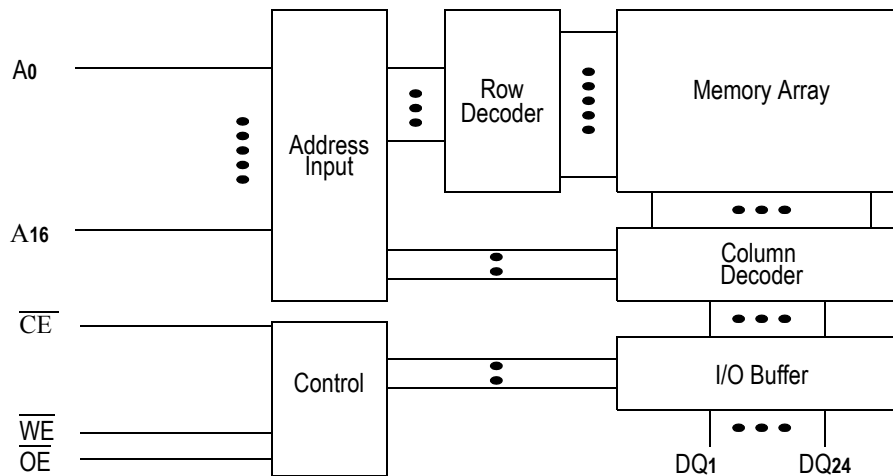
Description

The GS73024A is a high speed CMOS Static RAM organized as 131,072 words by 24 bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS73024A is available in a 119-bump BGA package.

119-Bump Ball Grid Array Package



Block Diagram



Pin Descriptions

Symbol	Description	Symbol	Description
A0 to A16	Address input	DQ1 to DQ24	Data input/output
$\overline{\text{WE}}$	Write enable input	OE	Output enable input
$\overline{\text{CE}}$	Chip enable input	V_{SS}	Ground
V_{DD}	+3.3 V power supply		

119-Bump, 1.27 mm Pitch BGA Pad Out—Top View (Package B)

	1	2	3	4	5	6	7
A	NC	A3	A2	A16	A1	A0	NC
B	NC	A7	A6	$\overline{\text{CE}}$	A5	A4	NC
C	DQ13	NC	NC	NC	NC	NC	DQ12
D	DQ14	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ11
E	DQ15	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ10
F	DQ16	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ9
G	DQ17	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ8
H	DQ18	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ7
J	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}
K	DQ19	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ6
L	DQ20	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ5
M	DQ21	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ4
N	DQ22	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ3
P	DQ23	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ2
R	DQ24	NC	NC	NC	NC	NC	DQ1
T	NC	A11	A10	$\overline{\text{WE}}$	A9	A8	NC
U	NC	A15	A14	$\overline{\text{OE}}$	A13	A12	NC

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	DQ0 to DQ23	V_{DD} Current
H	X	X	Not selected	High Z	ISB1, ISB2
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	
L	H	H	Output disable	High Z	

X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Input Voltage	V_{IN}	-0.5 to $V_{\text{DD}} + 0.5$ (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	-0.5 to $V_{\text{DD}} + 0.5$ (≤ 4.6 V max.)	V
Allowable BGA power dissipation	PD	1.5	W
Storage temperature	T_{STG}	-55 to 150	$^{\circ}\text{C}$

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -10/12	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for -8	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	$V_{DD}+0.3$	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	-40	—	85	°C

Notes:

1. Input overshoot voltage should be less than $V_{DD} + 2\text{ V}$ and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	5	pF
I/O Capacitance	C_{OUT}	$V_{OUT} = 0\text{ V}$	7	pF

Notes:

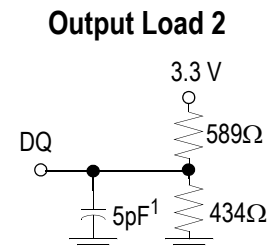
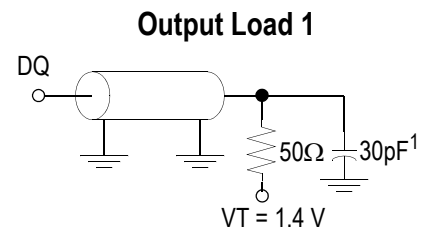
1. Tested at $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	$V_{IN} = 0\text{ to }V_{DD}$	-1 μA	1 μA
Output Leakage Current	I_{OL}	Output High Z, $V_{OUT} = 0\text{ to }V_{DD}$	-1 μA	1 μA
Output High Voltage	V_{OH}	$I_{OH} = -4\text{ mA}$	2.4	—
Output Low Voltage	V_{OL}	$I_{OL} = +4\text{ mA}$	—	0.4 V

AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4 \text{ V}$
Input low level	$V_{IL} = 0.4 \text{ V}$
Input rise time	$t = 1 \text{ V/ns}$
Input fall time	$t_f = 1 \text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1 & 2


Notes:

1. Includes scope and jig capacitance
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ}

Power Supply Currents

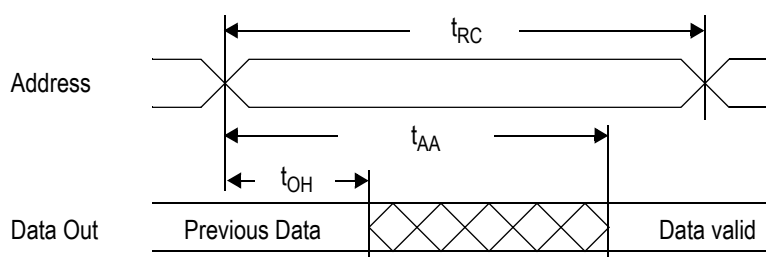
Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0 \text{ mA}$	250 mA	200 mA	170 mA	260 mA	210 mA	180 mA
Standby Current	I_{SB1}	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	40 mA	40 mA	30 mA	50 mA	50 mA	40 mA
Standby Current	I_{SB2}	$CE \geq V_{DD} - 0.2\text{V}$ All other inputs $\geq V_{DD} - 0.2\text{V}$ or $\leq 0.2\text{V}$	10 mA			20 mA		

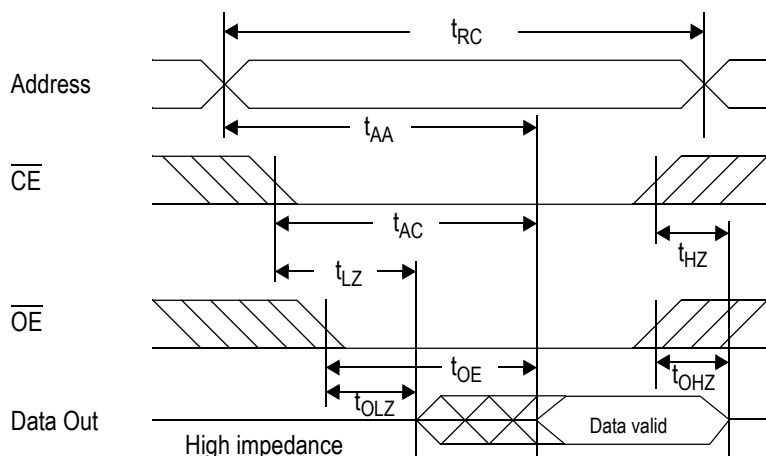
AC Characteristics
Read Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time (\overline{CE})	t_{AC}	—	8	—	10	—	12	ns
MUX control to output valid (V/\overline{S})	t_{AV}	—	8	—	10	—	12	ns
Output enable to output valid (\overline{OE})	t_{OE}	—	4	—	5	—	6	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Output hold from MUX controls change	t_{OH1}	3	—	3	—	3	—	ns
Chip enable to output in low Z (\overline{CE})	t_{LZ}^*	3	—	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}^*	0	—	0	—	0	—	ns
Chip disable to output in High Z (\overline{CE})	t_{HZ}^*	—	4	—	5	—	6	ns
Output disable to output in High Z (\overline{OE})	t_{OHZ}^*	—	4	—	5	—	6	ns

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

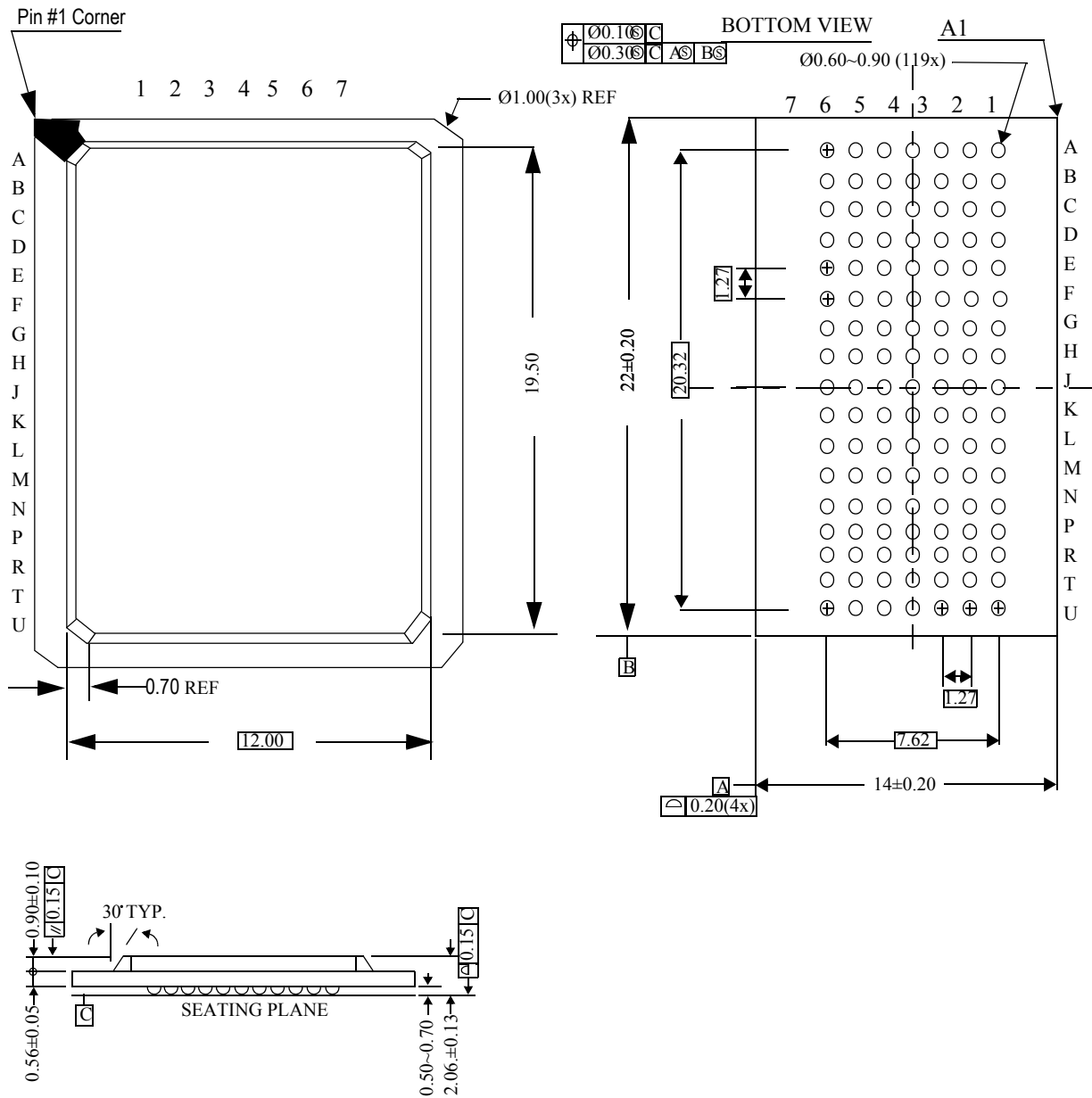


Read Cycle 2: $\overline{WE} = V_{IH}$

Write Cycle

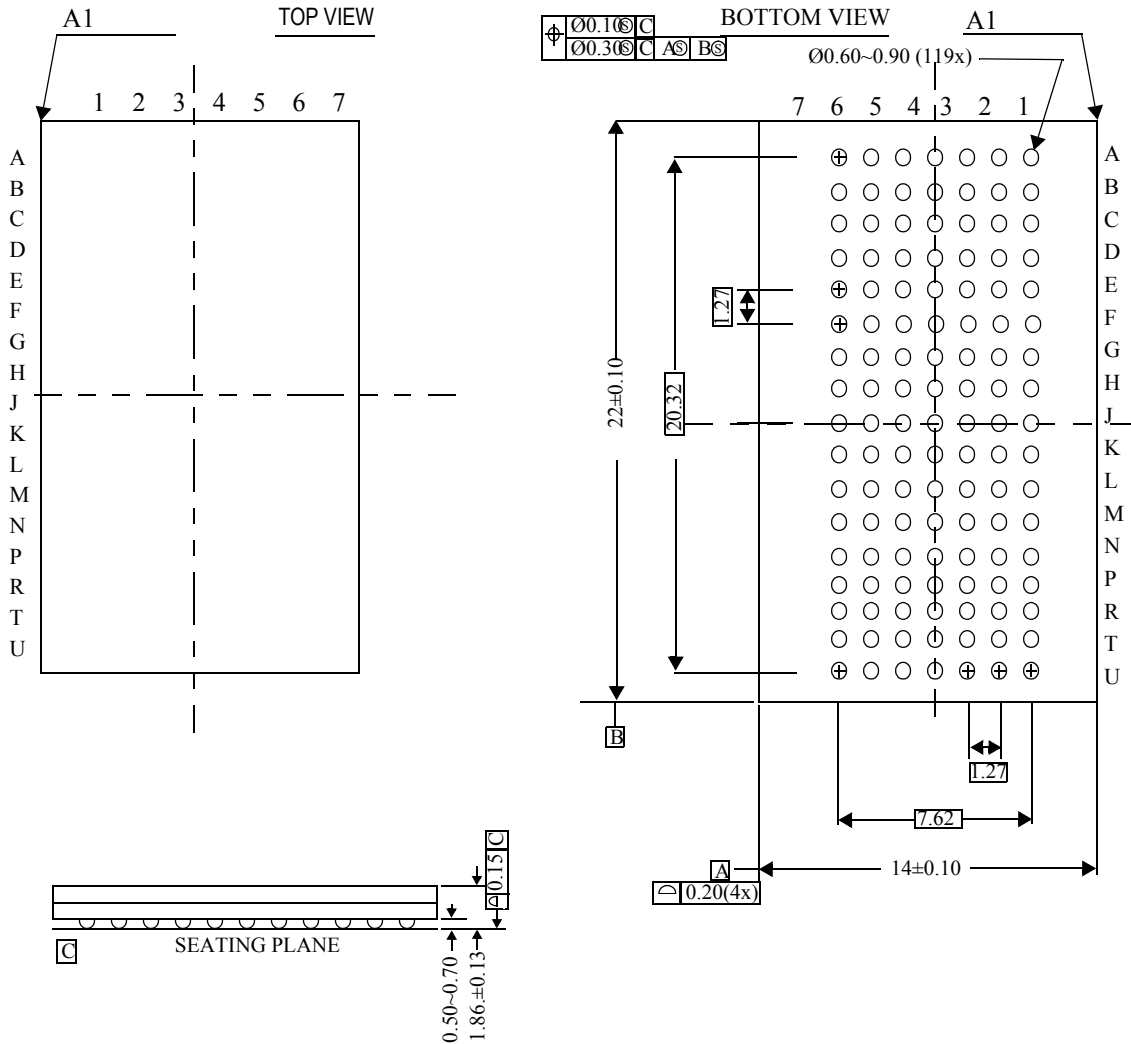
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	8	—	10	—	12	—	ns
Address valid to end of write	t_{AW}	5.5	—	7	—	8	—	ns
Chip enable to end of write (\overline{CE})	t_{CW}	5.5	—	7	—	8	—	ns
Data set up time	t_{DW}	4	—	5	—	6	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	5.5	—	7	—	8	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t_{WR}	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t_{WR1}	0	—	0	—	0	—	ns
Output Low Z from end of write	t_{WLZ}^*	2	—	3	—	3	—	ns
Write to output in High Z	t_{WHZ}^*	—	4	—	5	—	6	ns

* These parameters are sampled and are not 100% tested

Package Dimensions—119-Bump FPBGA (Package B, Variation 1)
(Date Code: yyww.31)



Package Dimensions—119-Bump FPBGA (Package B, Variation 2)
(Date Code: yyww.3H)



Ordering Information

Part Number ¹	Package	Access Time	Temp. Range	Status
GS73024AB-8	119-Bump BGA ²	8 ns	Commercial	
GS73024AB-10	119-Bump BGA ²	10 ns	Commercial	
GS73024AB-12	119-Bump BGA ²	12 ns	Commercial	
GS73024AB-8I	119-Bump BGA ²	8 ns	Industrial	
GS73024AB-10I	119-Bump BGA ²	10 ns	Industrial	
GS73024AB-12I	119-Bump BGA ²	12 ns	Industrial	

Notes:

1. Customers requiring Tape and Reel should add the character "T" to the end of the part number. For example: GS73024AB-12T.
2. Please see pages 9 and 10 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page/Revisions/Reason
GS73024A_r1		• Creation of new datasheet
GS73024A_r1; GS73024A_r1_01	Content	<ul style="list-style-type: none"> • Corrected pinout (balls C3, C5, R2, R3, R5, R6 changed to NC) • Corrected pin description table to reflect pinout corrections • Corrected truth table to reflect pinout corrections
GS73024A_r1_01; GS73024A_r1_02	Content/Format	<ul style="list-style-type: none"> • Updated format • Added variation information to package mechanical
GS73024A_r1_02; GS73024A_r1_03	Content	<ul style="list-style-type: none"> • Added Variation 2 119 BGA to datasheet • Added date codes to mechanicals