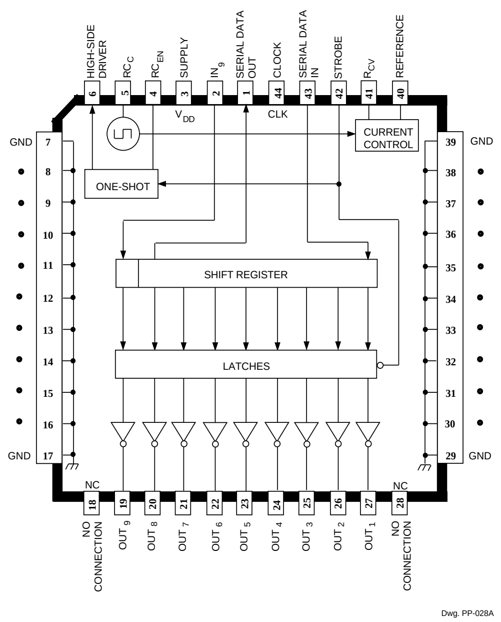
5829

Data Sheet
26185.50

9-BIT SERIAL-INPUT, LATCHED SINK DRIVER



Intended primarily to drive high-current, dot matrix 9- and 24-wire printer solenoids, the UCN5829EB serial-input, latched sink driver provides a complete driver function with a minimum external parts count. Included on chip are constant-frequency PWM current control for each output driver, a user-defined output enable timeout, current sensing, and thermal shutdown.

The 9-bit CMOS shift register and latches allow operation with most microprocessor/LSI-based systems. With a 5 V logic supply, these BiMOS devices will operate at data input rates greater than 3.3 MHz. The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, NMOS, and TTL circuits. A CMOS serial data output allows cascade connections in applications requiring additional drive lines as required for 24-wire printheads.

The device features nine open-collector Darlington drivers, each rated at 50 V and 1.6 A. Current-control for each output is provided by an internal current-sensing resistor and a constant-frequency chopper circuit. An external high-side driver can be used to optimize print head performance. It is enabled by an on-chip driver during the output enable timeout. Internal logic sequencing prevents false output operation during power up. Other high-current devices for driving dot matrix printheads are the UDN2961B/W and UDN2962W.

The UCN5829EB is supplied in a 44-lead power PLCC. Its batwing construction provides for maximum package power dissipation in a minimum-area, surface-mountable package.

ABSOLUTE MAXIMUM RATINGS

Output Current Voltage, V_{OUT} .... **50 V**

Output Current, $I_{OUT(S)}$

(Continuous) .... **1.6 A**

(Peak) .... **1.8 A**

Logic Supply Voltage, V_{DD} .... **7.0 V**

Input Voltage Range,

V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Package Power Dissipation,

P_D .... **See Graph**

Operating Temperature Range,

T_A .... **-20°C to +85°C**

Junction Temperature, T_J .... **+150°C***

Storage Temperature Range,

T_S .... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shut-down circuitry. These conditions can be tolerated, but should be avoided.

Caution: This CMOS device has input static protection but is susceptible to damage when exposed to extremely high static electrical charges.

FEATURES

- 1.6 A Continuous Output Current
- 50 V Minimum Sustaining Voltage
- Internal Current Sensing
- Constant-Frequency PWM Current Control
- Control for External High-Side Driver
- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic & Latches
- Internal Pull-Ups for TTL Compatibility
- User-Defined Output Enable Timeout
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **UCN5829EB** .

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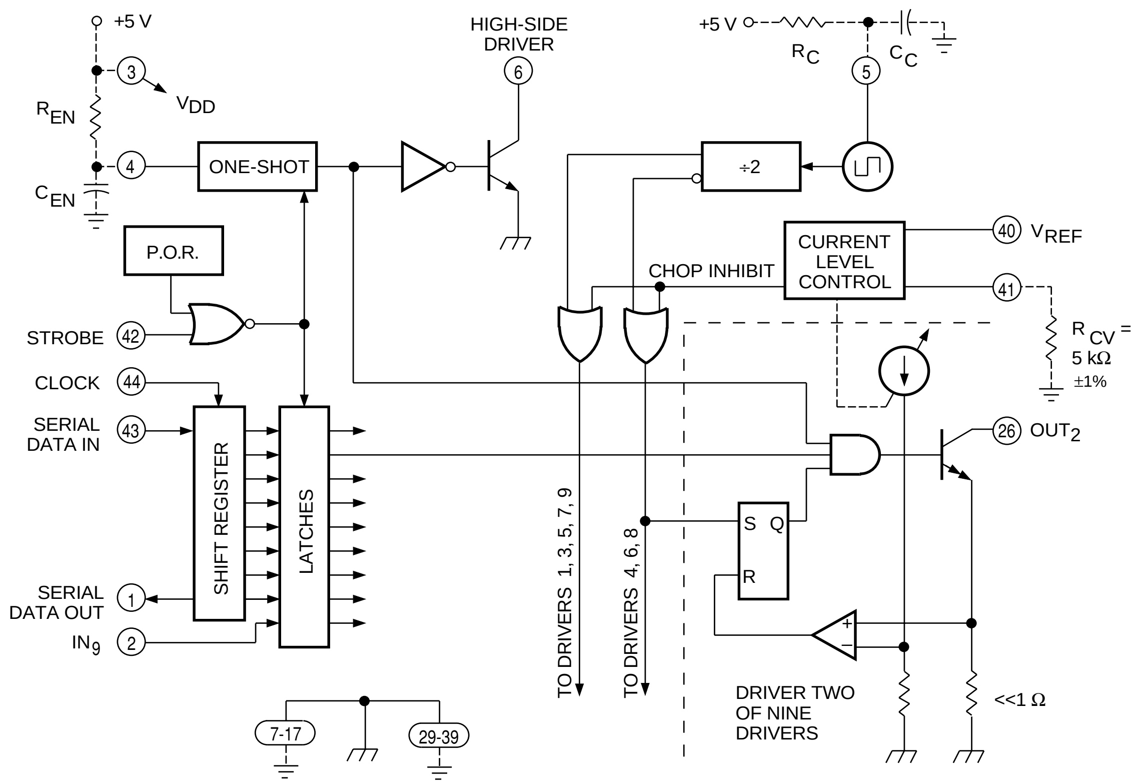
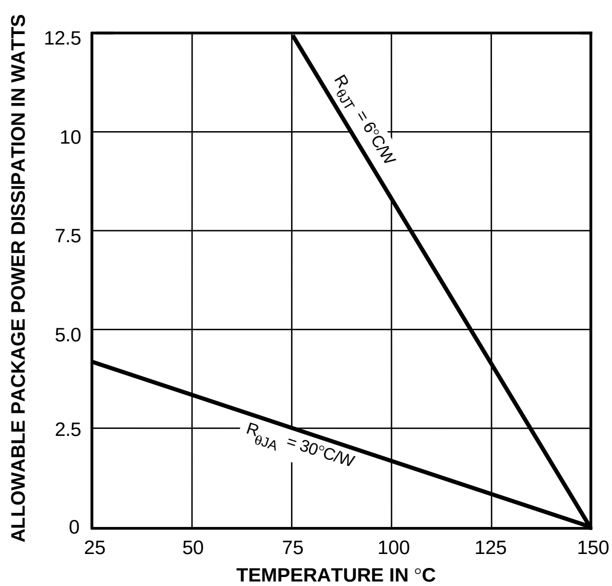
9-BIT SERIAL-INPUT, LATCHED SINK DRIVER

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-015A



Dwg. GP-020B

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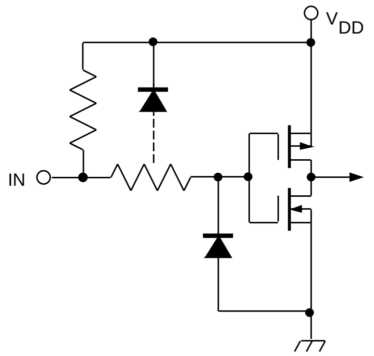
TYPICAL INPUT CIRCUITS



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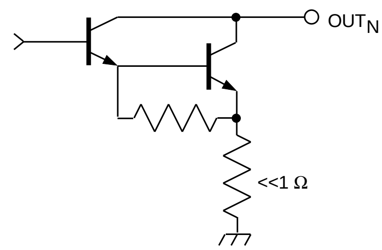
TYPICAL OUTPUT DRIVER



Dwg. EP-021-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Power Drivers (OUT_1 through OUT_9) with V_{REF} ≥4.5 V						
Output Leakage Current	I_{OUT}	V_{OUT} = 50 V	—	1.0	100	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 1.0 A	—	1.0	1.5	V
		I_{OUT} = 1.6 A	—	1.5	1.9	V
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = 1.6 A, L = 2.5 mH	50	—	—	V
Control Logic						
HSD Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 mA	—	0.5	1.0	V
Logic Input Voltage	$V_{IN(1)}$		3.5	—	5.3	V
	$V_{IN(0)}$		-0.3	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 5.0 V	—	—	1.0	µA
		V_{IN} = 0.8 V	—	-90	-180	µA
Reference Input Current	I_{REF}	V_{REF} = 3.0 V	—	500	900	µA
Logic Supply Current (V_{REF} = 2.0 V)	I_{DD}	All Drivers OFF	—	15	25	mA
		All Drivers ON, No Load	—	55	75	mA
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	MHz
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	250	—	mV
Clock to Serial Data Out Delay	t_{PD}	C_L = 30 pF	—	—	300	ns
Thermal Shutdown Temperature	T_J		—	165	—	°C

Continued next page...

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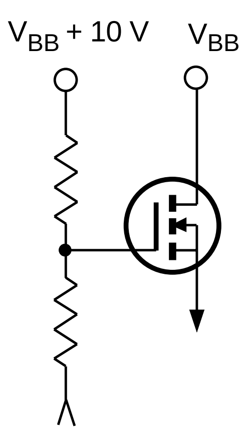
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Chopping Characteristics (T_J = +25°C to +150°C) with Fast Clamp Diodes						
Enable Timeout	t_{EN}	R_{EN} = 20 kΩ, C_{EN} = 0.01 µF	190	200	210	µs
Chopping Frequency	f_{ch}	R_C = 20 kΩ, C_C = 250 pF	90	100	110	kHz
Duty Cycle Range	dc	t_{on} / t_{on} + t_{off}	15	—	< 50	%
Chop Current Level	I_{TRIP}	V_{REF} = 2.0 V, f_{ch} < 100 kHz	0.9	1.0	1.1	A
		V_{REF} = 2.8 V, f_{ch} < 100 kHz	1.26	1.4	1.54	A
Output Current Control Range	V_{REF}		1.0	—	3.2	V
	I_{TRIP}		0.5	—	1.6	A
Delay	t_d	I_{TRIP} to $I_{OUT(P)}$, T_A = +25°C	—	300	500	ns
Chop Inhibit Voltage Range	V_{REF}		4.5	—	V_{DD} + 0.3	V

Negative current is defined as coming out of (sourcing) the specified device terminal.

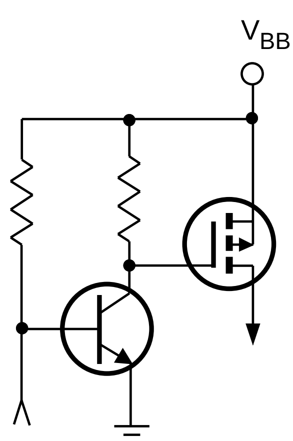
EXTERNAL HIGH-SIDE DRIVERS

NMOS



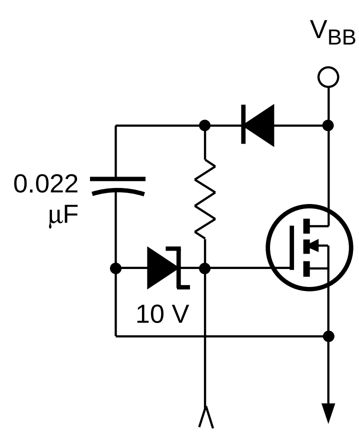
Dwg. EP-027

PMOS



Dwg. EP-028

CHARGE-PUMP CIRCUITRY FOR SINGLE-SUPPLY OPERATION



Dwg. EP-026

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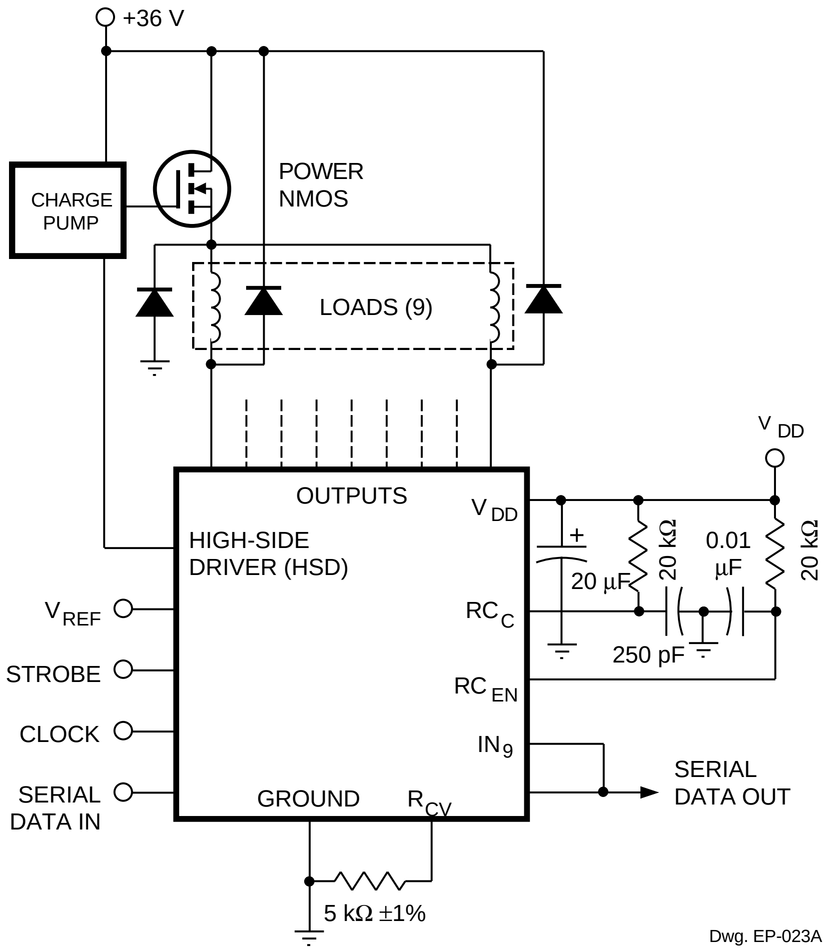
TEST CIRCUIT AND TYPICAL APPLICATION

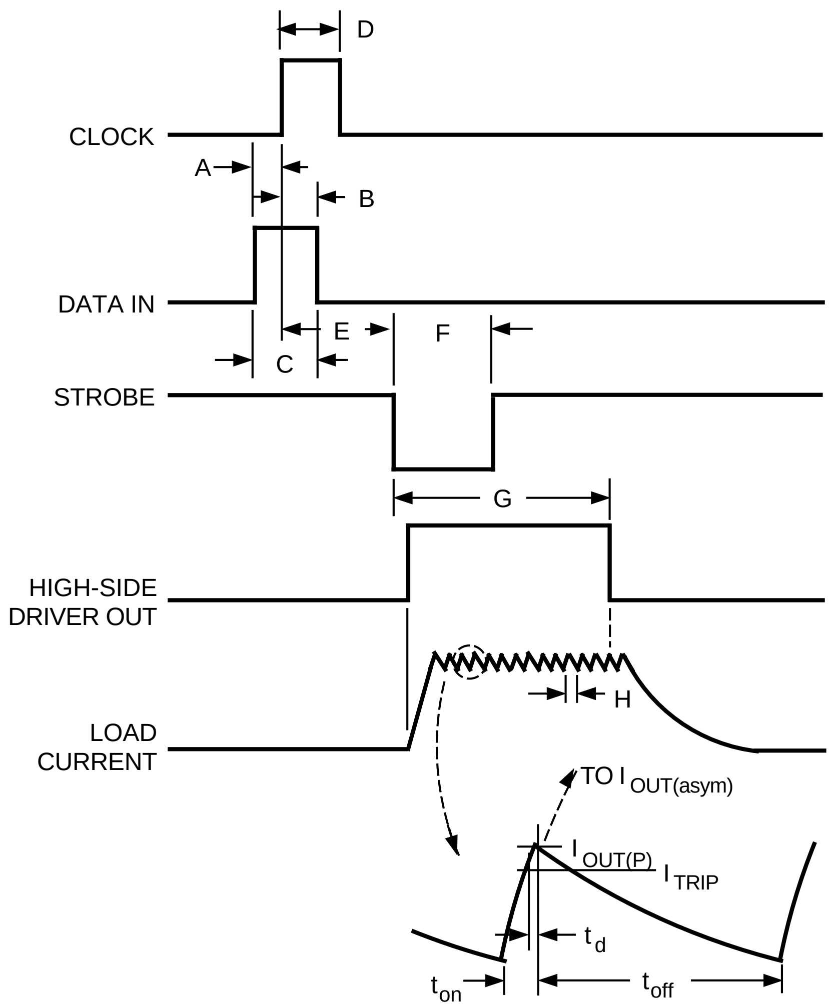


TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents* I_1 I_2 … I_9	Serial Data Output	Strobe Input	Latch Contents* I_1 I_2 … I_9	Output Contents* I_1 I_2 … I_9	HSD OUTPUT
H	↑	H R_1 … R_8	R_7	H	X	H	L
L	↑	L R_1 … R_8	R_7				
X	↓	R_1 R_2 … R_9	R_8				
		X X … X	X	H	R_1 R_2 … R_9		
		P_1 P_2 … P_9	P_8	L	P_1 P_2 … P_9	$\bar{P}_1$ $\bar{P}_2$ … $\bar{P}_9$	H

* Serial Data Output connected to $Input_9$.

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State



Dwg. WP-011A

TIMING CONDITIONS

T_A = +25°C, Logic Levels are V_{DD} and Ground

A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	**75 ns**
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	**75 ns**
C.	Minimum Data Pulse Width	**250 ns**
D.	Minimum Clock Pulse Width	**250 ns**
E.	Minimum Time Between Clock Activation and Strobe	**500 ns**
F.	Minimum Strobe Pulse Width	**500 ns**
G.	Enable Timeout, t_{EN}	**R_{EN} C_{EN}**
H.	Chop Period*, t_{on} + t_{off}	**2 R_C C_C**

* Chopping is disabled if V_{REF} is greater than 4.5 V.

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APPLICATIONS INFORMATION

The UCN5829EB is designed to drive high-current, 9- or 24-wire (3 devices cascaded) dot matrix impact printer solenoids. The internal CMOS control logic:

1) selects the operating channels from a 9- or 24-bit word previously loaded into the shift register,

2) controls the peak load current of the output drivers via nine constant-frequency switch-mode current choppers,

3) sets a user-defined print enable time, and

4) turns ON an external high-side driver during the print enable interval.

Data present at the SERIAL DATA INPUT is transferred to the shift register on the low-to-high transition of the CLOCK input pulse. The data must appear at the input prior to the rising edge of the clock input waveform. On succeeding clock pulses, the registers shift data information towards the SERIAL DATA OUTPUT. Information present at any register is transferred to its respective latch on the high-to-low transition of the STROBE (serial-to-parallel conversion). Drivers that have a logic high stored in their latch will be enabled for a set time interval (t_{EN}) generated by an internal one-shot. The output current is internally sensed and controlled in a fixed-frequency chopper format. Between strobe pulses, a new data word can be clocked in for the next print enable cycle.

PRINT ENABLE TIME

A high-to-low transition of the STROBE input starts an internal one-shot which sets the print enable time (t_{EN}) of the output drivers and the external high-side driver. The print enable time is determined by an external resistor (50 kΩ max) and capacitor (100 pF min) at RC_{EN} as

$$t_{EN} = R_{EN} C_{EN}$$

The print enable time can also be controlled from a microprocessor. In this mode, the internal one-shot is operated as an output disable function. In this mode, R_{EN} and C_{EN} are not used; instead a 10 kΩ series resistor is connected between RC_{EN} and an externally generated output disable pulse. As before, on the high-to-low STROBE transition, the outputs will be enabled. They will remain enabled until a low-to-high logic (≥3.3 V) DISABLE transition at RC_{EN}.

When operating in a continuous chopping mode, and neither print enable timeout nor output disable are desired, RC_{EN} should be grounded.

HIGH-SIDE DRIVER

To reduce the current decay time at the end of a print enable cycle, an external high-side driver can be used and controlled by the HIGH-SIDE DRIVER (HSD) output. The HSD is designed to drive an external N-channel MOSFET (with accompanying charge pump circuitry). During the print enable time (t_{EN}), the internal high-side driver is OFF, allowing the external high-side driver to be ON. If the external high-side driver is a P-channel device (eliminating the need for charge-pump circuitry), the HSD signal must be inverted for correct operation.

If an external high-side driver is used, an external ground clamp diode is also required.

OUTPUT CURRENT CONTROL

Each of the nine channels consists of a power Darlington sink driver, internal low-value current-sensing resistor, comparator, and an R/S flip-flop. The output current is sensed and controlled independently in each channel by means of a fixed-frequency chopper which sets the flip-flop and allows the output to turn ON. As the current increases in the load it is sensed by the internal sense resistor until the sense voltage equals the trip voltage of the comparator. At this time, the flip-flop is reset and the output is turned OFF. Over the range of V_{REF} = 1.0 V to 3.2 V, the output current trip point is a linear function of the reference voltage:

$$I_{TRIP} = V_{REF}/2$$

To ensure an accurate chop current level, an external 5 kΩ resistor (R_{CV}) is used. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays (typically 300 ns). After turn-off, the load current decays, circulating through the load and an external clamp diode. The output driver will stay OFF until the next chop pulse sets the flip-flop, turning ON the output, and allowing load current to rise again. The cycle repeats, maintaining the average printhead current at the desired level.

The chop pulse frequency is determined by an external resistor and capacitor at RC_C:

$$f_{ch} = \frac{1}{2\ R_C\ C_C}$$

To reduce the power supply and ground noise developed when operating nine channels synchronously, the outputs are split into two groups (OUTPUTS 2, 4, 6, 8 and OUTPUTS 1, 3, 5, 7, 9) for chopping pulses.

The chopping function is disabled when $V_{REF} > 4.5$ V. To prevent operation at higher than allowable current levels, V_{REF} should not exceed 3.2 V, except to disable the chopping function.

DUTY CYCLE LIMITS

For correct operation of the UCN5829EB, the duty cycle must be between 15% and 50% with 20% to 40% recommended. The lower limit is due to internal lockout circuitry while the upper limit guarantees synchronous operation. The duty cycle (dc) can be calculated as

$$dc = \frac{t_{on}}{t_{on} + t_{off}} \approx \frac{I_{OUT(P)} / I_{OUT(asym)} + v_d / v_c}{1 + v_d / v_c}$$

where $I_{OUT(asym)}$ = the asymptotic current value = v_c/R_L

v_d = discharge voltage across the load = $V_{HSD} + V_{DIODE}$

v_c = charge voltage across the load = $V_{BB} - V_{OUT(SAT)} - V_{HSD}$

For most practical cases, correct operation can be achieved if

$I_{OUT(asym)} / I_{OUT(P)} > 2.5$.

GENERAL

For applications with 9-wire printheads, SERIAL DATA OUT should be connected to IN_9. For 24-wire printhead applications, three devices (eight channels per device) are cascaded by connecting SERIAL DATA OUT to the next SERIAL DATA IN.

Each of the CMOS logic inputs have internal pull-up resistors for TTL compatibility.

An external transient-protection flyback diode is required at each output. Fast recovery diodes are recommended to reduce power dissipation in the UCN5829EB. Internal filtering prevents false triggering of the current sense comparator which can be caused by the recovery current spike of the diodes when the outputs turn ON.

The SUPPLY terminal should be well decoupled with a capacitor placed as close as possible to the device. Internal power-ON reset circuitry prevents false output triggering during power up.

Thermal protection circuitry is activated and turns OFF all drivers at a junction temperature of typically +165°C. The thermal shutdown is independent of all other functions. It should not be used as another control input but is intended only to protect the chip from catastrophic failures due to excessive junction temperatures. The output drivers are re-enabled when the junction temperature cools down to approximately +145°C.

TYPICAL APPLICATION

Shown is a typical application with the UCN5829EB controlling a chop current of 1 A through a 3 mH, 9 Ω load. To check the duty cycle and $I_{OUT(asym)}/I_{OUT(P)}$ restrictions

where $v_d = V_{HSD} + V_{DIODE} \approx 1.5 + 1.5 = 3$

$v_c = V_{BB} - V_{OUT(SAT)} - V_{HSD} = 36 - 1.5 - 1.5 = 33$

$I_{OUT(asym)} = v_c / R_L = 33 / 9 = 3.67$

then $I_{OUT(asym)} / I_{OUT(P)} = 3.67 / 1 = 3.67$

The condition of $I_{OUT(asym)} / I_{OUT(P)} > 2.5$ is met and the duty cycle will be within the proscribed limits. The actual duty cycle is

$$dc = \frac{I_{OUT(P)} / I_{OUT(asym)} + v_d/v_c}{1 + v_d/v_c} = \frac{1.0/3.67 + 2.5/33}{1 + 2.5/33} = 32\%$$

For a 50 kHz chopping frequency and a 250 µs print enable time, the remaining component values are

with $C_C = 250$ pF and $C_{EN} = 0.01$ µF

then $R_C = 1/(2\ f_{ch}\ C_C) = 1/(2 \times 50 \times 10^3 \times 250 \times 10^{-12}) = 40$ kΩ

and $R_{EN} = t_{EN} / C_{EN} = 250 \times 10^{-6} / 10 \times 10^{-9} = 25$ kΩ

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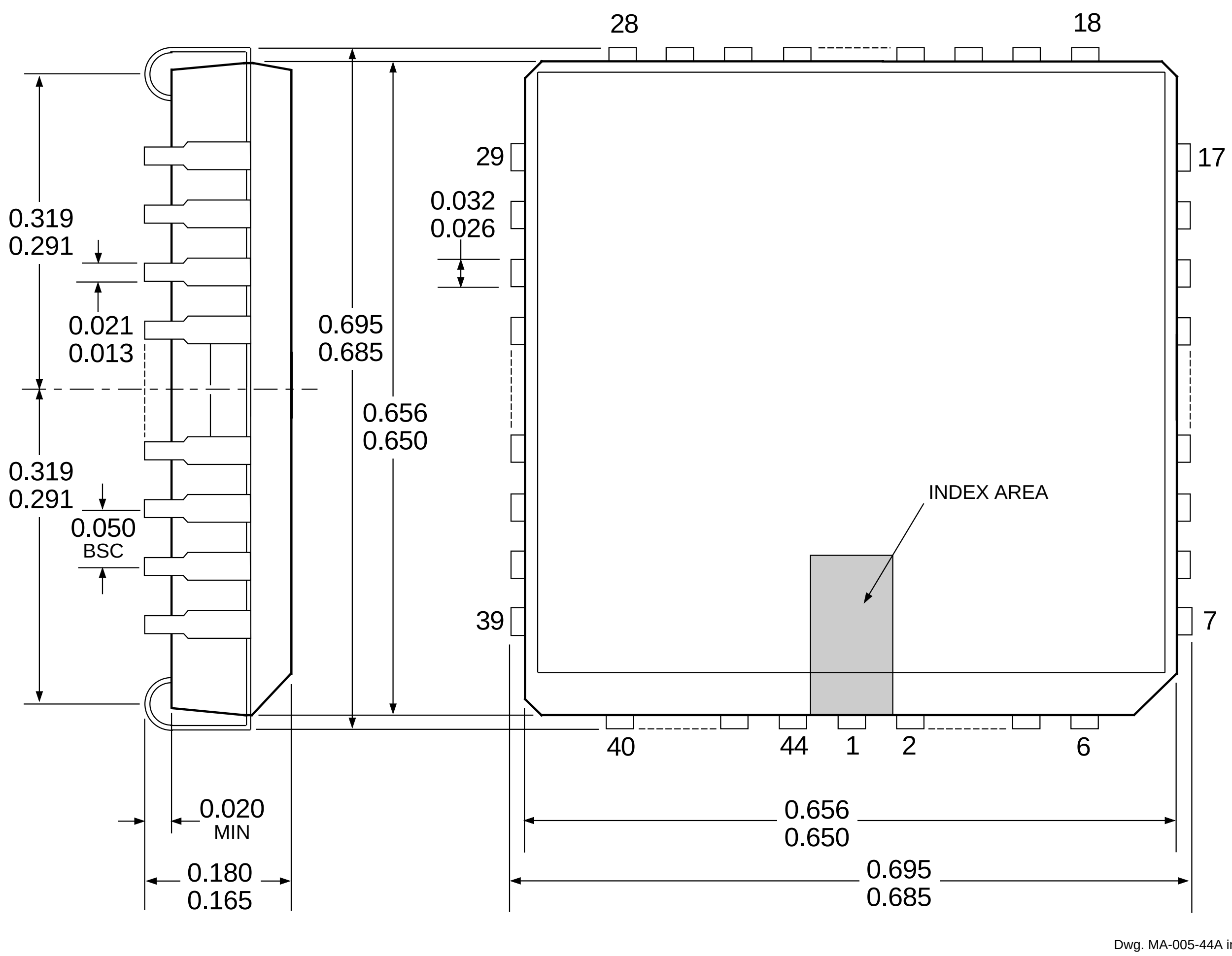
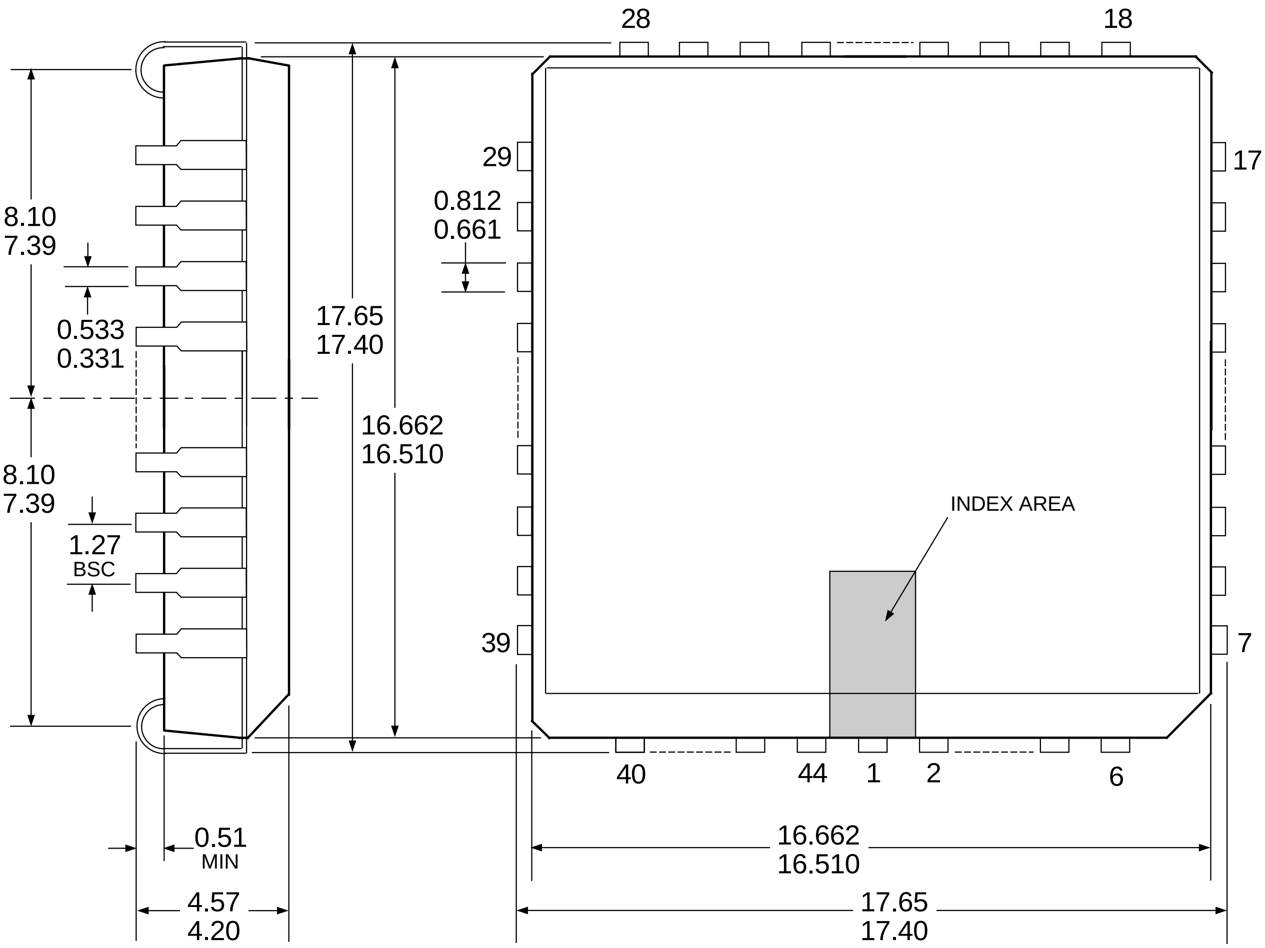
Dimensions in Inches
(controlling dimensions)



NOTES: 1. Webbed lead frame. Leads 7 through 17 and 29 through 39 are internally one piece.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead spacing tolerance is non-cumulative.

5829
9-BIT SERIAL-INPUT, LATCHED SINK DRIVER

Dimensions in Millimeters
(for reference only)



Dwg. MA-005-44A mm

NOTES: 1. Webbed lead frame. Leads 7 through 17 and 29 through 39 are internally one piece.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead spacing tolerance is non-cumulative.

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