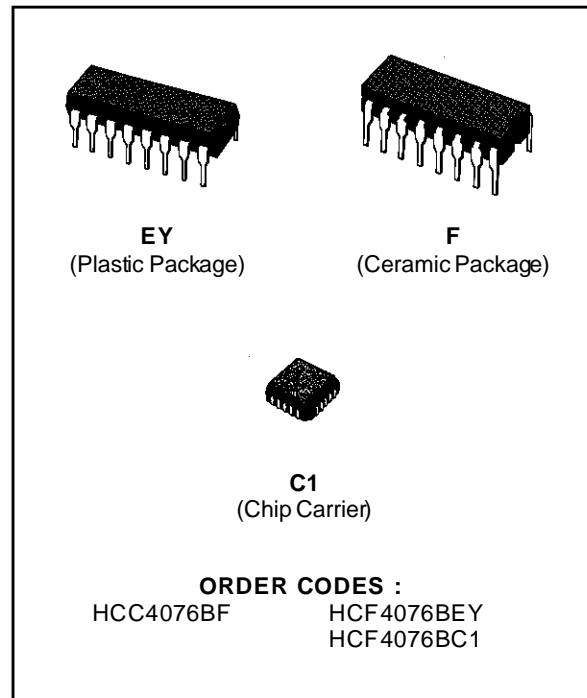


BCD RATE MULTIPLEXER

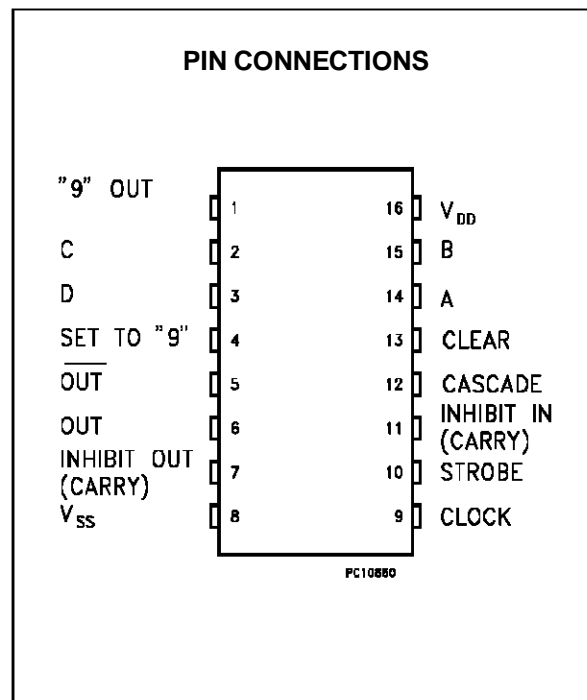
- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



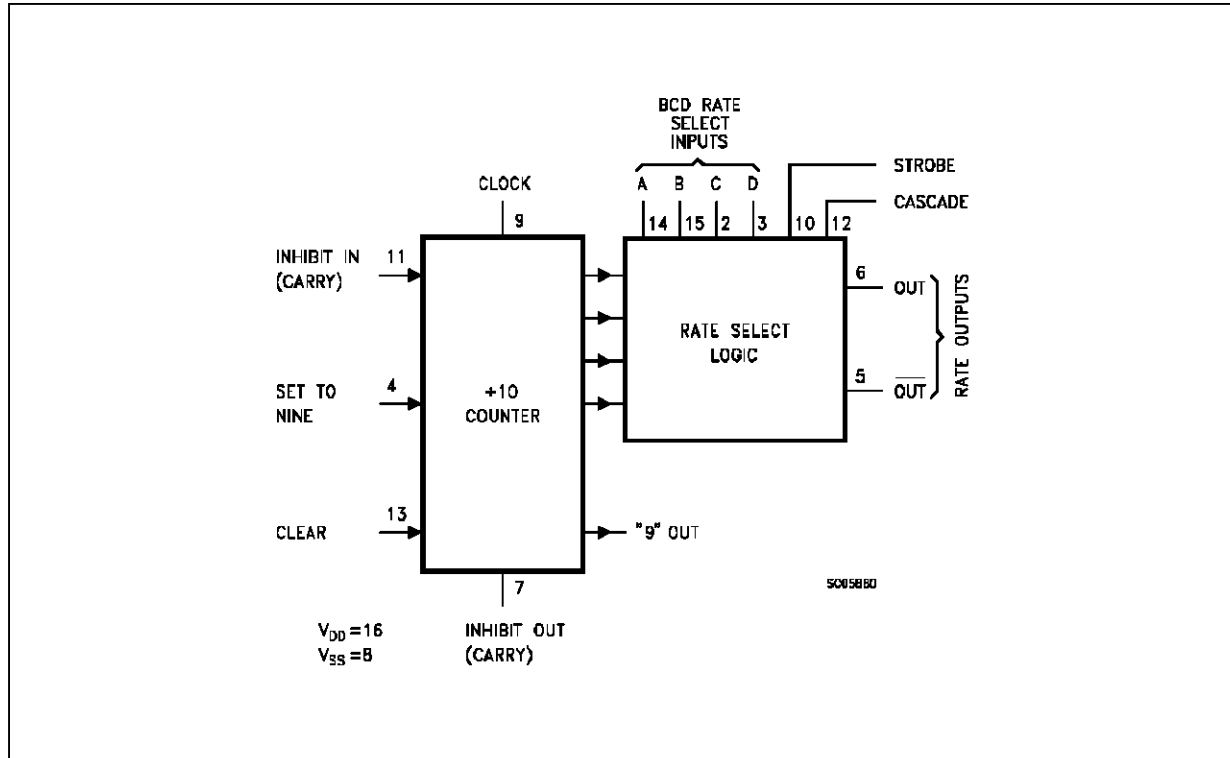
DESCRIPTION

The **HCC4527B** (extended temperature range) and **HCF4527B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in line plastic or ceramic package.

The **HCC/HCF4527B** is a low power 4 bit digital rate multiplier that provides an output pulse rate which is the clock input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric func-



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{DD} *	Supply Voltage: HCC Types HCF Types	-0.5 to +20 -0.5 to +18	V
V _i	Input Voltage	-0.5 to V _{DD} + 0.5	V
I _i	DC Input Current (any one input)	± 10	mA
P _{tot}	Total Power Dissipation (per package)	200	mW
	Dissipation per Output Transistor for Top = Full Package Temperature Range	100	mW
T _{op}	Operating Temperature: HCC Types HCF Types	-55 to +125 -40 to +85	°C
T _{stg}	Storage Temperature	-65 to +150	°C

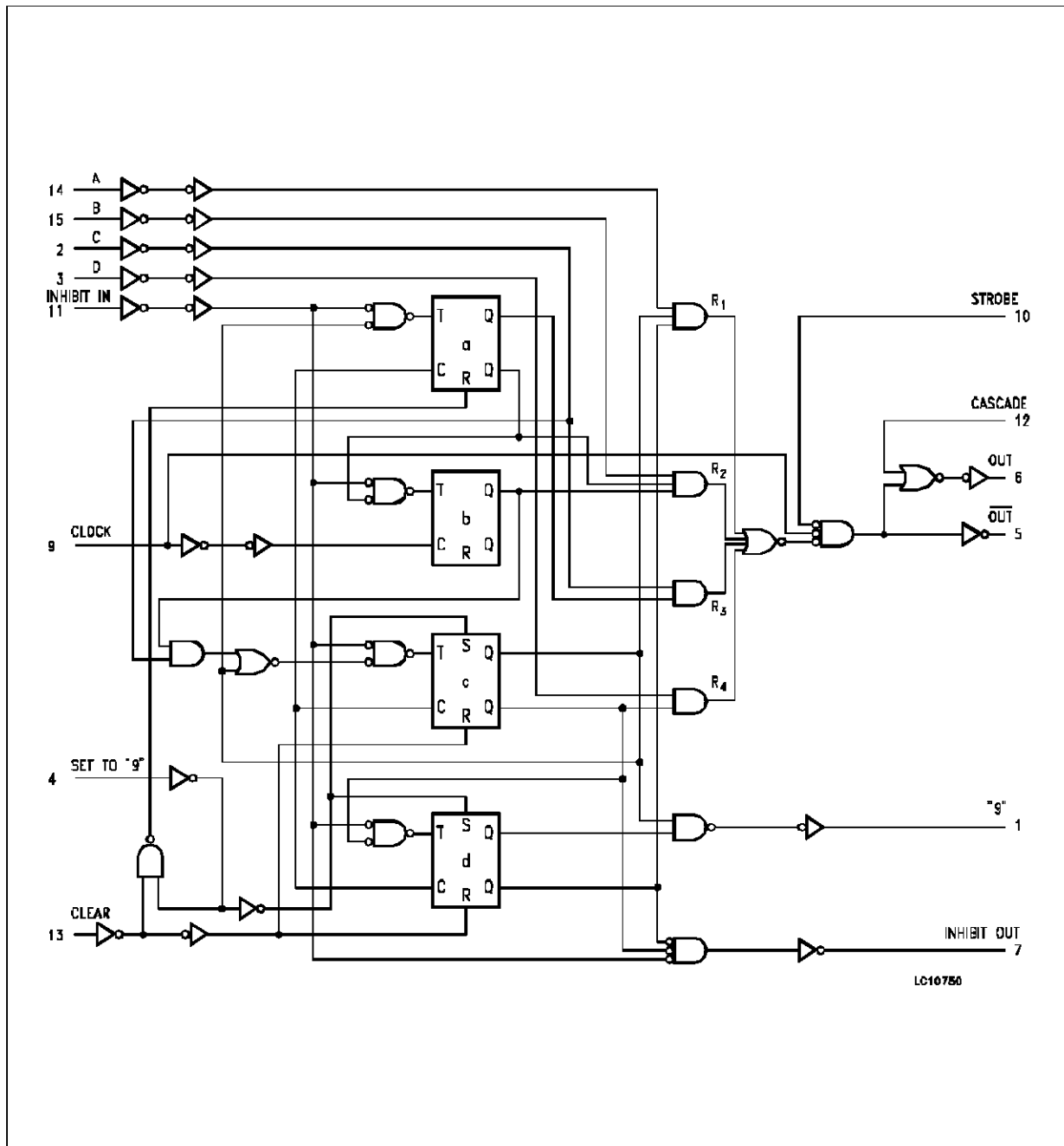
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage: HCC Types HCF Types	3 to 18 3 to 15	V
V _i	Input Voltage	0 to V _{DD}	V
T _{op}	Operating Temperature: HCC Types HCF Types	-55 to +125 -40 to +85	°C

LOGIC DIAGRAM



TRUTH TABLE

Inputs										Outputs			
Number of Pulsed or Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = LOW; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{\text{OUT}}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	■	■	H	■
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	●	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

● Output same as the first 16 lines of this truth table (depending on value of A, B, C, D)

■ Depends on internal state of counter.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW} *		25 °C			T _{HIGH} *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent Current	HCC Types	0/5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
V _{OH}	Output High Voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V _{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V _{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V _{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I _{OH}	Output Drive Current	HCC Types	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF Types	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.53		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input Leakage Current		0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
			0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	μ A
C _I	Input Capacitance		Any Input						5	7.5			pF	

* T_{LOW} = -55 °C for HCC device; -40 °C for HCF device.* T_{HIGH} = +125 °C for HCC device; +85 °C for HCF device.The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V

HCC/HCF4527B

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$, typical temperature coefficient for all V_{DD} values is $03\text{ } \%/^{\circ}\text{C}$, all input rise and fall times = 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to Output)		5		110	220	ns
			10		55	110	
			15		45	90	
t_{PLH} t_{PHL}	Propagation Delay Time Clock or Strobe to Output		5		150	300	ns
			10		75	150	
			15		60	120	
t_{PLH}	Propagation Delay Time Clock to Inhibit Output		5		320	640	ns
			10		145	290	
			15		100	200	
t_{PHL}	Propagation Delay Time Clock to Inhibit Output		5		250	500	ns
			10		100	200	
			15		75	150	
t_{PLH} t_{PHL}	Propagation Delay Time Clear to Output		5		380	760	ns
			10		175	550	
			15		130	260	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to "9" or "1" Q Output		5		300	600	ns
			10		125	250	
			15		90	180	
t_{PLH} t_{PHL}	Propagation Delay Time Cascade to Output		5		90	180	ns
			10		45	90	
			15		35	70	
t_{PLH} t_{PHL}	Propagation Delay Time Inhibit Input to Inhibit Output		5		130	260	ns
			10		60	120	
			15		45	90	
t_{PLH} t_{PHL}	Propagation Delay Time Set to Output		5		330	660	ns
			10		150	300	
			15		110	220	
t_{THL} t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{CL}	Maximum Clock Frequency		5	1.2	2.4		MHz
			10	2.5	5		
			15	3.5	7		
t_w	Clock Pulse Width		5	330	165		ns
			10	170	85		
			15	100	50		
t_r, t_f	Clock Rise or Fall Time		5			15	μs
			10			15	
			15			15	
t_w	Set or Clear Pulse Width		5	160	80		ns
			10	90	45		
			15	60	30		
t_{setup}	Inhibit Input Setup Time		5	100	50		ns
			10	40	20		
			15	20	10		

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Value			Unit
			V _{DD} (V)	Min.	Typ.	Max.	
t _R	Inhibit Input Removal Time		5	240	120		ns
			10	130	65		
			15	110	55		
t _R	Set Remova Time		5	150	75		ns
			10	80	40		
			15	50	25		
t _R	Clear Removal Time		5	60	30		ns
			10	40	20		
			15	30	15		

APPLICATION NOTE

For fractional multipliers with more than one digit, HCC/HCF4527B devices may be cascaded in two different modes: the Add mode and the Mltiply mode (see figures 1 and 2).

When two units are cascaded in Add mode and programmed to 9 and 4 respectively, the more significant unit will have 9 output pulses for every 10 input pulses and the other unit will have 4 output pulses for every 100 input pulses for a total of:

$$\frac{9}{10} + \frac{4}{100} = \frac{94}{100}$$

In the multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one:

If N₁ = 9 and N₂ = 4

$$f_{out2} = \frac{4}{10} f_{out1}$$

$$f_{out1} = \frac{9}{10} f_{clock}$$

$$f_{out2} = \frac{4}{10} \times \left(\frac{9}{10} f_{clock} \right) = \frac{36}{100} f_{clock}$$

Therefore 36 output pulses for every 100 clock input pulses.

HCC/HCF4527B

Fig. 1: Two HCC/HCF4527B Cascaded in The "Add" Mode With a Preset Number

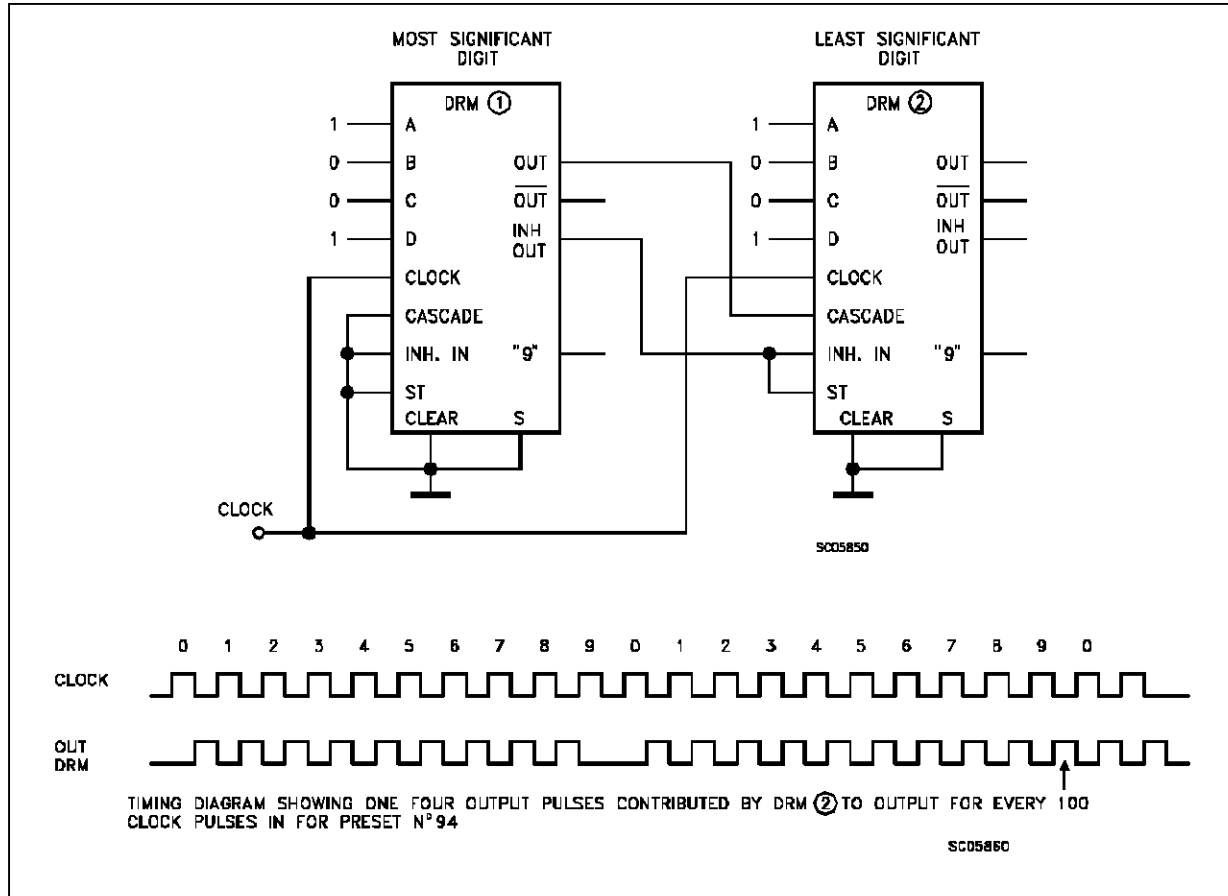


Fig. 2: Two HCC/HCF4527B Cascaded in The "Multiply" Mode With a Preset Number

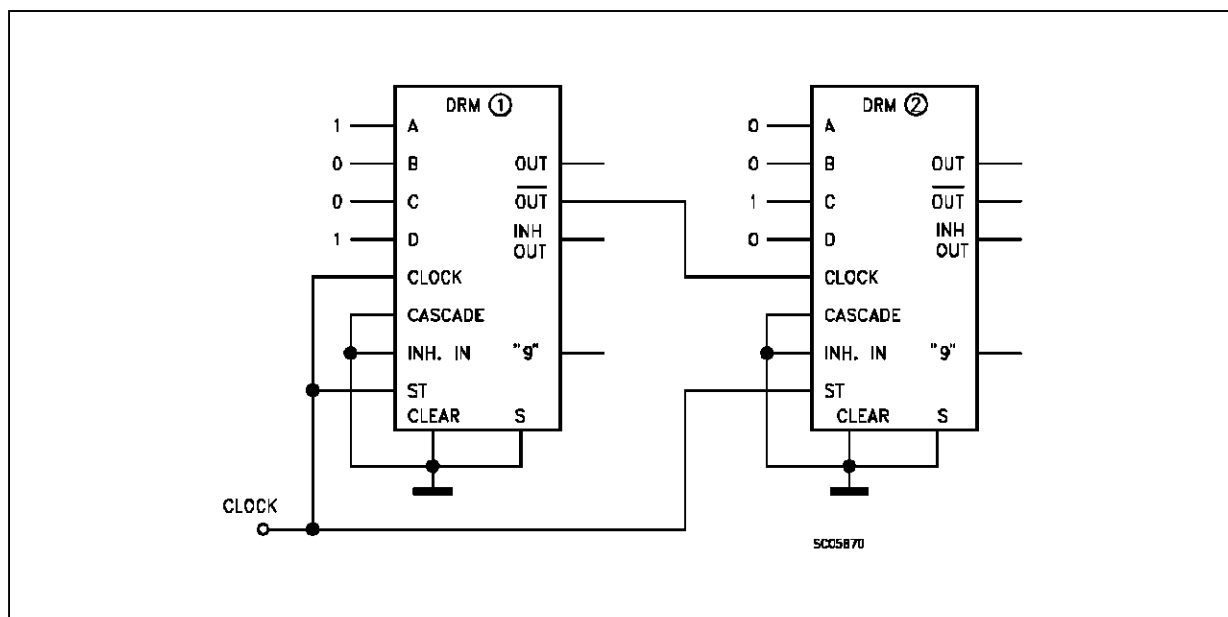
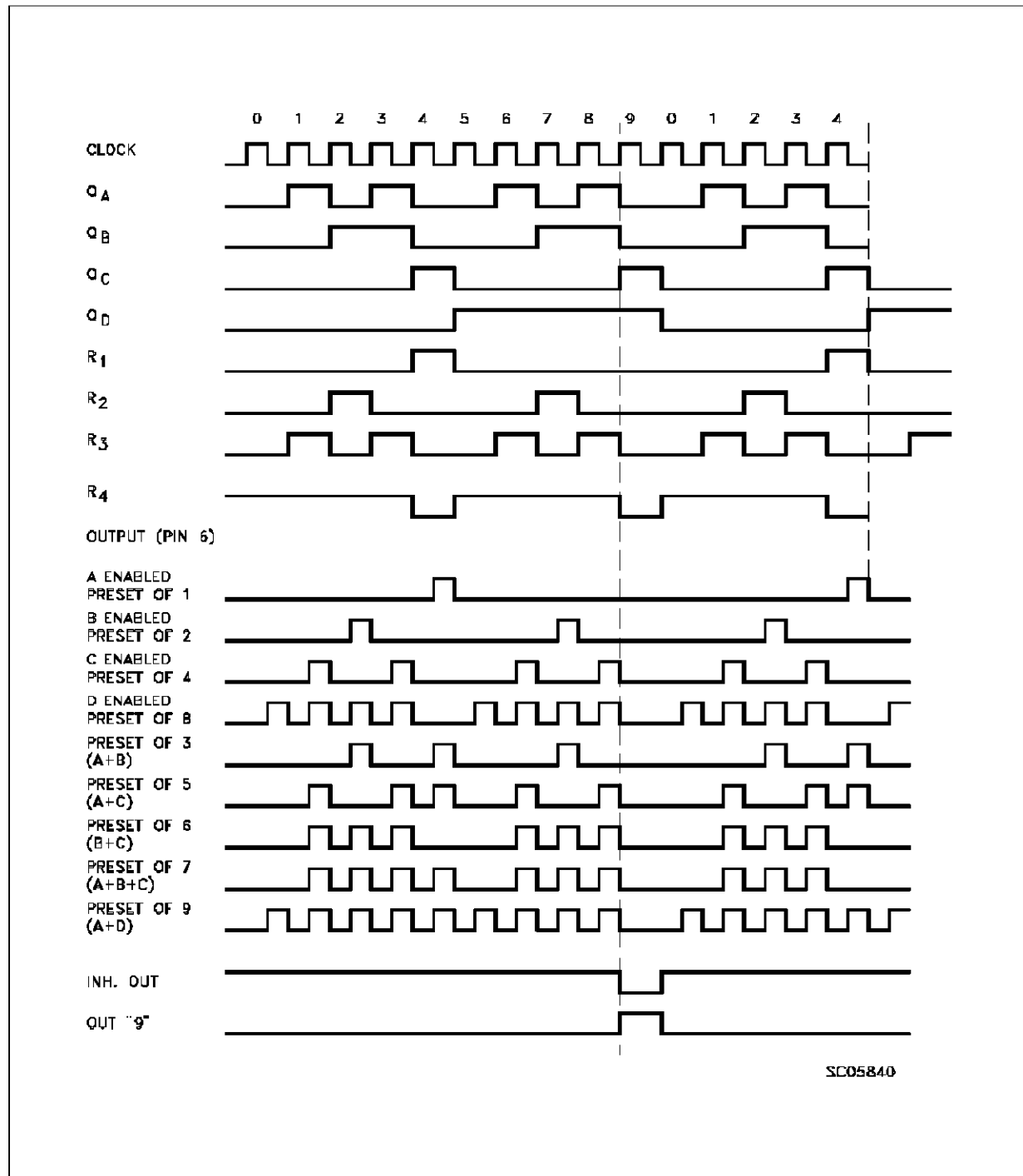


Fig. 3: Timing Diagram (see Logic Diagram)



Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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