PC100 Unbuffered DIMM(168pin)
SPD Specification(64Mb D-die base)

Rev. 0.1

Jan. 2000

M366S0424DTS-C80/C1H/C1L

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632D-TC80/ TC1H/ TC1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuration type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DEh	04h	34h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M366S0823DTS-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuration type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M374S0823DTS-C80/C1H/C1L

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuration type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F1h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
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