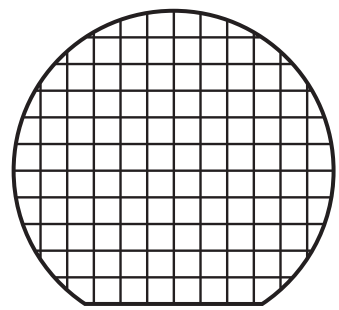
SRIX4K

13.56 MHz short-range contactless memory chip with 4096-bit EEPROM, anticollision and anti-clone functions

Features

- ISO 14443-2 Type B air interface compliant
- ISO 14443-3 Type B frame format compliant
- 13.56 MHz carrier frequency
- 847 kHz subcarrier frequency
- 106 Kbit/second data transfer
- France Telecom proprietary anti-clone function
- 8 bit Chip_ID based anticollision system
- 2 count-down binary counters with automated antitearing protection
- 64-bit unique identifier
- 4096-bit EEPROM with write protect feature
- Read_block and Write_block (32 bits)
- Internal tuning capacitor
- 1million erase/write cycles
- 40-year data retention
- Self-timed programming cycle
- 5 ms typical programming time



– Unsawn wafer
– Bumped and sawn wafer

Contents

List of tables

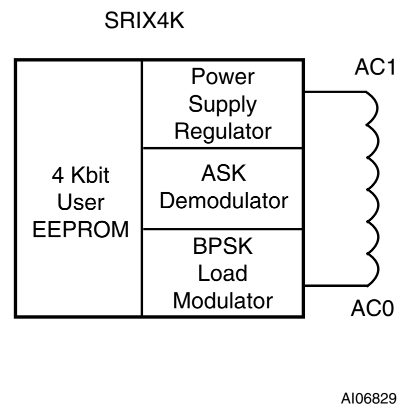
List of figures

1 Description

The SRIX4K is a contactless memory, powered by an externally transmitted radio wave. It contains a 4096-bit user EEPROM fabricated with STMicroelectronics CMOS technology. The memory is organized as 128 blocks of 32 bits. The SRIX4K is accessed via the 13.56 MHz carrier. Incoming data are demodulated and decoded from the received amplitude shift keying (ASK) modulation signal and outgoing data are generated by load variation using bit phase shift keying (BPSK) coding of a 847 kHz subcarrier. The received ASK wave is 10% modulated. The data transfer rate between the SRIX4K and the reader is 106 Kbit/s in both reception and emission modes.

The SRIX4K follows the ISO 14443-2 Type B recommendation for the radio-frequency power and signal interface.

Figure 1. Logic diagram



The SRIX4K is specifically designed for short range applications that need secure and re-usable products. The SRIX4K includes an anticollision mechanism that allows it to detect and select tags present at the same time within range of the reader. The anticollision is based on a probabilistic scanning method using slot markers. The SRIX4K provides an anti-clone function which allows its authentication. Using the STMicroelectronics single chip coupler, CRX14, it is easy to design a reader with the authentication capability and to build a system with a high level of security.

Table 1. Signal names

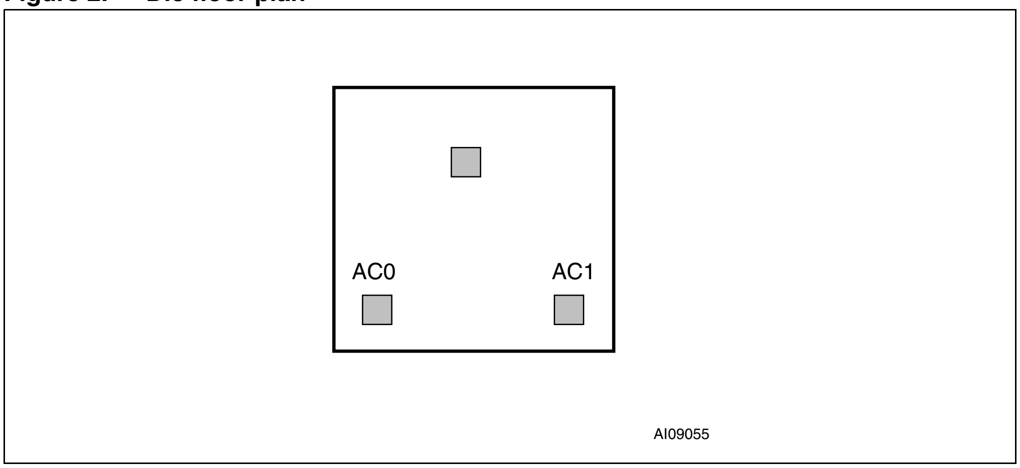
Signal name	Description
AC1	Antenna coil
AC0	Antenna coil

The SRIX4K contactless EEPROM can be randomly read and written in block mode (each block containing 32 bits). The instruction set includes the following ten commands:

- Read_block
- Write_block
- Initiate
- Pcall16
- Slot_marker
- Select
- Completion
- Reset_to_inventory
- Authenticate
- Get_UID

The SRIX4K memory is organized in three areas, as described in *Figure 12*. The first area is a resettable OTP (one time programmable) area in which bits can only be switched from 1 to 0. Using a special command, it is possible to erase all bits of this area to 1. The second area provides two 32-bit binary counters which can only be decremented from FFFF FFFFh to 0000 0000h, and gives a capacity of 4,294,967,296 units per counter. The last area is the EEPROM memory. It is accessible by block of 32 bits and includes an auto-erase cycle during each Write_block command.

Figure 2. Die floor plan



2 Signal description

2.0.1 AC1, AC0

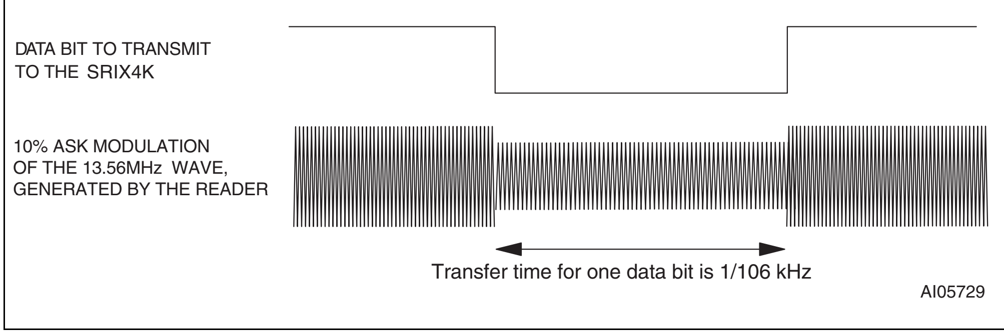
The pads for the antenna coil. AC1 and AC0 must be directly bonded to the antenna.

3 Data transfer

3.1 Input data transfer from the reader to the SRIX4K (request frame)

The reader must generate a 13.56 MHz sinusoidal carrier frequency at its antenna, with enough energy to “remote-power” the memory. The energy received at the SRIX4K’s antenna is transformed into a supply voltage by a regulator, and into data bits by the ASK demodulator. For the SRIX4K to decode correctly the information it receives, the reader must 10% amplitude-modulate the 13.56 MHz wave before sending it to the SRIX4K. This is represented in *Figure 3*. The data transfer rate is 106 Kbits/s.

Figure 3. 10% ASK modulation of the received wave



3.1.1 Character transmission format for request frame

The SRIX4K transmits and receives data bytes as 10-bit characters, with the least significant bit (b_0) transmitted first, as shown in *Figure 4*. Each bit duration, an ETU (elementary time unit), is equal to 9.44 µs (1/106 kHz).

These characters, framed by a start of frame (SOF) and an end of frame (EOF), are put together to form a command frame as shown in *Figure 10*. A frame includes an SOF, commands, addresses, data, a CRC and an EOF as defined in the ISO 14443-3 Type B Standard. If an error is detected during data transfer, the SRIX4K does not execute the command, but it does not generate an error frame.

Figure 4. SRIX4K request frame character format

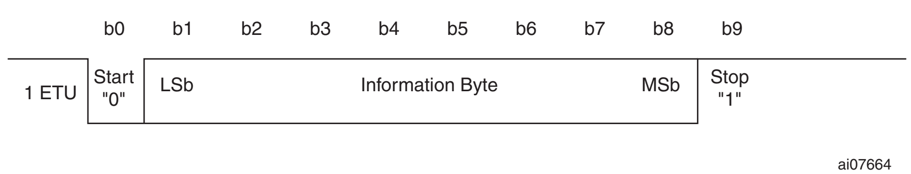


Table 2. Bit description

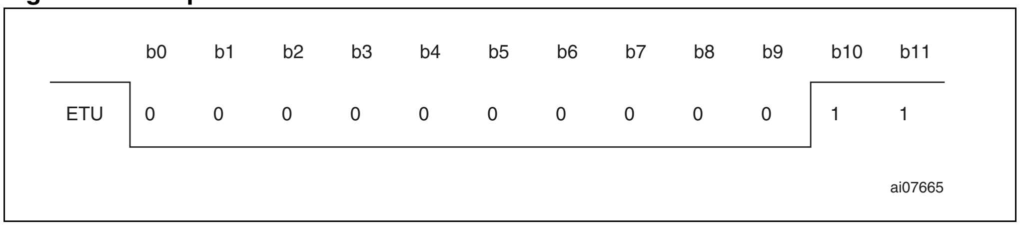
Bit	Description	Value
b_0	Start bit used to synchronize the transmission	$b_0 = 0$
b_1 to b_8	Information byte (command, address or data)	The information byte is sent with the least significant bit first
b_9	Stop bit used to indicate the end of a character	$b_9 = 1$

3.1.2 Request start of frame

The SOF described in *Figure 5* is composed of:

- one falling edge,
- followed by 10 ETUs at logic-0,
- followed by a single rising edge,
- followed by at least 2 ETUs (and at most 3) at logic-1.

Figure 5. Request start of frame

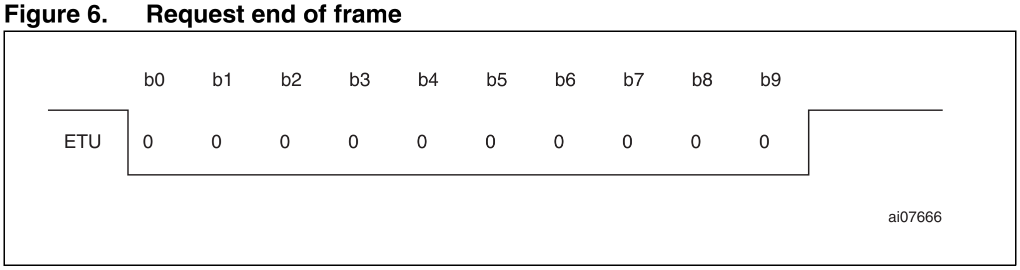


3.1.3 Request end of frame

The EOF shown in *Figure 6* is composed of:

- one falling edge,
- followed by 10 ETUs at logic-0,
- followed by a single rising edge.

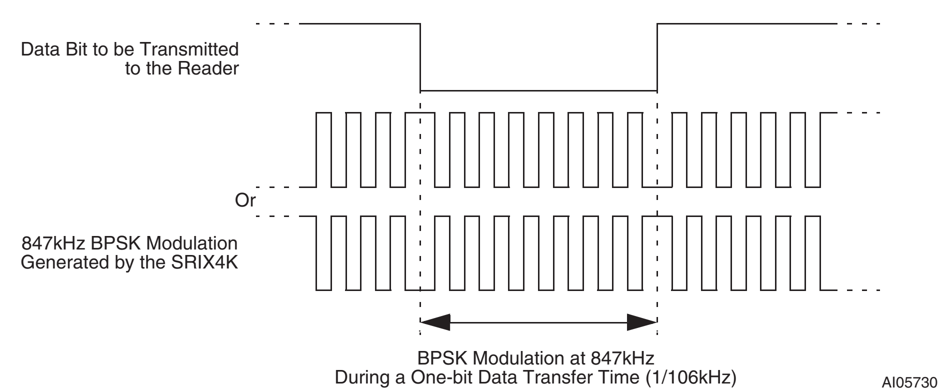
Figure 6. Request end of frame



3.2 Output data transfer from the SRIX4K to the reader (answer frame)

The data bits issued by the SRIX4K use retro-modulation. Retro-modulation is obtained by modifying the SRIX4K current consumption at the antenna (load modulation). The load modulation causes a variation at the reader antenna by inductive coupling. With appropriate detector circuitry, the reader is able to pick up information from the SRIX4K. To improve load-modulation detection, data is transmitted using a BPSK encoded, 847 kHz subcarrier frequency f_S as shown in *Figure 7*, and as specified in the ISO 14443-2 Type B Standard.

Figure 7. Wave transmitted using BPSK subcarrier modulation



3.2.1 Character transmission format for answer frame

The character format is the same as for input data transfer (*Figure 4*). The transmitted frames are made up of an SOF, data, a CRC and an EOF (*Figure 10*). As with an input data transfer, if an error occurs, the reader does not issue an error code to the SRIX4K, but it should be able to detect it and manage the situation. The data transfer rate is 106 Kbits/second.

3.2.2 Answer start of frame

The SOF described in *Figure 8* is composed of:

- followed by 10 ETUs at logic-0
- followed by 2 ETUs at logic-1

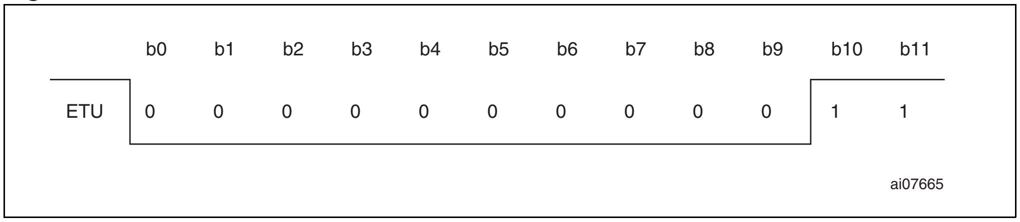
Figure 8. Answer start of frame

3.2.3 Answer end of frame

The EOF shown in *Figure 9* is composed of:

- followed by 10 ETUs at logic-0,
- followed by 2 ETUs at logic-1.

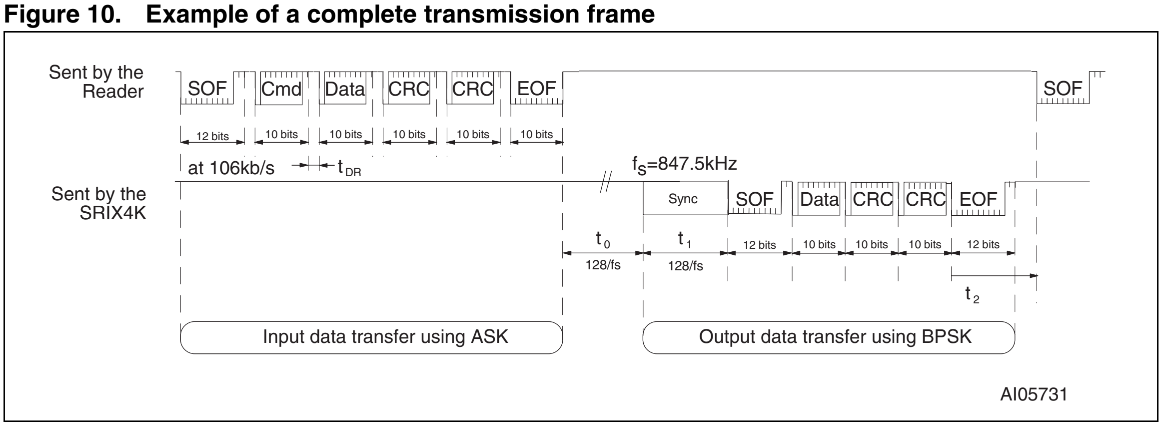
Figure 9. Answer end of frame



3.3 Transmission frame

Between the request data transfer and the Answer data transfer, all ASK and BPSK modulations are suspended for a minimum time of $t_0 = 128/f_S$. This delay allows the reader to switch from Transmission to Reception mode. It is repeated after each frame. After t_0, the 13.56 MHz carrier frequency is modulated by the SRIX4K at 847 kHz for a period of $t_1 = 128/f_S$ to allow the reader to synchronize. After t_1, the first phase transition generated by the SRIX4K forms the start bit ('0') of the Answer SOF. After the falling edge of the Answer EOF, the reader waits a minimum time, t_2, before sending a new request frame to the SRIX4K.

Figure 10. Example of a complete transmission frame



3.4 CRC

The 16-bit CRC used by the SRIX4K is generated in compliance with the ISO 14443 Type B recommendation. For further information, please see *Appendix A*. The initial register contents are all 1s: FFFFh.

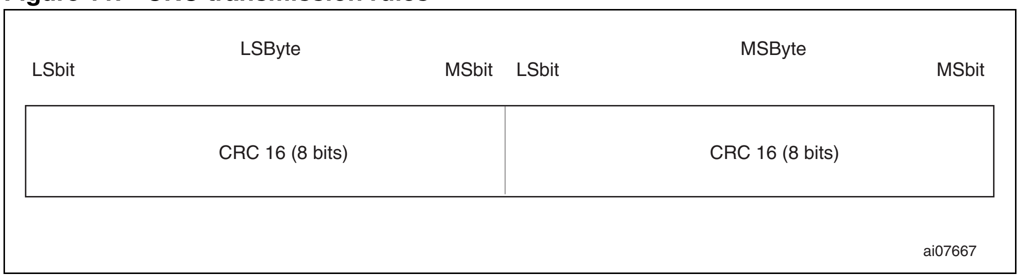
The two-byte CRC is present in every request and in every answer frame, before the EOF. The CRC is calculated on all the bytes between SOF (not included) and the CRC field.

Upon reception of a request from a reader, the SRIX4K verifies that the CRC value is valid. If it is invalid, the SRIX4K discards the frame and does not answer the reader.

Upon reception of an Answer from the SRIX4K, the reader should verify the validity of the CRC. In case of error, the actions to be taken are the reader designer's responsibility.

The CRC is transmitted with the least significant byte first and each byte is transmitted with the least significant bit first.

Figure 11. CRC transmission rules



4 Memory mapping

The SRIX4K is organized as 128 blocks of 32 bits as shown in *Figure 12*. All blocks are accessible by the Read_block command. Depending on the write access, they can be updated by the Write_block command. A Write_block updates all the 32 bits of the block.

Figure 12. SRIX4K memory mapping

Block Addr	Msb b_{31} b_{24}	32-bit block b_{23} b_{16} b_{15} b_8	b_7 Lsb b_0	Description
0	32 bits Boolean area			Resettable OTP bits
1	32 bits Boolean area			
2	32 bits Boolean area			
3	32 bits Boolean area			
4	32 bits Boolean area			
5	32 bits binary counter			Count down counter
6	32 bits binary counter			
7	User area			Lockable EEPROM
8	User area			
9	User area			
10	User area			
11	User area			
12	User area			
13	User area			
14	User area			
15	User area			
16	User area			EEPROM
...	User area			
127	User area			
255	OTP_Lock_Reg	ST Reserved	Fixed Chip_ID (Option)	System OTP bits
UID0	64 bits UID area			ROM
UID1				

4.1 Resettable OTP area

In this area contains five individual 32-bit Boolean words (see *Figure 13* for a map of the area). A Write_block command will not erase the previous contents of the block as the write cycle is not preceded by an auto-erase cycle. This feature can be used to reset selected bits from 1 to 0. All bits previously at 0 remain unchanged. When the 32 bits of a block are all at 0, the block is empty, and cannot be updated any more. See *Figure 14* and *Figure 15* for examples of the result of the Write_block command in the resettable OTP area.

Figure 13. Resettable OTP area (addresses 0 to 4)

Block address	MSb b31 … b24 b23 … 32-bit block b16 b15 … b8 b7 … LSb b0	Description
0	32-bit Boolean area	Resettable OTP bit
1	32-bit Boolean area	
2	32-bit Boolean area	
3	32-bit Boolean area	
4	32-bit Boolean area	

ai07657b

Figure 14. Write_block update in Standard mode (binary format)

	b31														b0
Previous data stored in block	1	...	1	**1**	0	1	0	1	1	**1**	**1**	1	**0**	1	1
Data to be written	1	...	1	**0**	0	1	0	1	1	**0**	**0**	1	**1**	1	1
New data stored in block	1	...	1	**0**	0	1	0	1	1	**0**	**0**	1	**0**	1	1

ai07658

The five 32-bit blocks making up the resettable OTP area can be erased in one go by adding an auto-erase cycle to the Write_block command. An auto-erase cycle is added each time the SRIX4K detects a Reload command. The Reload command is implemented through a specific update of the 32-bit binary counter located at block address 6 (see *Section 4.2: 32-bit binary counters* for details).

Figure 15. Write_block update in Reload mode (binary format)

	b31														b0
Previous data stored in block	1	...	1	1	**0**	1	0	1	1	**1**	**1**	1	**0**	1	1
Data to be written	1	...	1	1	**1**	1	0	1	1	**0**	**0**	1	**1**	1	1
New data stored in block	1	...	1	1	**1**	1	0	1	1	**0**	**0**	1	**1**	1	1

ai07659

4.2 32-bit binary counters

The two 32-bit binary counters located at block addresses 5 and 6, respectively, are used to count down from 2^{32} (4096 million) to 0. The SRIX4K uses dedicated logic that only allows the update of a counter if the new value is lower than the previous one. This feature allows the application to count down by steps of 1 or more. The initial value in Counter 5 is FFFF FFFEh and is FFFF FFFFh in Counter 6. When the value displayed is 0000 0000h, the counter is empty and cannot be reloaded. The counter is updated by issuing the Write_block command to block address 5 or 6, depending on which counter is to be updated. The Write_block command writes the new 32-bit value to the counter block address. *Figure 17* shows examples of how the counters operate.

The counter programming cycles are protected by automated antitearing logic. This function allows the counter value to be protected in case of power down within the programming cycle. In case of power down, the counter value is not updated and the previous value continues to be stored.

Figure 16. Binary counter (addresses 5 to 6)

Block Address	MSb b31 — b24 b23 — 32-bit block b16 b15 — b8 b7 — LSb b0	Description
5	32-bit binary counter	Count down Counter
6	32-bit binary counter	

ai07660b

Figure 17. Count down example (binary format)

	b31														b0
Initial data	1	...	1	1	1	1	1	1	1	1	1	1	1	1	1
1-unit decrement	1	...	1	1	1	1	1	1	1	1	1	1	1	1	**0**
1-unit decrement	1	...	1	1	1	1	1	1	1	1	1	1	1	**0**	**1**
1-unit decrement	1	...	1	1	1	1	1	1	1	1	1	1	1	**0**	**0**
8-unit decrement	1	...	1	1	1	1	1	1	1	1	1	**0**	**1**	**0**	**0**
Increment not allowed	1	...	1	1	1	1	1	1	1	1	1	**1**	**0**	**0**	**0**

ai07661

The counter with block address 6 controls the Reload command used to reset the resettable OTP area (addresses 0 to 4). Bits b_{31} to b_{21} act as an 11-bit Reload counter; whenever one of these 11 bits is updated, the SRIX4K detects the change and adds an Erase cycle to the Write_block command for locations 0 to 4 (see *Section 4.1: Resettable OTP area*). The Erase cycle remains active until a Power-off or a Select command is issued. The SRIX4K's resettable OTP area can be reloaded up to 2,047 times (2^{11}-1).

4.3 EEPROM area

The 121 blocks between addresses 7 and 127 are EEPROM blocks of 32 bits each (484 bytes in total). (See *Figure 18* for a map of the area.) These blocks can be accessed using the Read_block and Write_block commands. The Write_block command for the EEPROM area always includes an auto-erase cycle prior to the write cycle.

Blocks 7 to 15 can be write-protected. Write access is controlled by the 8 bits of the OTP_Lock_Reg located at block address 255 (see *Section 4.4.1: OTP_Lock_Reg* for details). Once protected, these blocks (7 to 15) cannot be unprotected.

Figure 18. EEPROM (addresses 7 to 127)

Block address	MSb b31 b24 b23 32-bit block b16 b15 b8 b7 LSb b0	Description
7	User area	Lockable EEPROM
8	User area	
9	User area	
10	User area	
11	User area	
12	User area	
13	User area	
14	User area	
15	User area	
16	User area	EEPROM
...	User area	
127	User area	

Ai07662c

4.4 System area

This area is used to modify the settings of the SRIX4K. It contains 3 registers: OTP_Lock_Reg, Fixed Chip_ID and ST Reserved. See *Figure 19* for a map of this area.

A Write_block command in this area will not erase the previous contents. Selected bits can thus be set from 1 to 0. All bits previously at 0 remain unchanged. Once all the 32 bits of a block are at 0, the block is empty and cannot be updated any more.

Figure 19. System area

Block address	MSb b31 b24 b23	32-bit block b16 b15 b8 b7	LSb b0	Description
255	OTP_Lock_Reg	ST reserved	Fixed Chip_ID (Option)	OTP

ai07663b

4.4.1 OTP_Lock_Reg

The 8 bits, b_{31} to b_{24}, of the System area (block address 255) are used as OTP_Lock_Reg bits in the SRIX4K. They control the write access to the 9 EEPROM blocks with addresses 7 to 15 as follows:

- When b_{24} is at 0, blocks 7 and 8 are write-protected
- When b_{25} is at 0, block 9 is write-protected
- When b_{26} is at 0, block 10 is write-protected
- When b_{27} is at 0, block 11 is write-protected
- When b_{28} is at 0, block 12 is write-protected
- When b_{29} is at 0, block 13 is write-protected
- When b_{30} is at 0, block 14 is write-protected
- When b_{31} is at 0, block 15 is write-protected.

The OTP_Lock_Reg bits cannot be erased. Once write-protected, EEPROM blocks behave like ROM blocks and cannot be unprotected.

4.4.2 Fixed Chip_ID (Option)

The SRIX4K is provided with an anticollision feature based on a random 8-bit Chip_ID. Prior to selecting an SRIX4K, an anticollision sequence has to be run to search for the Chip_ID of the SRIX4K. This is a very flexible feature, however the searching loop requires time to run.

For some applications, much time could be saved by knowing the value of the SRIX4K Chip_ID beforehand, so that the SRIX4K can be identified and selected directly without having to run an anticollision sequence. This is why the SRIX4K was designed with an optional mask setting used to program a fixed 8-bit Chip_ID to bits b_7 to b_0 of the system area. When the fixed Chip_ID option is used, the random Chip_ID function is disabled.

5 SRIX4K operation

All commands, data and CRC are transmitted to the SRIX4K as 10-bit characters using ASK modulation. The start bit of the 10 bits, b_0, is sent first. The command frame received by the SRIX4K at the antenna is demodulated by the 10% ASK demodulator, and decoded by the internal logic. Prior to any operation, the SRIX4K must have been selected by a Select command. Each frame transmitted to the SRIX4K must start with a start of frame, followed by one or more data characters, two CRC bytes and the final end of frame. When an invalid frame is decoded by the SRIX4K (wrong command or CRC error), the memory does not return any error code.

When a valid frame is received, the SRIX4K may have to return data to the reader. In this case, data is returned using BPSK encoding, in the form of 10-bit characters framed by an SOF and an EOF. The transfer is ended by the SRIX4K sending the 2 CRC bytes and the EOF.

6 SRIX4K states

The SRIX4K can be switched into different states. Depending on the current state of the SRIX4K, its logic will only answer to specific commands. These states are mainly used during the anticollision sequence, to identify and to access the SRIX4K in a very short time. The SRIX4K provides 6 different states, as described in the following paragraphs and in *Figure 20*.

6.1 Power-off state

The SRIX4K is in Power-off state when the electromagnetic field around the tag is not strong enough. In this state, the SRIX4K does not respond to any command.

6.2 Ready state

When the electromagnetic field is strong enough, the SRIX4K enters the Ready state. After power-up, the Chip_ID is initialized with a random value. The whole logic is reset and remains in this state until an Initiate() command is issued. Any other command will be ignored by the SRIX4K.

6.3 Inventory state

The SRIX4K switches from the Ready to the Inventory state after an Initiate() command has been issued. In Inventory state, the SRIX4K will respond to any anticollision commands: Initiate(), Pcall16() and Slot_marker(), and then remain in the Inventory state. It will switch to the Selected state after a Select(Chip_ID) command is issued, if the Chip_ID in the command matches its own. If not, it will remain in Inventory state.

6.4 Selected state

In Selected state, the SRIX4K is active and responds to all Read_block(), Write_block(), Authenticate() and Get_UID() commands. When an SRIX4K has entered the Selected state, it no longer responds to anticollision commands. So that the reader can access another tag, the SRIX4K can be switched to the Deselected state by sending a Select(Chip_ID2) with a Chip_ID that does not match its own, or it can be placed in Deactivated state by issuing a Completion() command. Only one SRIX4K can be in Selected state at a time.

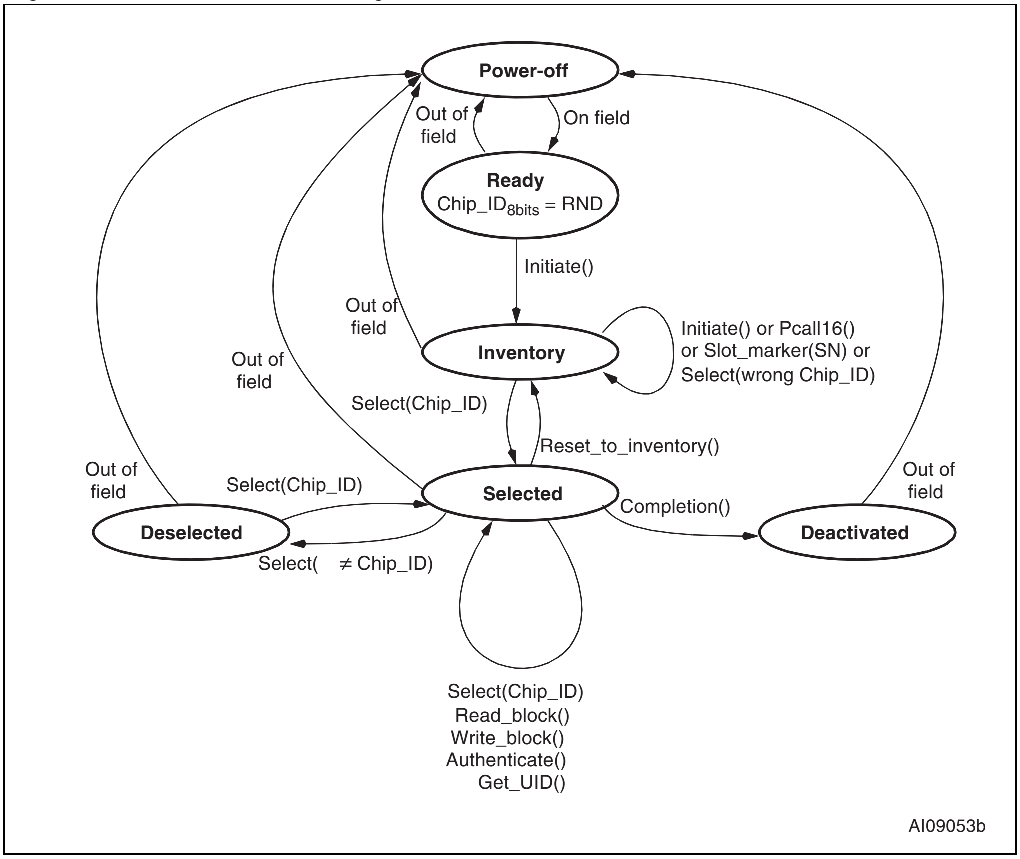
6.5 Deselected state

Once the SRIX4K is in Deselected state, only a Select(Chip_ID) command with a Chip_ID matching its own can switch it back to Selected state. All other commands are ignored.

6.6 Deactivated state

When in this state, the SRIX4K can only be turned off. All commands are ignored.

Figure 20. State transition diagram



7 Anticollision

The SRIX4K provides an anticollision mechanism that searches for the Chip_ID of each device that is present in the reader field range. When known, the Chip_ID is used to select an SRIX4K individually, and access its memory. The anticollision sequence is managed by the reader through a set of commands described in *Section 5: SRIX4K operation*:

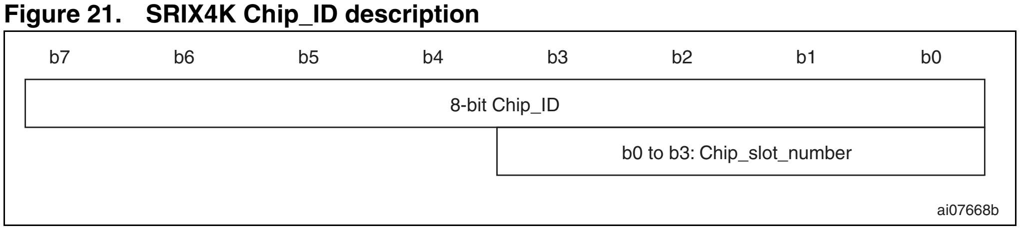
- Initiate()
- Pcall16()
- Slot_marker().

The reader is the master of the communication with one or more SRIX4K device(s). It initiates the tag communication activity by issuing an Initiate(), Pcall16() or Slot_marker() command to prompt the SRIX4K to answer. During the anticollision sequence, it might happen that two or more SRIX4K devices respond simultaneously, so causing a collision. The command set allows the reader to handle the sequence, to separate SRIX4K transmissions into different time slots. Once the anticollision sequence has completed, SRIX4K communication is fully under the control of the reader, allowing only one SRIX4K to transmit at a time.

The Anticollision scheme is based on the definition of time slots during which the SRIX4K devices are invited to answer with minimum identification data: the Chip_ID. The number of slots is fixed at 16 for the Pcall16() command. For the Initiate() command, there is no slot and the SRIX4K answers after the command is issued. SRIX4K devices are allowed to answer only once during the anticollision sequence. Consequently, even if there are several SRIX4K devices present in the reader field, there will probably be a slot in which only one SRIX4K answers, allowing the reader to capture its Chip_ID. Using the Chip_ID, the reader can then establish a communication channel with the identified SRIX4K. The purpose of the anticollision sequence is to allow the reader to select one SRIX4K at a time.

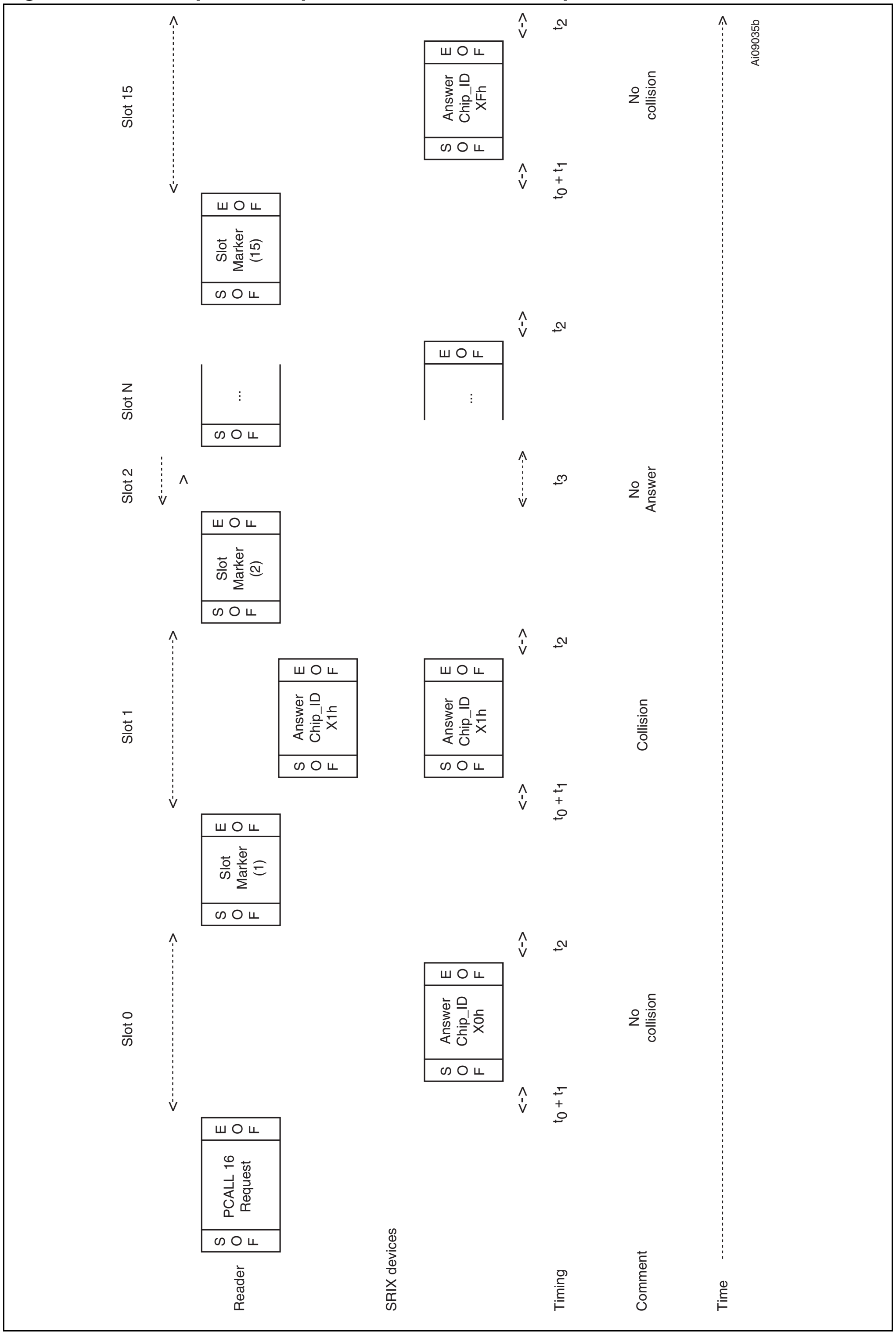
The SRIX4K is given an 8-bit Chip_ID value used by the reader to select only one among up to 256 tags present within its field range. The Chip_ID is initialized with a random value during the Ready state, or after an Initiate() command in the Inventory state.
The four least significant bits (b_0 to b_3) of the Chip_ID are also known as the Chip_slot_number. This 4-bit value is used by the Pcall16() and Slot_marker() commands during the anticollision sequence in the Inventory state.

Figure 21. SRIX4K Chip_ID description



Each time the SRIX4K receives a Pcall16() command, the Chip_slot_number is given a new 4-bit random value. If the new value is 0000_b, the SRIX4K returns its whole 8-bit Chip_ID in its answer to the Pcall16() command. The Pcall16() command is also used to define the slot number 0 of the anticollision sequence. When the SRIX4K receives the Slot_marker(SN) command, it compares its Chip_slot_number with the Slot_number parameter (SN). If they match, the SRIX4K returns its Chip_ID as a response to the command. If they do not, the SRIX4K does not answer. The Slot_marker(SN) command is used to define all the anticollision slot numbers from 1 to 15.

Figure 22. Description of a possible anticollision sequence



1. The value X in the Answer Chip_ID means a random hexadecimal character from 0 to F.

7.1 Description of an anticollision sequence

The anticollision sequence is initiated by the Initiate() command which triggers all the SRIX4K devices that are present in the reader field range, and that are in Inventory state. Only SRIX4K devices in Inventory state will respond to the Pcall16() and Slot_marker(SN) anticollision commands.

A new SRIX4K introduced in the field range during the anticollision sequence will not be taken into account as it will not respond to the Pcall16() or Slot_marker(SN) command (Ready state). To be considered during the anticollision sequence, it must have received the Initiate() command and entered the Inventory state.

Table 3 shows the elements of a standard anticollision sequence. (See *Figure 23* for an example.)

Table 3. Standard anticollision sequence

Step 1	Init:	Send Initiate(). – If no answer is detected, go to step1. – If only 1 answer is detected, select and access the SRIX4K. After accessing the SRIX4K, deselect the tag and go to step1. – If a collision (many answers) is detected, go to step2.
Step 2	Slot 0	Send Pcall16(). – If no answer or collision is detected, go to step3. – If 1 answer is detected, store the Chip_ID, Send Select() and go to step3.
Step 3	Slot 1	Send Slot_marker(1). – If no answer or collision is detected, go to step4. – If 1 answer is detected, store the Chip_ID, Send Select() and go to step4.
Step 4	Slot 2	Send Slot_marker(2). – If no answer or collision is detected, go to step5. – If 1 answer is detected, store the Chip_ID, Send Select() and go to step5.
Step N	Slop N	Send Slot_marker(3 up to 14) ... – If no answer or collision is detected, go to stepN+1. – If 1 answer is detected, store the Chip_ID, Send Select() and go to stepN+1.
Step 17	Slot 15	Send Slot_marker(15). – If no answer or collision is detected, go to step18. – If 1 answer is detected, store the Chip_ID, Send Select() and go to step18.
Step 18		All the slots have been generated and the Chip_ID values should be stored into the reader memory. Issue the Select(Chip_ID) command and access each identified SRIX4K one by one. After accessing each SRIX4K, switch them into Deselected or Deactivated state, depending on the application needs. – If collisions were detected between Step2 and Step17, go to Step2. – If no collision was detected between Step2 and Step17, go to Step1.

After each Slot_marker() command, there may be several, one or no answers from the SRIX4K devices. The reader must handle all the cases and store all the Chip_IDs, correctly decoded. At the end of the anticollision sequence, after Slot_marker(15), the reader can start working with one SRIX4K by issuing a Select() command containing the desired Chip_ID. If a collision is detected during the anticollision sequence, the reader has to generate a new sequence in order to identify all unidentified SRIX4K devices in the field. The anticollision sequence can stop when all SRIX4K devices have been identified.

Figure 23. Example of an anticollision sequence

Command	Tag 1 Chip_ID	Tag 2 Chip_ID	Tag 3 Chip_ID	Tag 4 Chip_ID	Tag 5 Chip_ID	Tag 6 Chip_ID	Tag 7 Chip_ID	Tag 8 Chip_ID	Comments
READY State	28h	75h	40h	01h	02h	FEh	A9h	7Ch	Each tag gets a random Chip_ID
INITIATE ()	40h	13h	3Fh	4Ah	50h	48h	52h	7Ch	Each tag get a new random Chip_ID. All tags answer: collisions
PCALL16()	45h	12h	30h	43h	55h	43h	53h	73h	All CHIP_SLOT_NUMBERs get a new random value
			30h						Slot0: only one answer
SELECT(30h)			30h						Tag3 is identified
SLOT_MARKER(1)									Slot1: no answer
SLOT_MARKER(2)		12h							Slot2: only one answer
SELECT(12h)		12h							Tag2 is identified
SLOT_MARKER(3)				43h		43h	53h	73h	Slot3: collisions
SLOT_MARKER(4)									Slot4: no answer
SLOT_MARKER(5)	45h				55h				Slot5: collisions
SLOT_MARKER(6)									Slot6: no answer
SLOT_MARKER(N)									SlotN: no answer
SLOT_MARKER(F)									SlotF: no answer
PCALL16()	40h			41h	53h	42h	50h	74h	All CHIP_SLOT_NUMBERs get a new random value
	40h						50h		Slot0: collisions
SLOT_MARKER(1)				41h					Slot1: only one answer
SELECT(41h)				41h					Tag4 is identified
SLOT_MARKER(2)						42h			Slot2: only one answer
SELECT(42h)						42h			Tag6 is identified
SLOT_MARKER(3)					53h				Slot3: only one answer
SELECT(53h)					53h				Tag5 is identified
SLOT_MARKER(4)								74h	Slot4: only one answer
SELECT(74h)								74h	Tag8 is identified
SLOT_MARKER(N)									SlotN: no answer
PCALL16()	41h						50h		All CHIP_SLOT_NUMBERs get a new random value
							50h		Slot0: only one answer
SELECT(50h)							50h		Tag7 is identified
SLOT_MARKER(1)	41h								Slot1: only one answer but already found for tag4
SLOT_MARKER(N)									SlotN: no answer
PCALL16()	43h								All CHIP_SLOT_NUMBERs get a new random value
									Slot0: only one answer
SLOT_MARKER(3)	43h								Slot3: only one answer
SELECT(43h)	43h								Tag1 is identified
									All tags are identified

ai07669

8 Anti-clone function

The SRIX4K provides an anti-clone function that allows the application to authentication the device. This function uses reserved data that is stored in the SRIX4K memory at its time of manufacture.

The Authentication system is based on a proprietary challenge/response mechanism which allows the application software to authenticate any member of the secure memory tag SRXxxx family from STMicroelectronics (of which the SRIX4K is the prime example). A reader system, based on the ST CRX14 chip coupler, can check each SRIX4K tag for authenticity, and protect the application system against silicon copies or emulators.

A complete description of the Authentication system is available under non disclosure agreement (NDA) with STMicroelectronics. For more details about this SRIX4K function, please contact your nearest STMicroelectronics sales office.

9 SRIX4K commands

See the paragraphs below for a detailed description of the commands available on the SRIX4K. The commands and their hexadecimal codes are summarized in *Table 4*. A brief is given in *Appendix B*.

Table 4. Command code

Hexadecimal Code	Command
06h-00h	Initiate()
06h-04h	Pcall16()
x6h	Slot_marker (SN)
08h	Read_block(Addr)
09h	Write_block(Addr, Data)
0Ah	Authenticate(RND)
0Bh	Get_UID()
0Ch	Reset_to_inventory
0Eh	Select(Chip_ID)
0Fh	Completion()

9.1 Initiate() command

Command code = 06h - 00h

Initiate() is used to initiate the anticollision sequence of the SRIX4K. On receiving the Initiate() command, all SRIX4K devices in Ready state switch to Inventory state, set a new 8-bit Chip_ID random value, and return their Chip_ID value. This command is useful when only one SRIX4K in Ready state is present in the reader field range. It speeds up the Chip_ID search process. The Chip_slot_number is not used during Initiate() command access.

Figure 24. Initiate request format

SOF	Initiate		CRC_L	CRC_H	EOF
	06h	00h	8 bits	8 bits	

AI07670b

Request parameter:

- No parameter

Figure 25. Initiate response format

SOF	Chip_ID	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	

AI07671

Response parameter:

- Chip_ID of the SRIX4K

Figure 26. Initiate frame exchange between reader and SRIX4K

Reader	SOF	06h	00h	CRC_L	CRC_H	EOF						
SRIX4K							<-t_0-><-t_1->	SOF	Chip_ID	CRC_L	CRC_H	EOF

AI07672b

9.2 Pcall16() command

Command code = 06h - 04h

The SRIX4K must be in Inventory state to interpret the Pcall16() command.

On receiving the Pcall16() command, the SRIX4K first generates a new random Chip_slot_number value (in the 4 least significant bits of the Chip_ID). Chip_slot_number can take on a value between 0 an 15 (1111_b). The value is retained until a new Pcall16() or Initiate() command is issued, or until the SRIX4K is powered off. The new Chip_slot_number value is then compared with the value 0000_b. If they match, the SRIX4K returns its Chip_ID value. If not, the SRIX4K does not send any response.

The Pcall16() command, used together with the Slot_marker() command, allows the reader to search for all the Chip_IDs when there are more than one SRIX4K device in Inventory state present in the reader field range.

Figure 27. Pcall16 request format

SOF	Pcall16		CRC_L	CRC_H	EOF
	06h	04h	8 bits	8 bits	

AI07673b

Request parameter:

- No parameter

Figure 28. Pcall16 response format

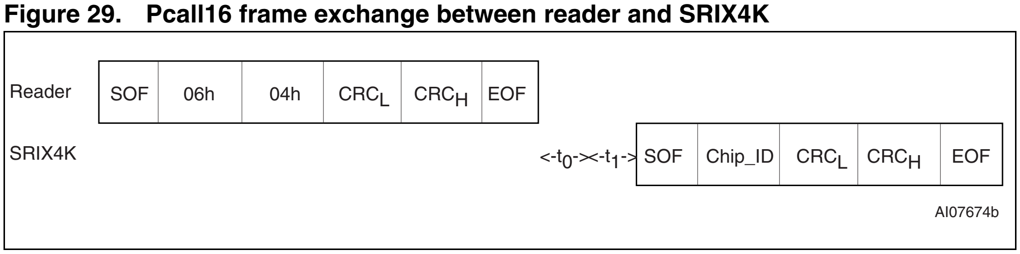
SOF	Chip_ID	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	

AI07671

Response parameter:

- Chip_ID of the SRIX4K

Figure 29. Pcall16 frame exchange between reader and SRIX4K



9.3 Slot_marker(SN) command

Command code = x6h

The SRIX4K must be in Inventory state to interpret the Slot_marker(SN) command.

The Slot_marker byte code is divided into two parts:

- b_3 to b_0: 4-bit command code
  with fixed value 6.
- b_7 to b_4: 4 bits known as the Slot_number (SN). They assume a value between 1 and 15. The value 0 is reserved by the Pcall16() command.

On receiving the Slot_marker() command, the SRIX4K compares its Chip_slot_number value with the Slot_number value given in the command code. If they match, the SRIX4K returns its Chip_ID value. If not, the SRIX4K does not send any response.

The Slot_marker() command, used together with the Pcall16() command, allows the reader to search for all the Chip_IDs when there are more than one SRIX4K device in Inventory state present in the reader field range.

Figure 30. Slot_marker request format

SOF	SLOT_MARKER	CRC_L	CRC_H	EOF
	X6h	8 bits	8 bits	

AI07675

Request parameter:

- x: Slot number

Figure 31. Slot_marker response format

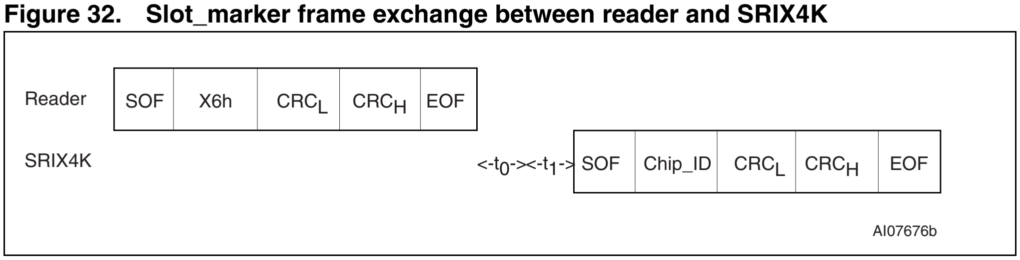
SOF	Chip_ID	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	

AI07671

Response parameters:

- Chip_ID of the SRIX4K

Figure 32. Slot_marker frame exchange between reader and SRIX4K



9.4 Select(Chip_ID) command

Command code = 0Eh

The Select() command allows the SRIX4K to enter the Selected state. Until this command is issued, the SRIX4K will not accept any other command, except for Initiate(), Pcall16() and Slot_marker(). The Select() command returns the 8 bits of the Chip_ID value. An SRIX4K in Selected state, that receives a Select() command with a Chip_ID that does not match its own is automatically switched to Deselected state.

Figure 33. Select request format

SOF	Select	Chip_ID	CRC_L	CRC_H	EOF
	0Eh	8 bits	8 bits	8 bits	

AI07677b

Request parameter:

- 8-bit Chip_ID stored during the anticollision sequence

Figure 34. Select response format

SOF	Chip_ID	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	

AI07671

Response parameters:

- Chip_ID of the selected tag. Must be equal to the transmitted Chip_ID

Figure 35. Select frame exchange between reader and SRIX4K

Reader	SOF	0Eh	Chip_ID	CRC_L	CRC_H	EOF						
SRIX4K							<-t_0-><-t_1->	SOF	Chip_ID	CRC_L	CRC_H	EOF

AI07678b

9.5 Completion() command

Command code = 0Fh

On receiving the Completion() command, an SRIX4K in Selected state switches to Deactivated state and stops decoding any new commands. The SRIX4K is then locked in this state until a complete reset (tag out of the field range). A new SRIX4K can thus be accessed through a Select() command without having to remove the previous one from the field. The Completion() command does not generate a response.

All SRIX4K devices not in Selected state ignore the Completion() command.

Figure 36. Completion request format

SOF	Completion	CRC_L	CRC_H	EOF
	0Fh	8 bits	8 bits	

AI07679b

Request parameters:

- No parameter

Figure 37. Completion response format

No Response

AI07680

Figure 38. Completion frame exchange between reader and SRIX4K

Reader	SOF	0Fh	CRC_L	CRC_H	EOF	
SRIX4K						No Response

AI07681

9.6 Reset_to_inventory() command

Command code = 0Ch

On receiving the Reset_to_inventory() command, all SRIX4K devices in Selected state revert to Inventory state. The concerned SRIX4K devices are thus resubmitted to the anticollision sequence. This command is useful when two SRIX4K devices with the same 8-bit Chip_ID happen to be in Selected state at the same time. Forcing them to go through the anticollision sequence again allows the reader to generates new Pcall16() commands and so, to set new random Chip_IDs.

The Reset_to_inventory() command does not generate a response.

All SRIX4K devices that are not in Selected state ignore the Reset_to_inventory() command.

Figure 39. Reset_to_inventory request format

SOF	Reset_to_inventory	CRC_L	CRC_H	EOF
	0Ch	8 bits	8 bits	

AI07682b

Request parameter:

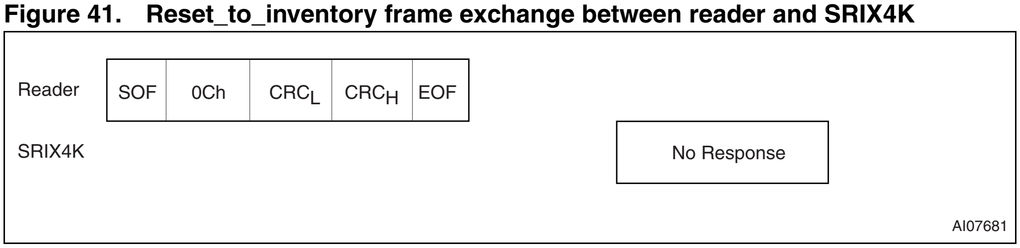
- No parameter

Figure 40. Reset_to_inventory response format

No Response

AI07680

Figure 41. Reset_to_inventory frame exchange between reader and SRIX4K



9.7 Read_block(Addr) command

Command code = 08h

On receiving the Read_block command, the SRIX4K reads the desired block and returns the 4 data bytes contained in the block. Data bytes are transmitted with the Least Significant byte first and each byte is transmitted with the least significant bit first.

The address byte gives access to the 128 blocks of the SRIX4K (addresses 0 to 127). Read_block commands issued with a block address above 127 will not be interpreted and the SRIX4K will not return any response, except for the System area located at address 255.

The SRIX4K must have received a Select() command and be switched to Selected state before any Read_block() command can be accepted. All Read_block() commands sent to the SRIX4K before a Select() command is issued are ignored.

Figure 42. Read_block request format

SOF	Read_block	Address	CRC_L	CRC_H	EOF
	08h	8 bits	8 bits	8 bits	

AI07684b

Request parameter:

- Address: block addresses from 0 to 127, or 255

Figure 43. Read_block response format

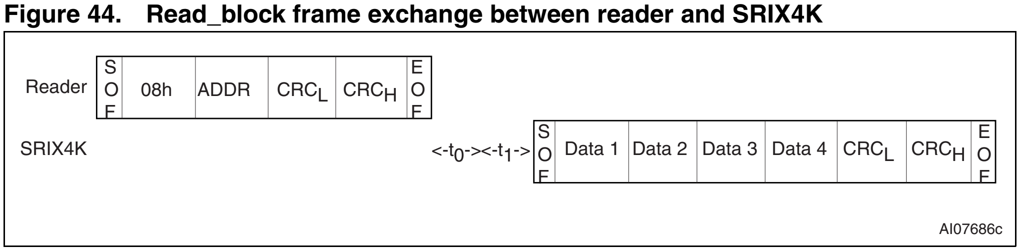
SOF	Data 1	Data 2	Data 3	Data 4	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	

AI07685b

Response parameters:

- Data 1: Less significant data byte
- Data 2: Data byte
- Data 3: Data byte
- Data 4: Most significant data byte

Figure 44. Read_block frame exchange between reader and SRIX4K



9.8 Write_block (Addr, Data) command

Command code = 09h

On receiving the Write_block command, the SRIX4K writes the 4 bytes contained in the command to the addressed block, provided that the block is available and not write-protected. Data bytes are transmitted with the least significant byte first, and each byte is transmitted with the least significant bit first.

The address byte gives access to the 128 blocks of the SRIX4K (addresses 0 to 127). Write_block commands issued with a block address above 127 will not be interpreted and the SRIX4K will not return any response, except for the System area located at address 255.

The result of the Write_block command is submitted to the addressed block. See the following Figures for a complete description of the Write_block command:

- *Figure 13: Resettable OTP area (addresses 0 to 4)*.
- *Figure 16: Binary counter (addresses 5 to 6)*.
- *Figure 18: EEPROM (addresses 7 to 127)*.

The Write_block command does not give rise to a response from the SRIX4K. The reader must check after the programming time, t_W, that the data was correctly programmed. The SRIX4K must have received a Select() command and be switched to Selected state before any Write_block command can be accepted. All Write_block commands sent to the SRIX4K before a Select() command is issued, are ignored.

Figure 45. Write_block request format

SOF	Write_block	Address	Data 1	Data 2	Data 3	Data 4	CRC_L	CRC_H	EOF
	09h	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	

AI07687b

Request parameters:

- Address: block addresses from 0 to 127, or 255
- Data 1: Less significant data byte
- Data 2: Data byte
- Data 3: Data byte
- Data 4: Most significant data byte.

Figure 46. Write_block response format

No Response

AI07680

Figure 47. Write_block frame exchange between reader and SRIX4K

Reader	SOF	09h	Address	Data 1	Data 2	Data 3	Data 4	CRC_L	CRC_H	EOF
SRIX4K										No response

AI0768b

9.9 Get_UID() command

Command code = 0Bh

On receiving the Get_UID command, the SRIX4K returns its 8 UID bytes. UID bytes are transmitted with the least significant byte first, and each byte is transmitted with the least significant bit first.

The SRIX4K must have received a Select() command and be switched to Selected state before any Get_UID() command can be accepted. All Get_UID() commands sent to the SRIX4K before a Select() command is issued, are ignored.

Figure 48. Get_UID request format

SOF	Get_UID	CRC_L	CRC_H	EOF
	0Bh	8 bits	8 bits	

AI07693b

Request parameter:

- No parameter

Figure 49. Get_UID response format

SOF	UID 0	UID 1	UID 2	UID 3	UID 4	UID 5	UID 6	UID 7	CRC_L	CRC_H	EOF
	8 bits	8 bIts	8 bIts	8 bIts	8 bIts	8 bIts	8 bIts	8 bIts	8 bits	8 bIts	

AI07694

Response parameters:

- UID 0: Less significant UID byte
- UID 1 to UID 6: UID bytes
- UID 7: Most significant UID byte.

Unique Identifier (UID)

Members of the SRIX4K family are uniquely identified by a 64-bit Unique Identifier (UID). This is used for addressing each SRIX4K device uniquely after the anticollision loop. The UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. It is a read-only code, and comprises (as summarized in *Figure 50*):

- an 8-bit prefix, with the most significant bits set to D0h
- an 8-bit IC manufacturer code (ISO/IEC 7816-6/AM1) set to 02h (for STMicroelectronics)
- a 6-bit IC code set to 00 0011b = 3d for SRIX4K
- a 42-bit unique serial number

Figure 50. 64-bit unique identifier of the SRIX4K

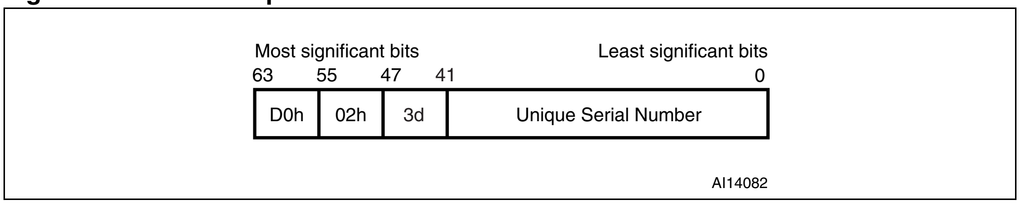
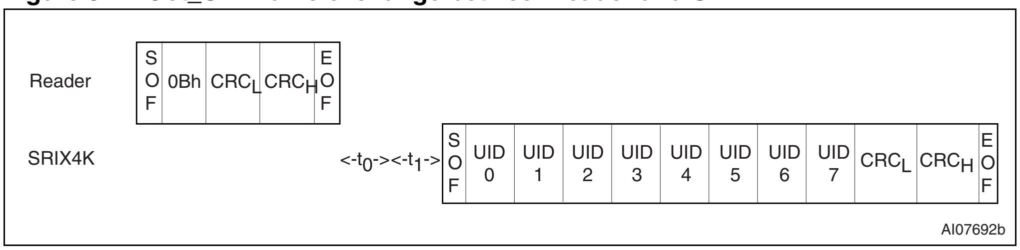


Figure 51. Get_UID frame exchange between reader and SRIX4K



9.10 Power-on state

After power-on, the SRIX4K is in the following state:

- It is in the low-power state.
- It is in Ready state.
- It shows highest impedance with respect to the reader antenna field.
- It will not respond to any command except Initiate().

10 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage conditions	Wafer (kept in its antistatic bag)	15	25	°C
t_{STG}				23	months
I_{CC}	Supply current on AC0 / AC1		–20	20	mA
V_{MAX}	Input voltage on AC0 / AC1		–7	7	V
V_{ESD}	Electrostatic discharge voltage(1)	Machine model	–100	100	V
		Human body model	–1000	1000	V

1. Mil. Std. 883 - Method 3015

11 DC and ac parameters

Table 6. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–20	85	°C

Table 7. DC characteristics

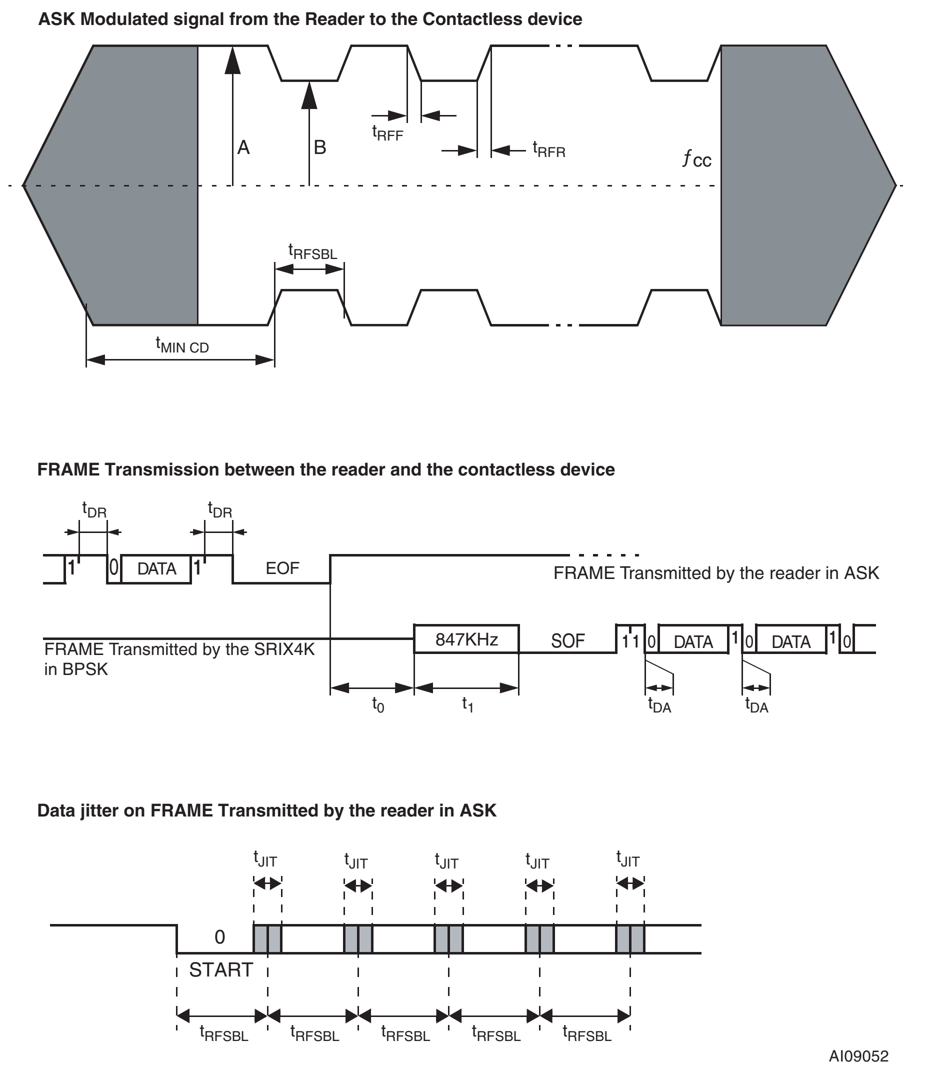
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Regulated voltage		2.5		3.5	V
I_{CC}	Supply current (active in read)	V_{CC} = 3.0 V			100	µA
I_{CC}	Supply current (active in write)	V_{CC} = 3.0 V			250	µA
V_{RET}	Retromodulation induced voltage	ISO 10373-6	20			mV
C_{TUN}	Internal tuning capacitor	13.56 MHz		64		pF

Table 8. AC characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{CC}	External RF signal frequency		13.553	13.567	MHz
$MI_{CARRIER}$	Carrier modulation index	MI=(A-B)/(A+B)	8	14	%
t_{RFR}, t_{RFF}	10% rise and fall times		0.8	2.5	µs
t_{RFSBL}	Minimum pulse width for start bit	ETU = 128/f_{CC}	9.44		µs
t_{JIT}	ASK modulation data jitter	Coupler to SRIX4K	–2	+2	µs
$t_{MIN\ CD}$	Minimum time from carrier generation to first data		5		ms
f_S	Subcarrier frequency	f_{CC}/16	847.5		kHz
t_0	Antenna reversal delay	128/f_S	151		µs
t_1	Synchronization delay	128/f_S	151		µs
t_2	Answer to new request delay	14 ETU	132		µs
t_{DR}	Time between request characters	Coupler to SRIX4K	0	57	µs
t_{DA}	Time between answer characters	SRIX4K to coupler	0		µs
t_W	Programming time for write	With no auto-erase cycle (OTP)		3	ms
		With auto-erase cycle (EEPROM)		5	ms
		Binary counter decrement		7	ms

1. All timing measurements were performed on a reference antenna with the following characteristics:
External size: 75 mm x 48 mm
Number of turns: 3
Width of conductor: 1 mm
Space between 2 conductors: 0.4 mm
Value of the coil: 1.4 µH
Tuning Frequency: 14.4 MHz.

Figure 52. SRIX4K synchronous timing, transmit and receive



12 Part numbering

Table 9. Ordering information scheme

Example: SRIX4K – W4 /1GE

Device type

SRIX4K

Package

W4 = 180 µm ± 15 µm unsawn wafer

SBN18 = 180 µm ± 15 µm bumped and sawn wafer on 8-inch frame

Customer code

1GE = generic product

xxx = customer code after personalization

Note: Devices are shipped from the factory with the memory content bits erased to 1.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A ISO 14443 Type B CRC calculation

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTE unsigned char
#define USHORT unsigned short

unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
   ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
   ch = (ch^(ch<<4));
   *lpwCrc = (*lpwCrc >> 8)^((USHORT)ch <<
8)^((USHORT)ch<<3)^((USHORT)ch>>4);
   return(*lpwCrc);
}

void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE
*TransmitSecond)
{
BYTE chBlock; USHORTt wCrc;
   wCrc = 0xFFFF; // ISO 3309
   do
      {
      chBlock = *Data++;
      UpdateCrc(chBlock, &wCrc);
      } while (--Length);
   wCrc = ~wCrc; // ISO 3309
   *TransmitFirst = (BYTE) (wCrc & 0xFF);
   *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
   return;
}

int main(void)
{
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
   printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1”);
   printf("CRC_B of [ ");
   for(i=0; i<4; i++)
      printf("%02X ",BuffCRC_B[i]);
   ComputeCrc(BuffCRC_B, 4, &First, &Second);
   printf("] Transmitted: %02X then %02X.”, First, Second);
   return(0);
```

Appendix B SRIX4K command summary

Figure 53. Initiate frame exchange between reader and SRIX4K

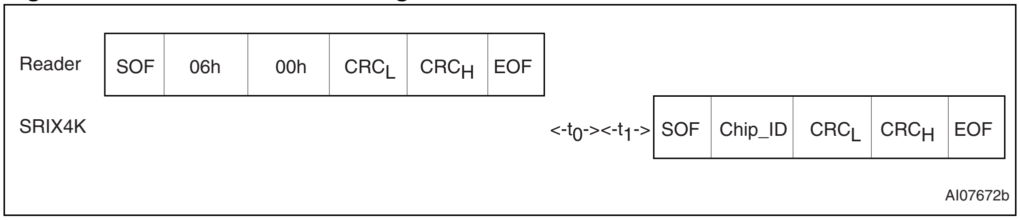


Figure 54. Pcall16 frame exchange between reader and SRIX4K

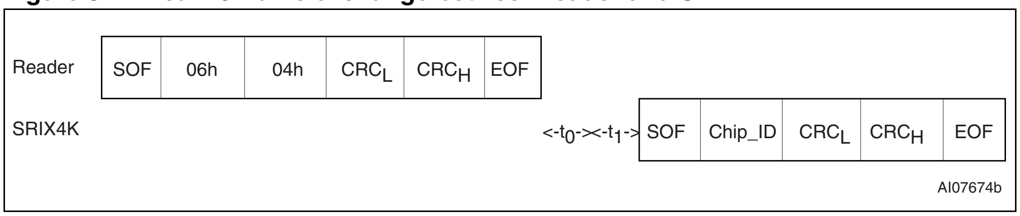


Figure 55. Slot_marker frame exchange between reader and SRIX4K

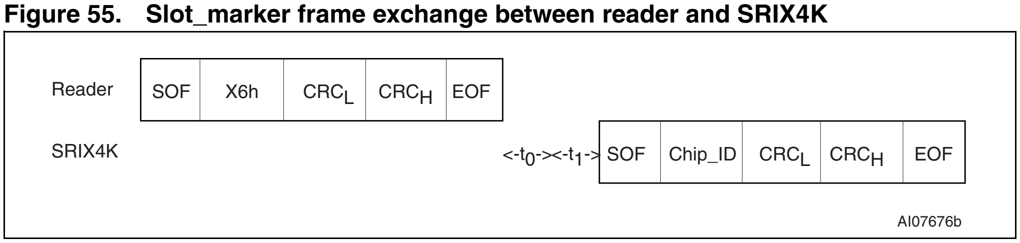


Figure 56. Select frame exchange between reader and SRIX4K

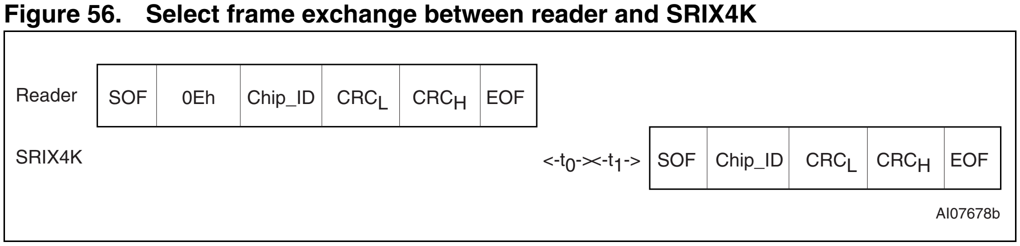


Figure 57. Completion frame exchange between reader and SRIX4K

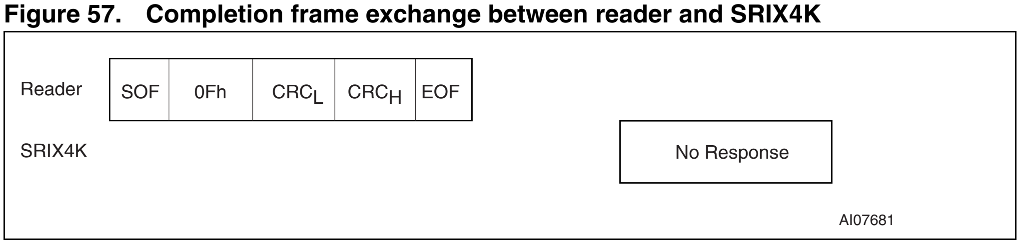


Figure 58. Reset_to_inventory frame exchange between reader and SRIX4K

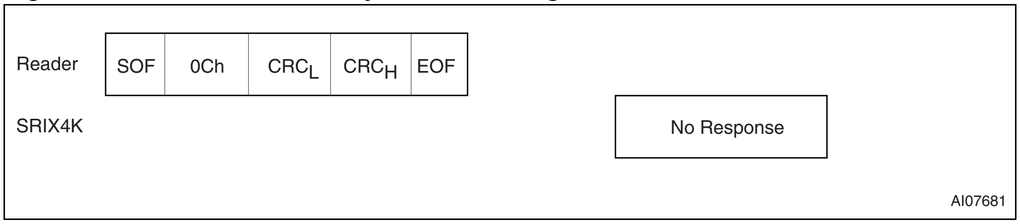


Figure 59. Read_block frame exchange between reader and SRIX4K

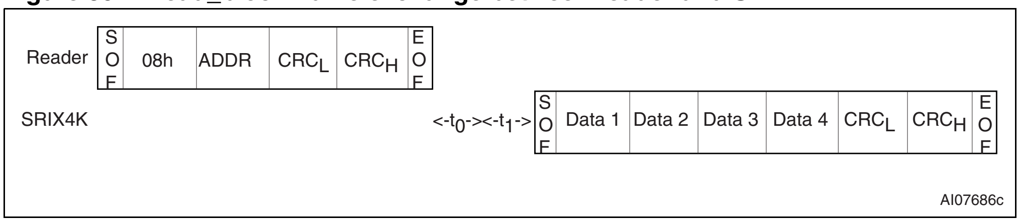


Figure 60. Write_block frame exchange between reader and SRIX4K

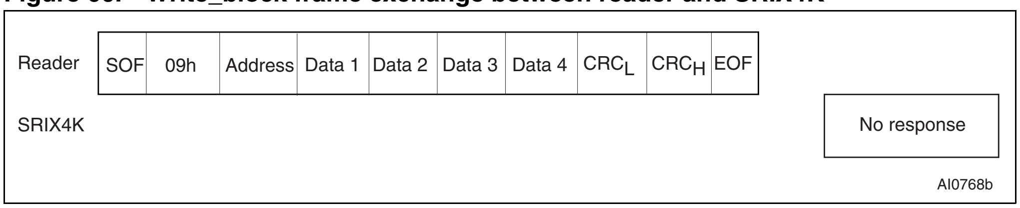
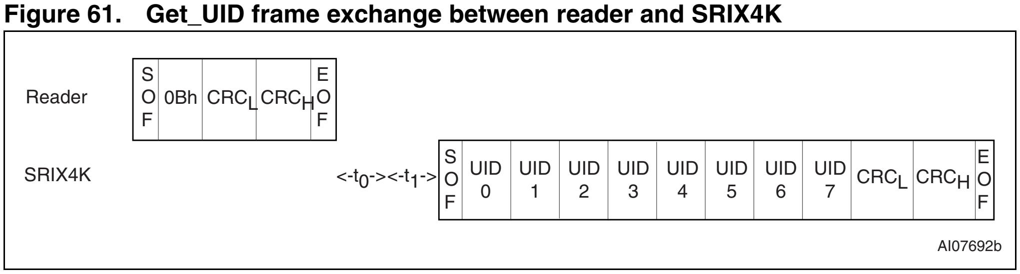


Figure 61. Get_UID frame exchange between reader and SRIX4K



Revision history

Table 10. Document revision history

Date	Version	Changes
28-Nov-2002	1.0	Document written
17-Jul-2003	1.1	Data briefing extracted
12-Mar-2004	2.0	First public release of full datasheet
26-Apr-2004	3.0	Correction to memory map
29-Nov-2004	4.0	*Package mechanical* section revised.
13-Dec-2004	5.0	V_{RET} and C_{TUN} parameters added to *Table 7: DC characteristics*.
17-Aug-2005	6.0	Updated initial counter values in *Section 4.2: 32-bit binary counters on page 16*.
10-Apr-2007	7	Document reformatted. Small text changes. All antennas are ECOPACK® compliant. *Unique Identifier (UID) on page 38* added. C_{TUN} min and max values removed, typical value added in *Table 7: DC characteristics*. Space removed between t0 and t1 in “frame exchange between reader and SRIX4K” Figures (see *Appendix B: SRIX4K command summary on page 44*).
28-Aug-2008	8	SRIX4K products no longer delivered in A3, A4 and A5 antennas. *Table 5: Absolute maximum ratings* and *Table 9: Ordering information scheme* clarified. Small text changes.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com