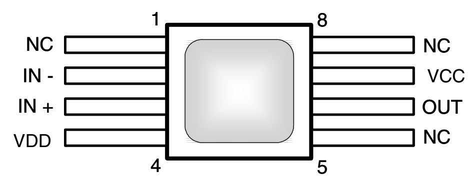
RHF43B

Rad-hard precision bipolar single operational amplifier

Features

- High radiation immunity: 300 kRad TID at high/low dose rate (ELDRS-free), tested immunity of SEL /SEU at 125° C under 120 MeV/mg/cm² LET ions, 14 V supply
- Rail-to-rail output
- 8 MHz gain bandwidth at 16 V
- Low input offset voltage: 100 µV typ
- Supply current: 2.2 mA typ
- Operating from 3 to 16 V
- Input bias current: 30 nA typ
- ESD internal protection ≥ 2 kV
- Latch-up immunity: 200 mA
- QML-V RHA, ELDRS-free qualified under smd 5962-06237

Ceramic Flat-8



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package.

Applications

- Space probes and satellites
- Defense systems
- Scientific instrumentation
- Nuclear systems

Description

The RHF43B is a precision bipolar operational amplifier available in a ceramic 8-pin flat package and in die form. In addition to its low offset voltage, rail-to-rail feature and wide supply voltage, the RHF43B is designed for increased tolerance to radiation. Its intrinsic ELDRS-free rad-hard design allows this product to be used in space applications and in applications operating in harsh environments.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	18 ±9	V
V_{id}	Differential input voltage (2)	±1.2	V
V_{in}	Input voltage range(3)	V_{DD}-0.3 to 16	V
I_{IN}	Input current	45	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4)(5)	125	°C/W
R_{thjc}	Thermal resistance junction to case(4)(5)	40	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	2	kV
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 sec)	260	°C
Radiation related parameters			
Dose	Low dose rate of 0.01 $rad.sec^{-1}$ (up to Vcc = 16 V)	300	kRad
	High dose rate of 50-300 $rad.sec^{-1}$ (up to Vcc = 16 V)	300	kRad
HI	Heavy ion latch-up (SEL) immune with heavy ions (up to Vcc = 14 V)	120	$MeV.cm^2/mg$

1. All values, except differential voltage are with respect to network terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output terminal must never exceed V_{CC} + 0.3 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	V_{DD} to V_{CC}	V
T_{oper}	Operating free air temperature range	-55 to +125	°C

2 Electrical characteristics

Table 3. 16 V supply: V_{CC} = +16 V, V_{DD} = 0 V, load to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Ambient temp.	Min.	Typ.	Max.	Unit
DC performance							
I_{CC}	Supply current	No load	+125°C			2.9	mA
			+25°C		2.5	2.9	
			-55°C			2.9	
V_{io}	Offset voltage	$V_{icm} = V_{CC}/2$	+125°C	-500		500	µV
			+25°C	-300	100	300	
			-55°C	-500		500	
DV_{io}	Input offset voltage drift		-		1		µV/°C
I_{ib}	Input bias current	$V_{icm} = V_{CC}/2$	+125°C	-100		100	nA
			+25°C	-60	30	60	
			-55°C	-100		100	
DI_{ib}	Input offset current temperature drift	$V_{icm} = V_{CC}/2$	-		100		pA/°C
I_{io}	Input offset current	$V_{icm} = V_{CC}/2$	+125°C	-35		35	nA
			+25°C	-15	1	15	
			-55°C	-35		35	
R_{in}	Differential input resistance between in+ and in-		+25°C		0.16		MΩ
	Input resistance between in+ (or in-) and GND		+25°C		2000		
C_{in}	Differential input capacitance between in+ and in-		+25°C		8		pF
	Input capacitance between in+ (or in-) and GND		+25°C		2		
CMR	Common mode rejection ratio	$0 < V_{icm} < 16$ V	+125°C	72			dB
			+25°C	72	110		
			-55°C	72			
SVR	Supply rejection ratio	$3 V < V_{CC} < 16$ V $V_{icm} = V_{CC}/2$	+125°C	80			dB
			+25°C	90	120		
			-55°C	80			
A_{VD}	Large signal voltage gain	V_{out}= 0.5 V to 15.5 V R_L = 1 kΩ $0 < V_{icm} < 16$ V	+125°C	60			dB
			+25°C	74	85		
			-55°C	60			

Table 3. 16 V supply: V_{CC} = +16 V, V_{DD} = 0 V, load to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Ambient temp.	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	R_L = 1 kΩ	+125°C	15.6			V
			+25°C	15.7	15.8		
			-55°C	15.6			
		R_L = 10 kΩ	+125°C	15.8			
			+25°C	15.9	15.96		
			-55°C	15.8			
V_{OL}	Low level output voltage	R_L = 1 kΩ	+125°C			0.3	V
			+25°C		0.1	0.2	
			-55°C			0.3	
		R_L = 10 kΩ	+125°C			0.1	
			+25°C		0.04	0.06	
			-55°C			0.1	
I_{out}	Output sink current	$V_{out} = V_{CC}$	+125°C	15			mA
			+25°C	20	30		
			-55°C	15			
	Output source current	$V_{out} = V_{CC}$	+125°C	10			
			+25°C	15	25		
			-55°C	10			
AC performance							
GBP	Gain bandwidth product	F = 100 kHz R_L= 1 kΩ, C_L= 100 pF	+125°C	3.5			MHz
			+25°C	6	8		
			-55°C	3.5			
F_u	Unity gain frequency	R_L= 1 kΩ, C_L= 100 pF	+25°C		5		MHz
ϕm	Phase margin	Gain = +5 R_L= 1 kΩ, C_L= 100 pF	+25°C		50		Degrees
SR	Slew rate	R_L= 1 kΩ, C_L= 100 pF	+125°C	1.7			V/μs
			+25°C	2	3		
			-55°C	1.7			
e_n	Equivalent input noise voltage	F = 1 kHz	+25°C		7.5		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent input noise current	F = 1 kHz	+25°C		1		$\frac{pA}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	$V_{out} = (V_{CC}-1\ V)/5$ Gain = -5.1 $V_{icm} = V_{CC}/2$	+25°C		0.01		%

Table 4. 3 V supply: V_{CC} = + 3 V, V_{DD} = 0, load to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Ambient temp.	Min.	Typ.	Max.	Unit
DC performance							
I_{CC}	Supply current	No load	+125°C			2.6	mA
			+25°C		2.2	2.6	
			-55°C			2.6	
V_{io}	Offset voltage		+125°C	-500		500	µV
			+25°C	-300	100	300	
			-55°C	-500		500	
DV_{io}	Input offset voltage drift		-		1		µV/°C
I_{ib}	Input bias current	V_{CC} = +4 V $V_{icm} = V_{CC}/2$	+125°C	-100		100	nA
			+25°C	-60	30	60	
			-55°C	-100		100	
DI_{ib}	Input offset current temperature drift	V_{CC} = +4 V $V_{icm} = V_{CC}/2$	-		100		pA/°C
I_{io}	Input offset current	V_{CC} = +4 V $V_{icm} = V_{CC}/2$	+125°C	-35		35	nA
			+25°C	-15	1	15	
			-55°C	-35		35	
R_{in}	Differential input resistance between in+ and in-		+25°C		0.16		MΩ
	Input resistance between in+ (or in-) and GND		+25°C		2000		
C_{in}	Differential input capacitance between in+ and in-		+25°C		8		pF
	Input capacitance between in+ (or in-) and GND		+25°C		2		
CMR	Common mode rejection ratio	$0 < V_{icm} < 3$ V	+125°C	72			dB
			+25°C	72	90		
			-55°C	72			
A_{VD}	Large signal voltage gain	V_{out}= 0.5 V to 2.5 V R_L = 1 kΩ $0 < V_{icm} < 3$ V	+125°C	60			dB
			+25°C	74	85		
			-55°C	60			

Table 4. 3 V supply: V_{CC} = + 3 V, V_{DD} = 0, load to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Ambient temp.	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	R_L = 1 kΩ	+125°C	2.8			V
			+25°C	2.9	2.95		
			-55°C	2.8			
		R_L = 10 kΩ	+125°C	2.9			
			+25°C	2.94	2.98		
			-55°C	2.9			
V_{OL}	Low level output voltage	R_L = 1 kΩ	+125°C			0.2	V
			+25°C		0.05	0.1	
			-55°C			0.2	
		R_L = 10 kΩ	+125°C			0.1	
			+25°C		0.02	0.06	
			-55°C			0.1	
I_{out}	Output sink current	$V_{out} = V_{CC}$	+125°C	15			mA
			+25°C	20	30		
			-55°C	15			
	Output source current	$V_{out} = V_{CC}$	+125°C	10			
			+25°C	15	25		
			-55°C	10			
AC performance							
GBP	Gain bandwidth product	F = 100 kHz R_L= 1 kΩ, C_L= 100 pF	+125°C	3.5			MHz
			+25°C	6	7.5		
			-55°C	3.5			
F_u	Unity gain frequency	R_L= 1 kΩ, C_L= 100 pF	+25°C		5		MHz
ϕm	Phase margin	Gain = +5 R_L= 1 kΩ, C_L= 100 pF	+25°C		50		Degrees
SR	Slew rate	R_L= 1 kΩ, C_L= 100 pF	+125°C	1.7			V/µs
			+25°C	2	2.7		
			-55°C	1.7			
e_n	Equivalent input noise voltage	F = 1 kHz	+25°C		7		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent input noise current	F = 1 kHz	+25°C		0.8		$\frac{pA}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion	$V_{out} = (V_{CC}$-1 V)/5 Gain = -5.1 $V_{icm} = V_{CC}/2$	+25°C		0.01		%

Figure 1. Input offset voltage distribution

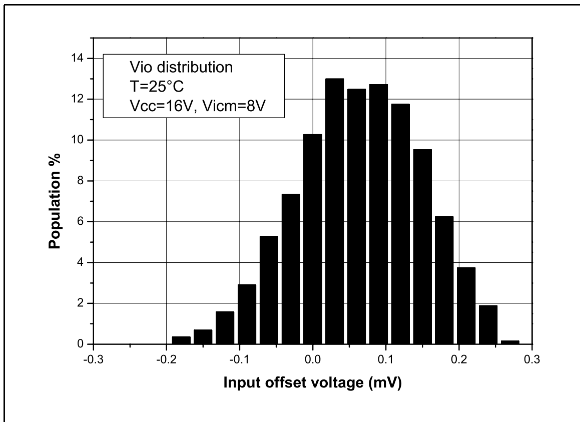


Figure 2. Input bias current vs. supply voltage

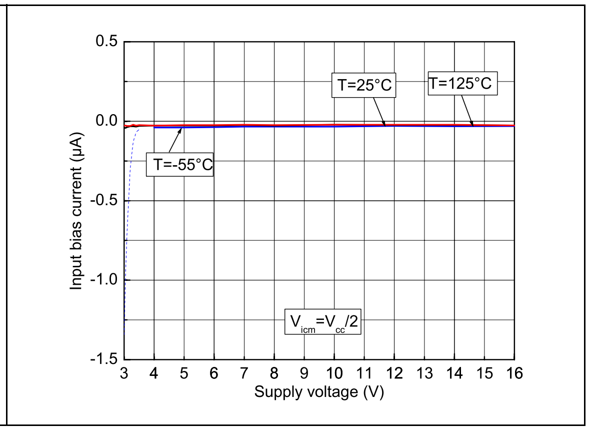


Figure 3. Input bias current vs. Vicm at V_{CC} = 3 V

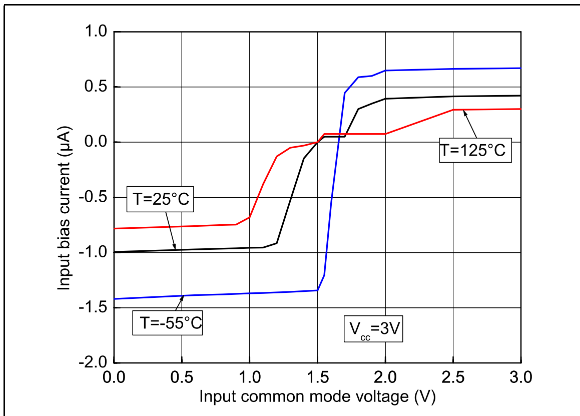


Figure 4. Input bias current vs. Vicm at V_{CC} = 4 V

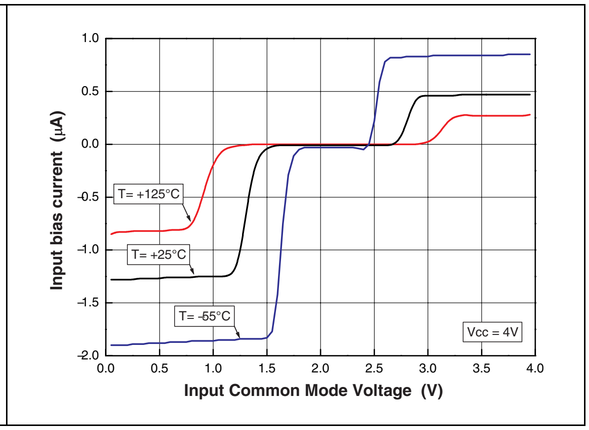


Figure 5. Input bias current vs. Vicm at V_{CC} = 16 V

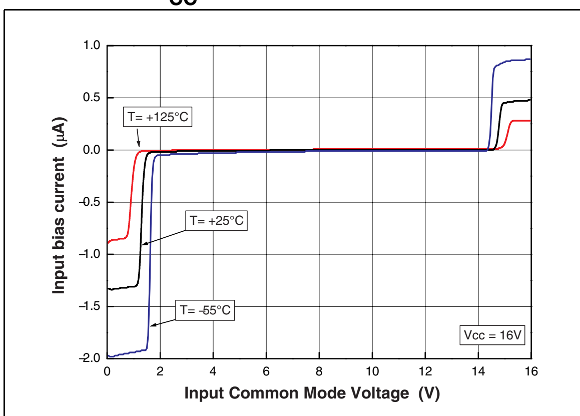


Figure 6. Supply current vs. Vicm in follower configuration at V_{CC} = 3 V

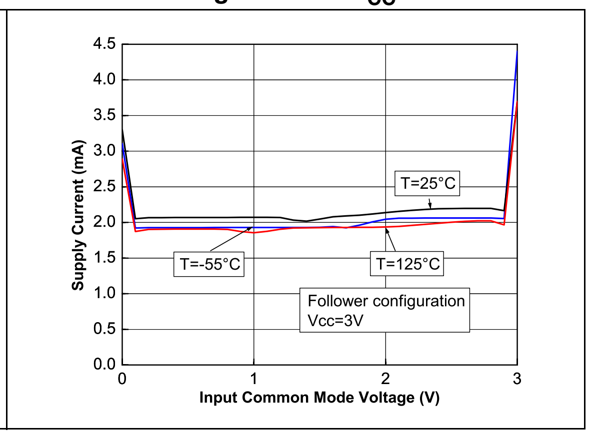


Figure 7. Supply current vs. Vicm in follower configuration at V_{CC} = 16 V

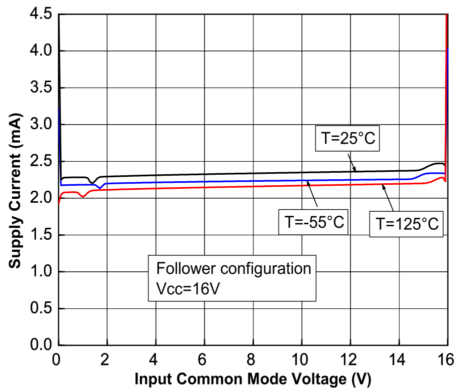


Figure 8. Supply current vs. supply voltage at V_{icm} = V_{CC}/2

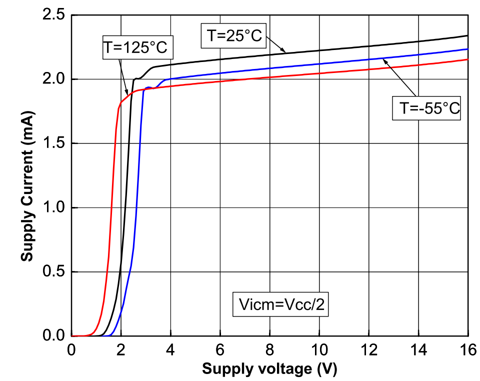


Figure 9. Output current vs. supply voltage at V_{icm} = V_{CC}/2

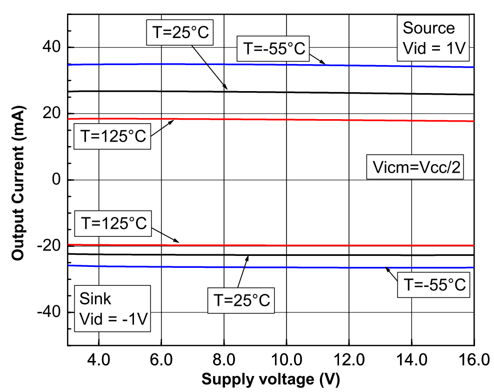


Figure 10. Output current vs. output voltage at V_{CC} = 3 V

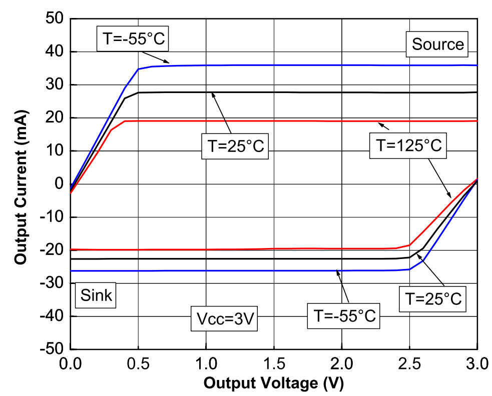


Figure 11. Output current vs. output voltage at V_{CC} = 16 V

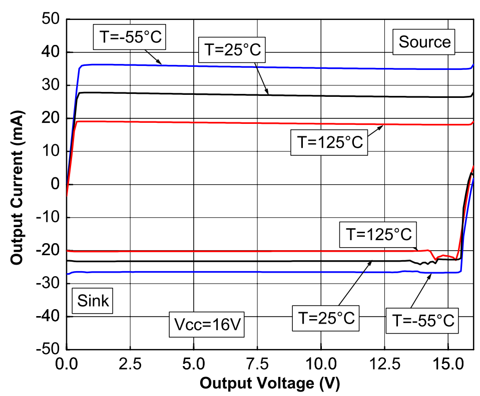


Figure 12. Differential input voltage vs. output voltage at V_{CC} = 3 V

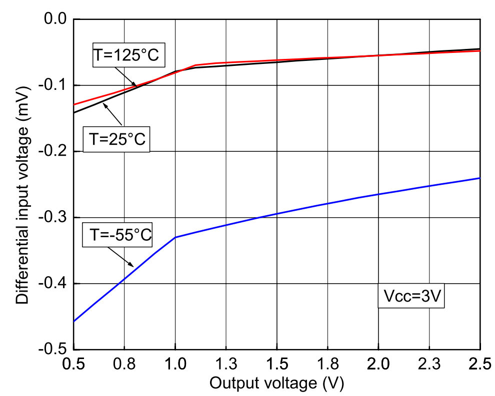


Figure 13. Differential input voltage vs. output voltage at V_{CC} = 16 V

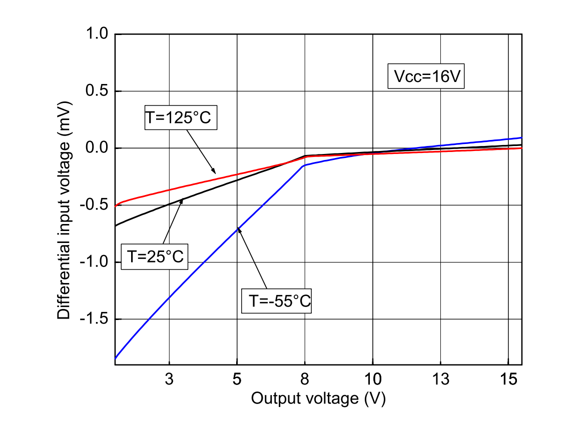


Figure 14. Noise vs. frequency at V_{CC}= 3 V and V_{CC} = 16 V

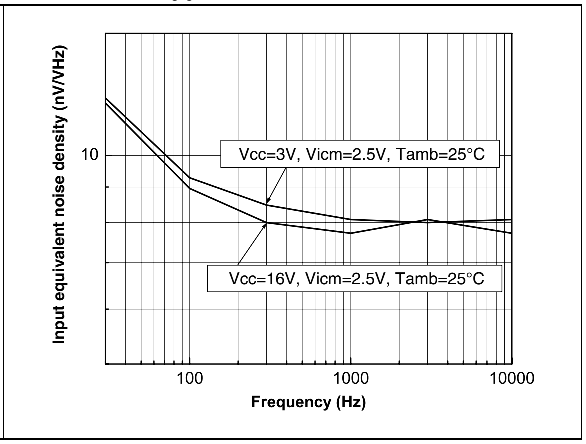


Figure 15. Voltage gain and phase vs. frequency at V_{icm} = 1.5 V

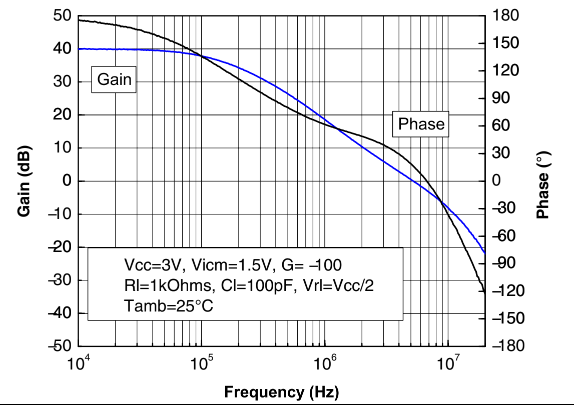


Figure 16. Voltage gain and phase vs. frequency at V_{icm} = 2.5 V

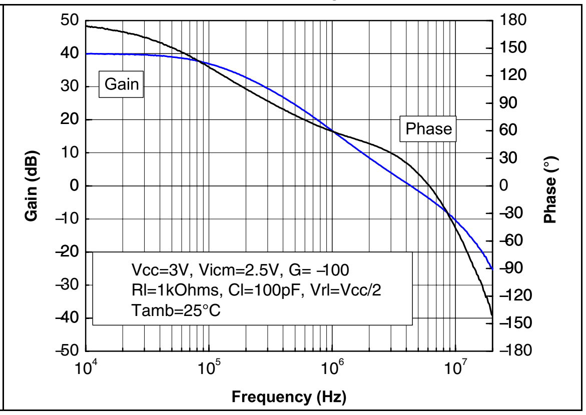


Figure 17. Voltage gain and phase vs. frequency at V_{icm} = 0.5 V

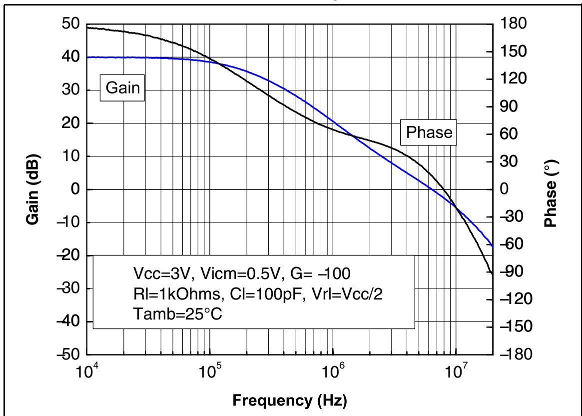


Figure 18. Voltage gain and phase vs. frequency at V_{icm} = 8 V

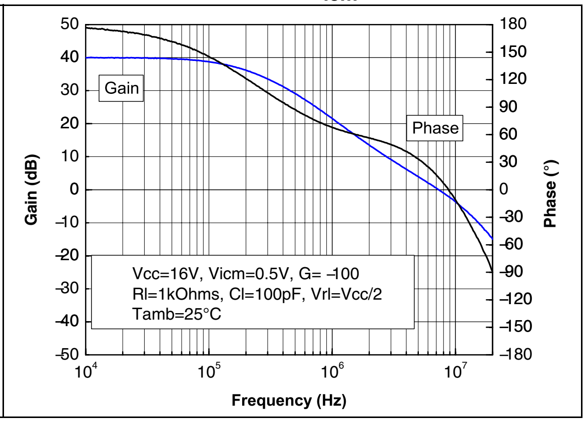


Figure 19. Voltage gain and phase vs. frequency at V_{icm} = 15.5 V

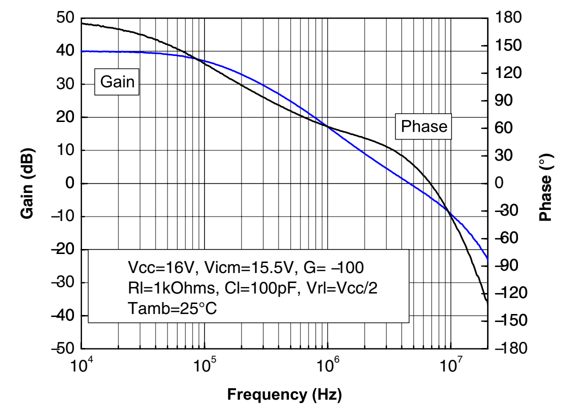


Figure 20. Voltage gain and phase vs. frequency at V_{icm} = 0.5 V

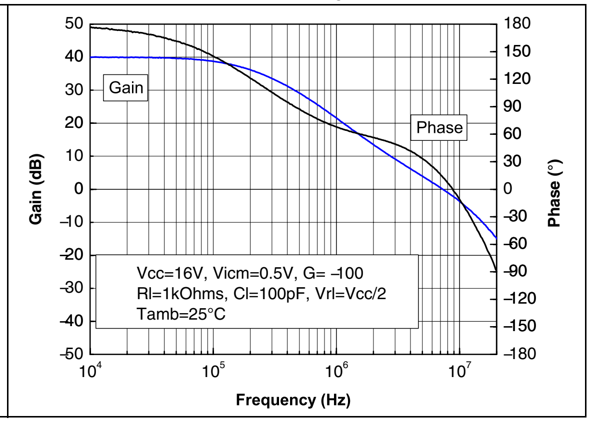


Figure 21. Inverting large signal pulse response at V_{CC} = 3 V, +25°C

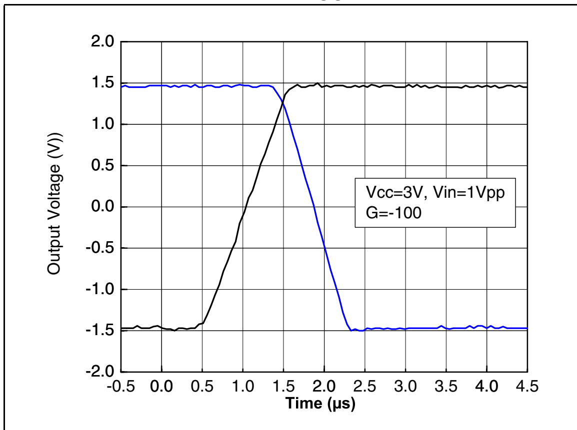
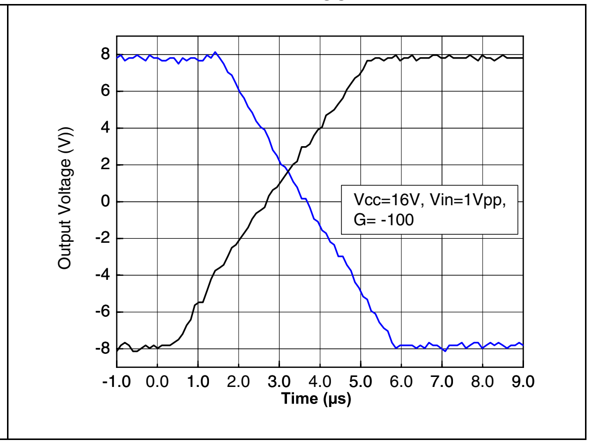


Figure 22. Inverting Large signal pulse response at V_{CC} = 16 V, +25°C



3 Achieving good stability at low gains

At low frequencies, the RHF43B can be used in a low gain configuration as shown in *Figure 23*. At lower frequencies, the stability is not affected by the value of the gain, which can be set close to 1 V/V (0 dB), and is reduced to its simplest expression G1=1+Rfb/Rg. Therefore, an R-C cell is added in the gain network so that the gain is increased (up to 5) at higher frequencies (where the stability of the amplifier could be affected). At higher frequencies, the gain becomes G2=1+Rfb/(Rg//R).

Figure 23. Low gain configuration

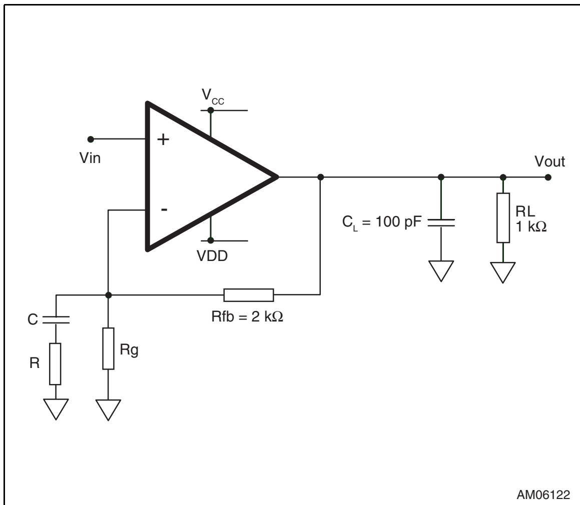
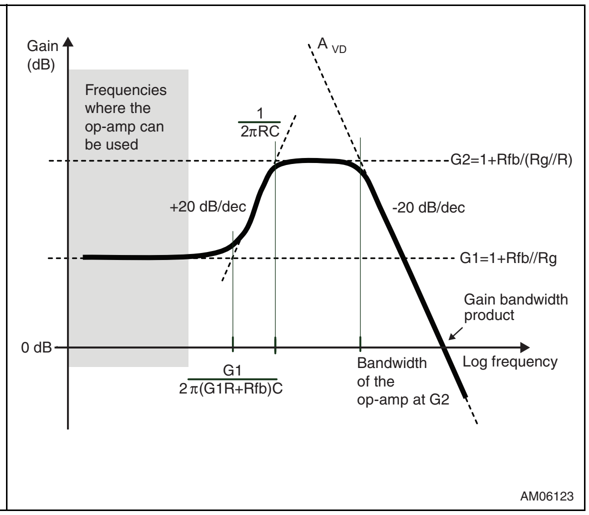


Figure 24. Closed-loop gain



Rg becomes a complex impedance. The closed-loop gain features a variation in frequency and can be expressed as:

$$\text{Gain} = G1\frac{1 + jC\omega \times \left(\frac{G1R + Rfb}{G1}\right)}{1 + jCR\omega}$$

where a pole appears at 1/2πRC and a zero at G1/2π(G1R+Rfb)C. The frequency can be plotted as shown in *Figure 24*.

Table 5. External components versus low-frequency gain

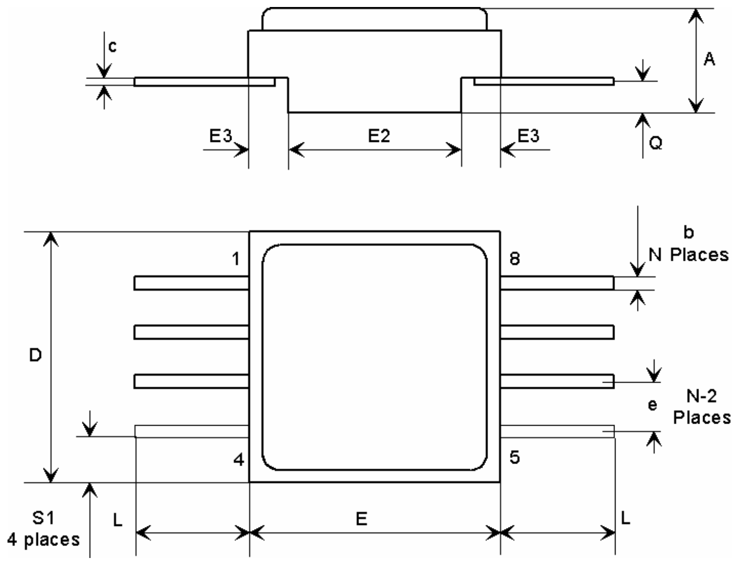
G1 (V/V)	R (Ω)	C (nF)	Rg (Ω)	Rfb (Ω)
1.1	510	1	20k	2k
2	510	1	2k	2k
3	510	1	1k	2k
4	510	1	750	2.4k
5	Not connected	Not connected	820	3.3k

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 Ceramic Flat-8 package information

Figure 25. Ceramic Flat-8 package mechanical drawing



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 6. Ceramic Flat-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.092
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

5 Ordering information

Table 7. Order codes

Order code	SMD pin	Quality level	Package	Lead finish	Packing	Marking	EPPL
RHF43BK1	-	Engineering model	Flat-8	Gold	Strip pack	RHF43BK1	-
RHF43BK-01V	5962F062370 1VXC	QMLV-Flight	Flat-8	Gold	Strip pack	5962F06237 01VXC	Y
RHF43BDIE2V	5962F062370 1V9A	QMLV-Flight	Die	-	Strip pack	-	-

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-May-2007	1	First public release.
10-Dec-2007	2	Changed name of pins on pinout diagram on cover page. Modified supply current values over temperature range in electrical characteristics. Power dissipation removed from AMR table.
29-Jan-2008	3	Added ELRS-free rad-hard design in description on cover page. Modified description of heavy ion latch-up (SEL) immunity parameter in *Table 1 on page 2*.
11-May-2009	4	Updated radiation immunity in *Features on page 1* and in *Table 1 on page 2*. Updated smb reference in *Features on page 1*.
15-Oct-2009	5	Updated test conditions for Avd vs. Vicm in *Table 3 on page 3* and *Table 4 on page 5*. Updated input current and voltage noise in *Table 3*. Updated order codes in *Table 7 on page 14*.
30-Mar-2010	6	Added *Figure 4* and *Figure 5*. Added information for ambient temperature in *Table 3* and *Table 4*. Added *Chapter 3*.
20-Aug-2010	7	Corrected "L" dimension in *Table 6*.
27-Jul-2011	8	Added *Note: on page 13* and in the "Pin connections" diagram on the coverpage.

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