RHF350

Rad-hard 550 MHz low noise operational amplifier

Datasheet — production data

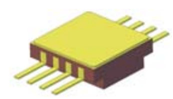
Features

- Bandwidth: 550 MHz (unity gain)
- Quiescent current: 4 mA
- Slew rate: 940 V/µs
- Input noise: 1.5 nV/√Hz
- Distortion: SFDR = -66 dBc (10 MHz, $1V_{pp}$)
- 2.8 V_{pp} minimum output swing on 100 Ω load for a +5 V supply
- 5 V power supply
- 300 krad MIL-STD-883 1019 ELDRS free compliant
- SEL immune at 125 °C, LET up to 110 MEV.cm^2/mg
- SET characterized, LET up to 110 MEV.cm^2/mg
- QMLV qualified
- Available in ceramic Flat-8S package

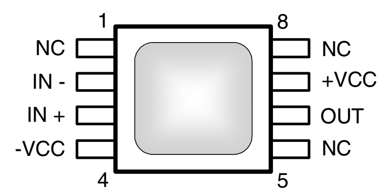
Applications

- Communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high energy physics
- Harsh radiation environments
- ADC drivers

Ceramic Flat-8S



Pin connections
(top view)



The upper metallic lid is not electrically connected to any pin, nor to the IC die inside the package.

Description

The RHF350 device is a current feedback operational amplifier that uses very high speed complementary technology to provide a bandwidth of up to 550 MHz while drawing only 4 mA of quiescent current. With a slew rate of 940 V/µs and an output stage optimized for driving a standard 100 Ω load, this circuit is highly suitable for applications where speed and power-saving are the main requirements. The device is a single operator available in a Flat-8 hermetic ceramic package, saving board space as well as providing excellent thermal and dynamic performance.

Table 1. Device summary(1)

Reference	SMD	Quality level	Package	Lead finish	Mass	EPPL	Temperature range
RHF350K1	-	Engineering model	Flat-8S	Gold	0.45 g	-	-55 °C to +125 °C
RHF350K-01V	5962F0723201VXC	QML-V model					

1. Contact ST sales for information about the specific conditions for products in QML-Q versions.

This is information on a product in full production. www.st.com

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Contents

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1 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{id}	Differential input voltage(2)	+/-0.5	V
V_{in}	Input voltage range(3)	+/-2.5	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Flat-8 thermal resistance junction to ambient	50	°C/W
R_{thjc}	Flat-8 thermal resistance junction to case	30	°C/W
P_{max}	Flat-8 maximum power dissipation(4) (T_{amb} = 25 °C) for T_j = 150 °C	830	mW
ESD	HBM: human body model(5) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 2 0.5	kV
	MM: machine model(6) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 200 60	V
	CDM: charged device model(7) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 1.5 1.5	kV
	Latch-up immunity	200	mA

1. All voltages values are measured with respect to the ground pin.
2. Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed V_{CC} +0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on all amplifiers.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. This is a minimum value.
   Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin.

Table 3. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 5.5	V
V_{icm}	Common mode input voltage	$-V_{CC}$ +1.5 V to $+V_{CC}$ -1.5 V	V
T_A	Ambient temperature range	-55 to +125	°C

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2 Electrical characteristics

Note: All electrical parameters apply both pre and post irradiation. Post irradiation data are guaranteed by qualification, they are not tested in production.

Table 4. Radiations

		Value	Unit
TID	High dose rate (50 - 300 rad / sec.) up to	300	krad
Heavy-ions	SEL immunity (at 125 °C) up to SEU characterized up to	110	MeV.cm²/mg

Table 5. Electrical characteristics for V_{CC} = ±2.5 V, (unless otherwise specified)

Symbol	Parameter	Test conditions	Temp.(1)	Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Input offset voltage		+125 °C	-4	1	4	mV
			+25 °C	-4	0.4	4	
			-55 °C	-4	0.8	4	
I_{ib+}	Non-inverting input bias current		+125 °C		8.5	35	µA
			+25 °C		9	35	
			-55 °C		9	35	
I_{ib-}	Inverting input bias current		+125 °C		2.5	25	µA
			+25 °C		2	20	
			-55 °C		1.8	25	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±1 V	+125 °C	50	55		dB
			+25 °C	54	57		
			-55 °C	50	58		
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	ΔV_{CC} = 3.5 V to 5 V	+125 °C	55	87		dB
			+25 °C	68	87		
			-55 °C	55	88		
PSRR	Power supply rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{out}$)	ΔV_{CC} = 200 mV_{pp} at 1 kHz	+25 °C		51		dB
I_{CC}	Supply current	No load	+125 °C		3.8	4.9	mA
			+25 °C		4	4.9	
			-55 °C		4	4.9	

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Table 5. Electrical characteristics for V_{CC} = ±2.5 V, (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Temp.[1]	Min.	Typ.	Max.	Unit
Dynamic performance and output characteristics							
R_{OL}	Transimpedance	ΔV_{out}= ±1 V, R_L = 100 Ω	+125 °C	150	244		kΩ
			+25 °C	170	260		
			-55 °C	150	276		
Bw	Small signal -3 dB bandwidth	R_L = 100 Ω, A_V = +1	+25 °C		550		MHz
		R_L = 100 Ω, A_V = +2	+25 °C		390		
		R_L = 100 Ω, A_V = +10	+25 °C		125		
		R_L = 100 Ω, A_V = -2	+125 °C	250	380		
			+25 °C	250	425		
			-55 °C	250	466		
SR	Slew rate[2]	V_{out} = 2 V_{pp}, A_V = +2, R_L = 100 Ω	+25 °C	700	940		V/µs
V_{OH}	High level output voltage	R_L = 100 Ω	+125 °C	1.3	1.6		V
			+25 °C	1.44	1.55		
			-55 °C	1.3	1.5		
V_{OL}	High level output voltage	R_L = 100 Ω	+125 °C		-1.6	-1.3	
			+25 °C		-1.55	-1.44	
			-55 °C		-1.5	-1.3	
I_{sink}	Output sink current	Output to GND	+125 °C	135	210		mA
			+25 °C	135	225		
			-55 °C	135	225		
I_{source}	Output source current	Output to GND	+125 °C		-200	-140	
			+25 °C		-225	-140	
			-55 °C		-240	-140	

1. $T_{min} < T_{amb} < T_{max}$: worst case of the parameter on a standard sample across the temperature range. The evaluation is done on 50 units in the SO-8 plastic package.
2. Not physically tested. Guaranteed by design, measured on bench.

Table 6. Closed-loop gain and feedback components

Gain (V/V)	+ 1	- 1	+ 2	- 2	+ 10	- 10
R_{fb} (Ω)	820	300	300	300	300	300

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Figure 1. Frequency response, positive gain

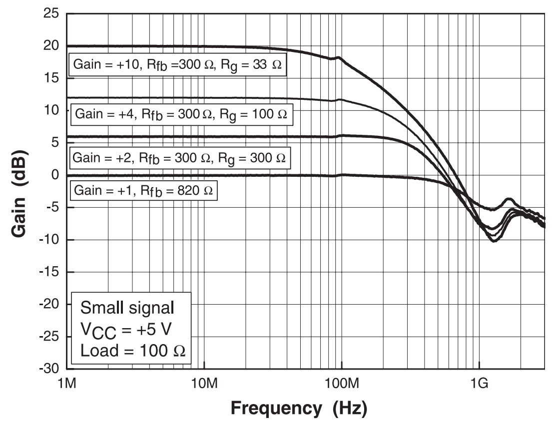

Figure 2. Flatness, gain = +1

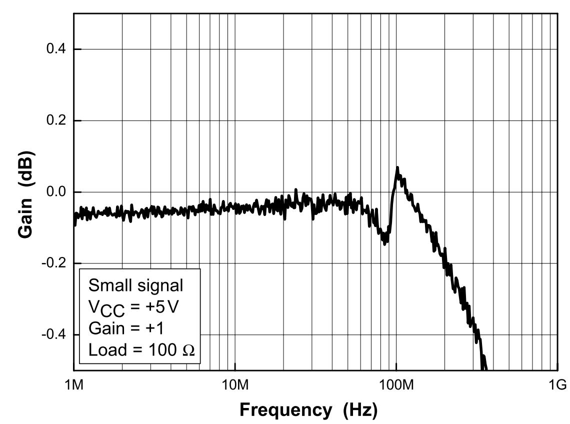

Figure 3. Flatness, gain = +2

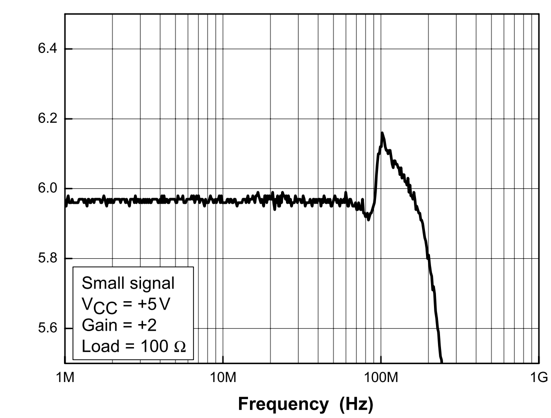

Figure 4. Flatness, gain = +4

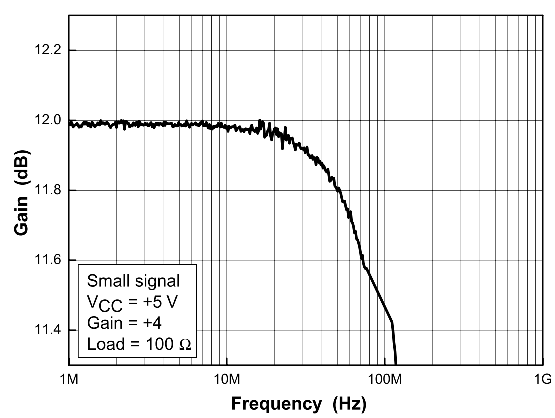

Figure 5. Flatness, gain = +10

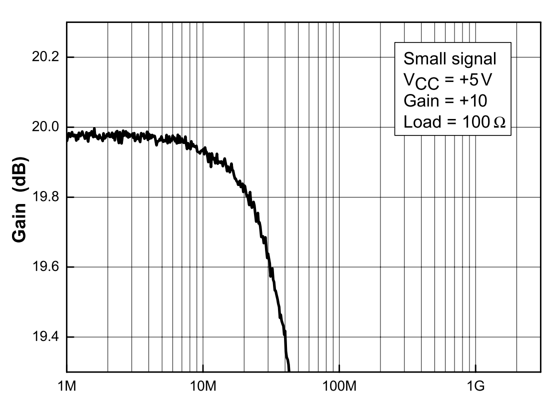

Figure 6. Slew rate

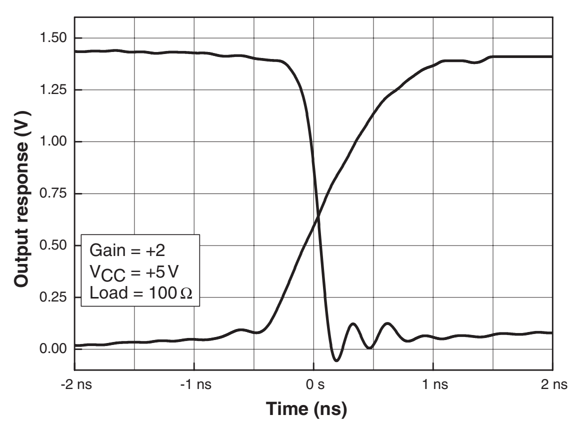

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Figure 7. I_{sink}

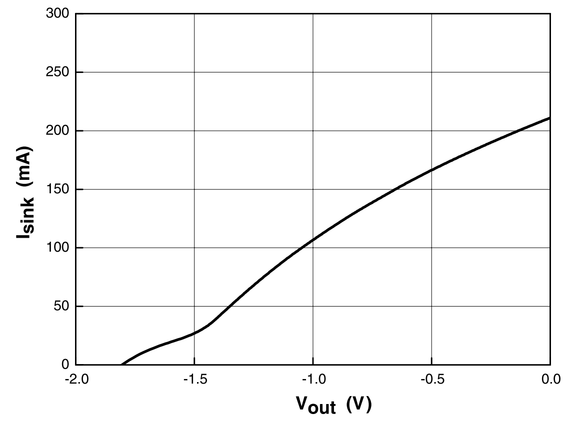

Figure 8. I_{source}

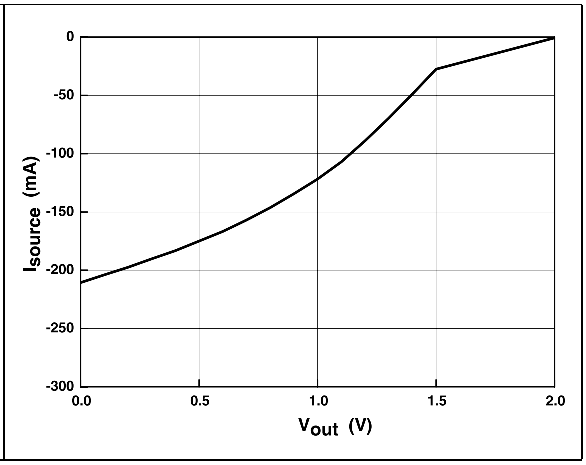

Figure 9. Input current noise vs. frequency

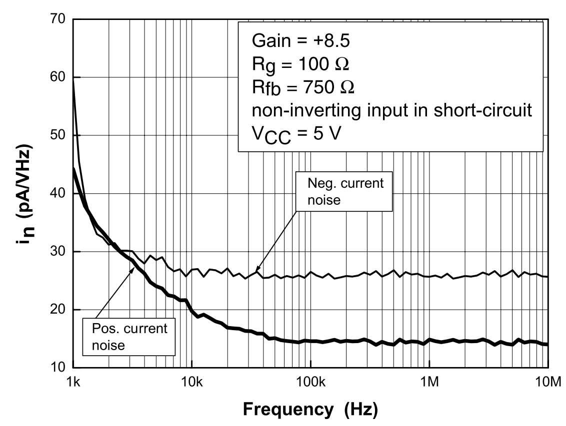

Figure 10. Input voltage noise vs. frequency

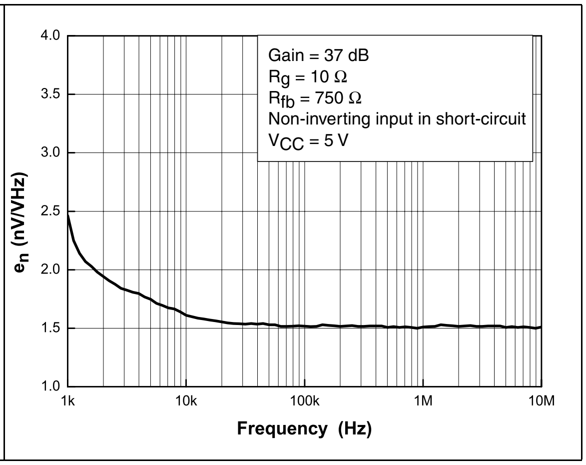

Figure 11. Quiescent current vs. V_{CC}

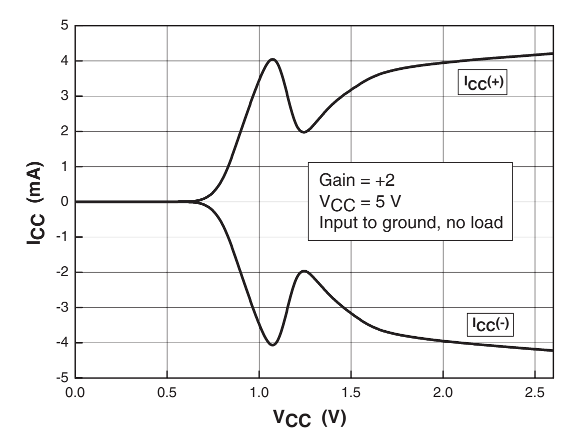

Figure 12. Noise

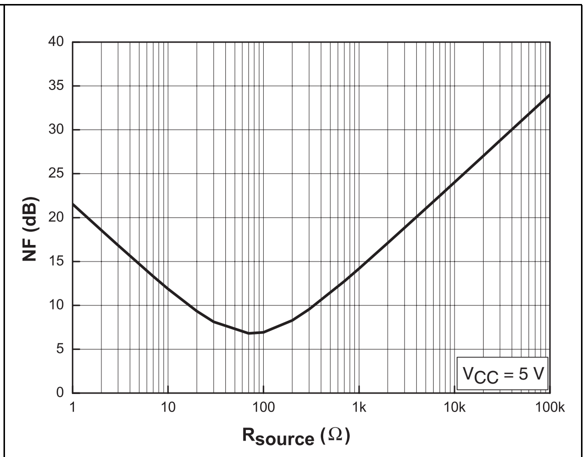

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Figure 13. Distortion vs. output amplitude

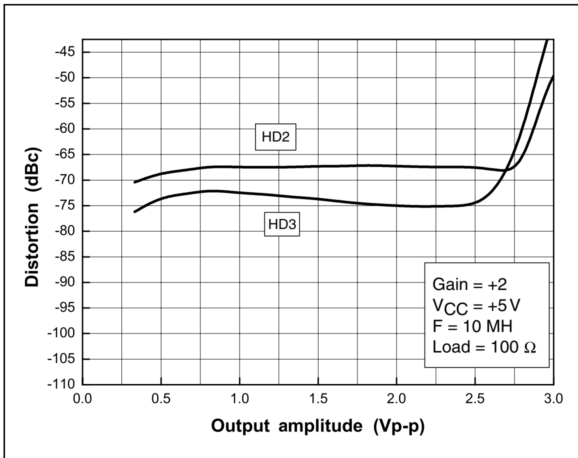

Figure 14. Output amplitude vs. load

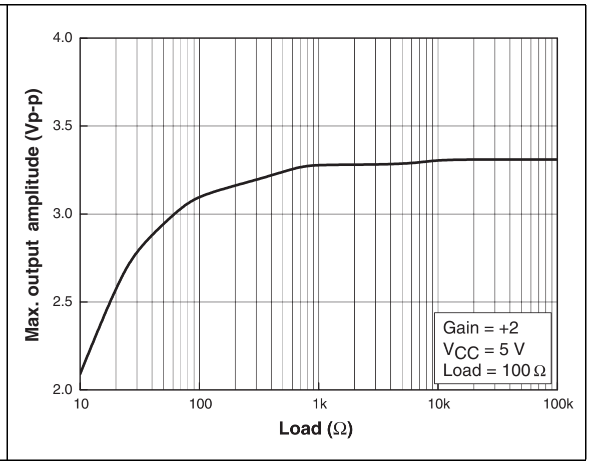

Figure 15. Reverse isolation vs. frequency

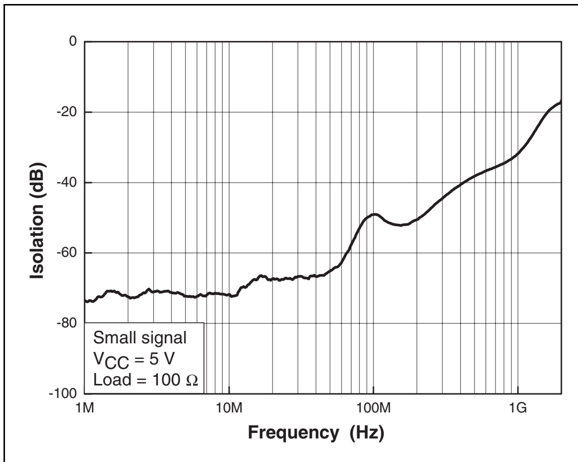

Figure 16. SVR vs. temperature

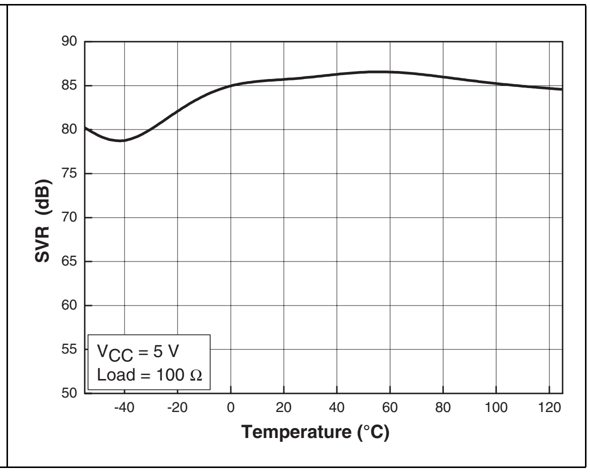

Figure 17. I_{out} vs. temperature

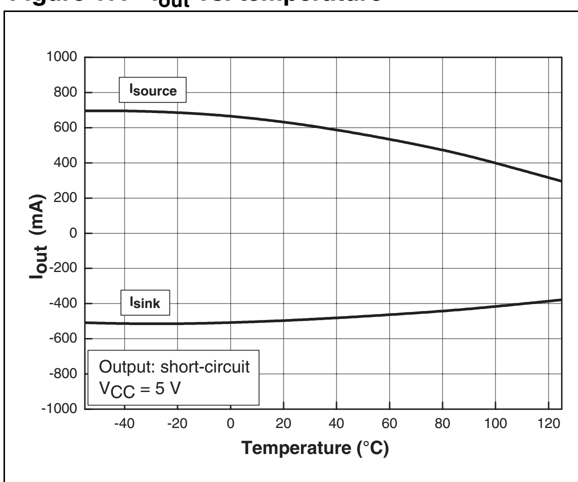

Figure 18. R_{OL} vs. temperature

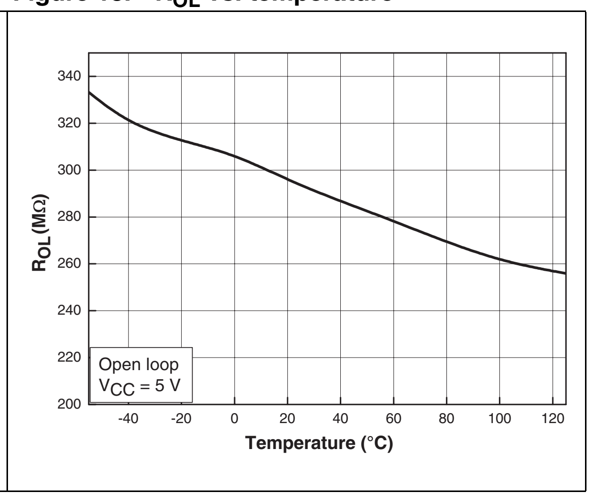

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Figure 19. CMR vs. temperature

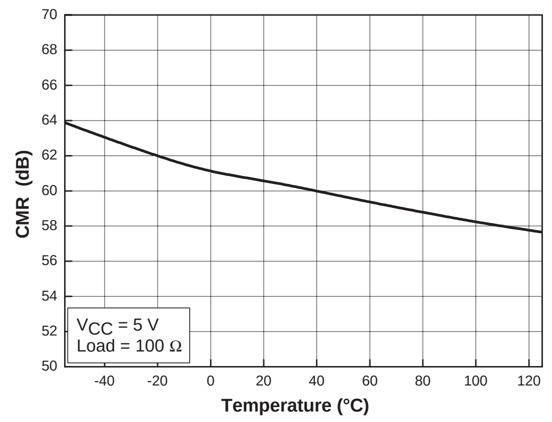


Figure 20. I_{bias} vs. temperature

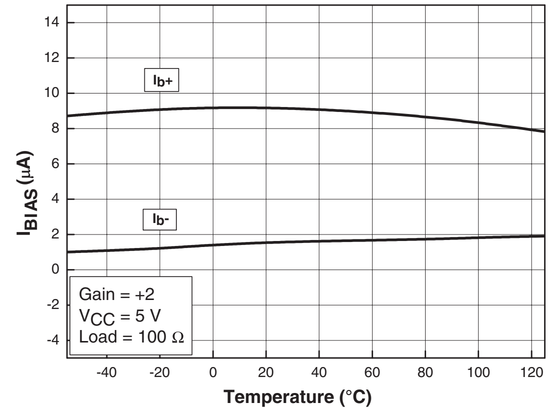


Figure 21. V_{io} vs. temperature

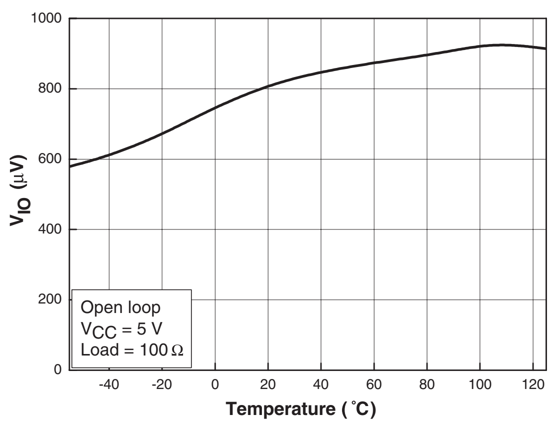


Figure 22. V_{OH} and V_{OL} vs. temperature

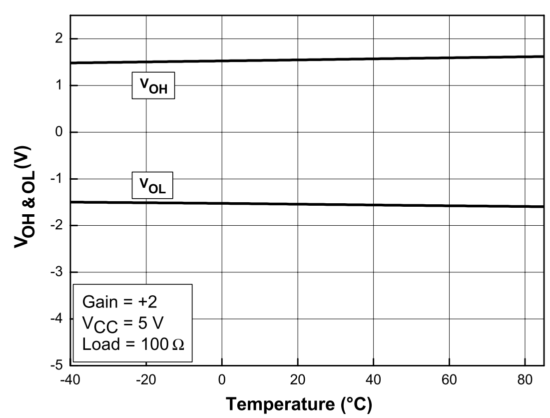
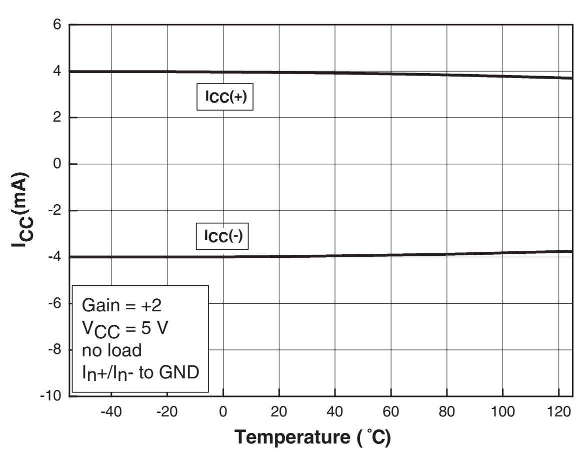


Figure 23. I_{CC} vs. temperature



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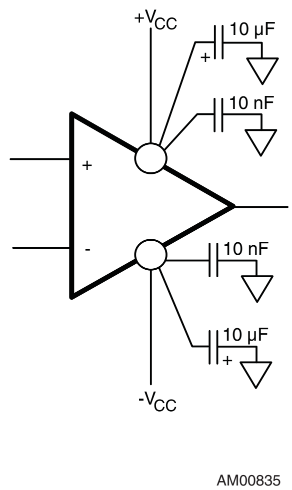
3 Power supply considerations

Correct power supply bypassing is very important to optimize performance in high-frequency ranges. The bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1 µF is necessary to minimize the distortion. For better quality bypassing, a 10 nF capacitor can be added. It should also be placed as close as possible to the IC pins. The bypass capacitors must be incorporated for both the negative and positive supply.

Figure 24. Circuit for power supply bypassing



Single power supply

In the event that a single supply system is used, biasing is necessary to obtain a positive output dynamic range between the 0 V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier provides an output swing from +0.9 V to +4.1 V on a 100 Ω load.

The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (35 µA maximum) as 1% of the current through the resistance divider, to keep a stable mid-supply two resistances of 750 Ω can be used.

The input provides a high-pass filter with a break frequency below 10 Hz which is necessary to remove the original 0 V DC component of the input signal, and to set it at $+V_{CC}/2$.

Figure 25 on page 11 illustrates a 5 V single power supply configuration. A capacitor C_G is added to the gain network to ensure a unity gain at low frequencies in order to keep the right DC component at the output. C_G contributes to a high-pass filter with $R_{fb}//R_G$ and its value is calculated with regard to the cut-off frequency of this low-pass filter.

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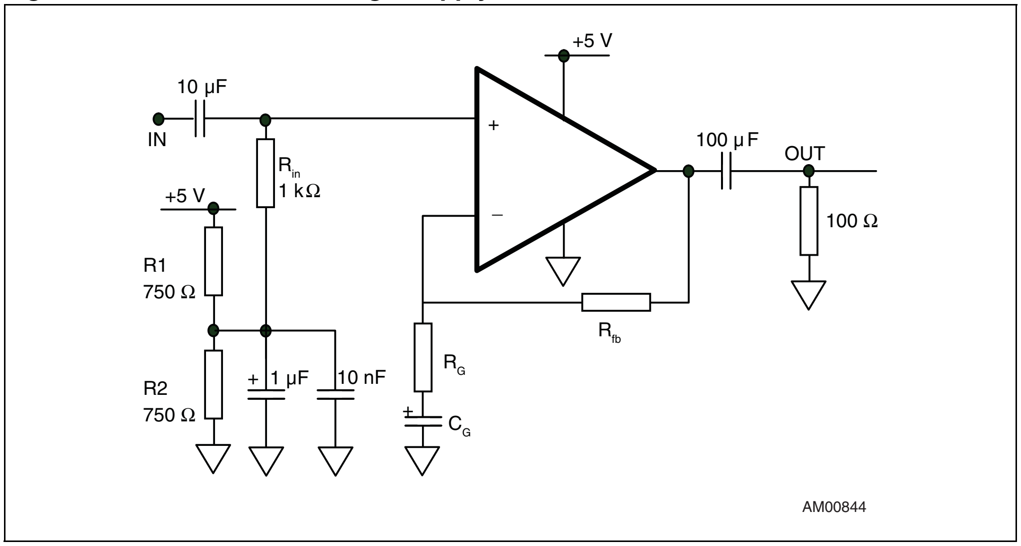
Figure 25. Circuit for +5 V single supply



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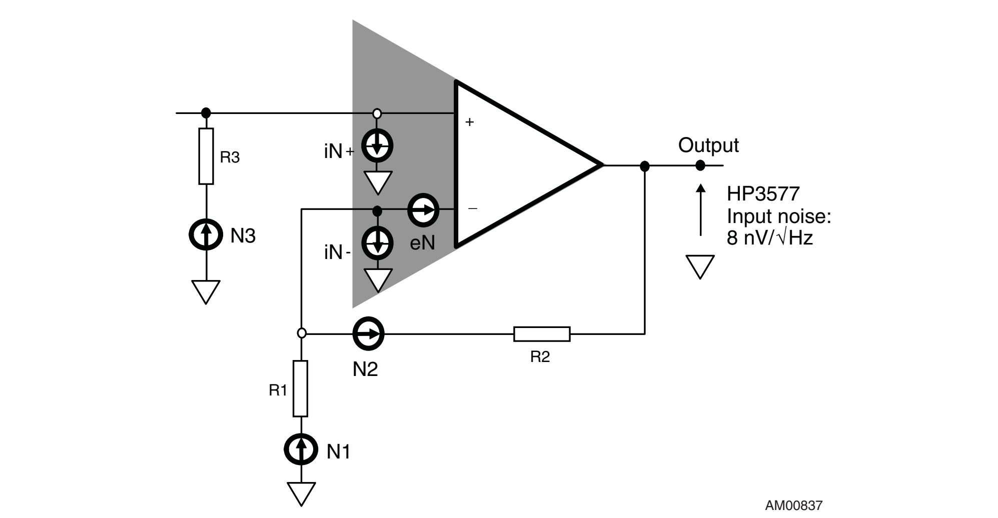
4 Noise measurements

The noise model is shown in *Figure 26*.

- eN: input voltage noise of the amplifier.
- iNn: negative input current noise of the amplifier.
- iNp: positive input current noise of the amplifier.

Figure 26. Noise model



The thermal noise of a resistance *R* is:

Equation 1

$$\sqrt{4kTR\Delta F}$$

where *ΔF* is the specified bandwidth.

On a 1 Hz bandwidth the thermal noise is reduced to:

Equation 2

$$\sqrt{4kTR}$$

where *k* is the Boltzmann's constant, equal to 1,374.E(-23)J/°K. *T* is the temperature (°K).

The output noise eNo is calculated using the superposition theorem. However, *eNo* is not the simple sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in *Equation 3*.

Equation 3

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

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Equation 4

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

Equation 5

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2}$$

The input noise is called **equivalent input noise** because it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (*eNo/g*).

After simplification of the fourth and the fifth term of *Equation 4* we obtain:

Equation 6

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

4.1 Measurement of the input voltage noise *eN*

If we assume a short-circuit on the non-inverting input (R3 = 0), from *Equation 6* we can derive:

Equation 7

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}$$

In order to easily extract the value of *eN*, the resistance *R2* will be chosen to be as low as possible. On the other hand, the gain must be large enough.

R3 = 0, gain: g = 100

4.2 Measurement of the negative input current noise *iNn*

To measure the negative input current noise *iNn*, we set R3 = 0 and use *Equation 7*. This time, the gain must be lower in order to decrease the thermal noise contribution.

R3 = 0, gain: g = 10

4.3 Measurement of the positive input current noise *iNp*

To extract *iNp* from *Equation 5*, a resistance *R3* is connected to the non-inverting input. The value of *R3* must be chosen in order to keep its thermal noise contribution as low as possible against the *iNp* contribution.

R3 = 100 W, gain: g = 10

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5 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series of equations.

Equation 8

$$V_{out} = C_0 + C_1 V_{in} + C_2 V^2{}_{in} + \ldots + C_n V^n{}_{in}$$

Where the input is $V_{in} = A\sin\omega t$, C_0 is the DC component, $C_1 (V_{in})$ is the fundamental and C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

Equation 9

$$V_{in} = A\sin\omega_1 t + A\sin\omega_2 t$$

then:

Equation 10

$$V_{out} = C_0 + C_1(A\sin\omega_1 t + A\sin\omega_2 t) + C_2(A\sin\omega_1 t + A\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + A\sin\omega_2 t)^n$$

From this expression, we can extract the distortion terms, and the intermodulation terms from a single sine wave.

- Second-order intermodulation terms IM2 by the frequencies $(\omega_1 - \omega_2)$ and $(\omega_1 + \omega_2)$ with an amplitude of $C2A^2$.
- Third-order intermodulation terms IM3 by the frequencies $(2\omega_1 - \omega_2)$, $(2\omega_1 + \omega_2)$, $(-\omega_1 + 2\omega_2)$ and $(\omega_1 + 2\omega_2)$ with an amplitude of $(3/4)C3A^3$.

The intermodulation product of the driver is measured by using the driver as a mixer in a summing amplifier configuration (*Figure 27*). In this way, the non-linearity problem of an external mixing device is avoided.

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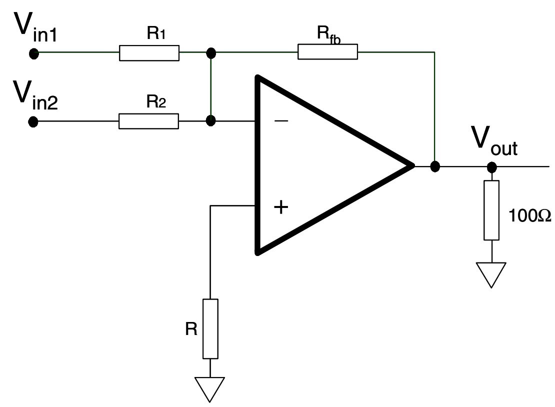
Figure 27. Inverting summing amplifier



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6 Inverting amplifier biasing

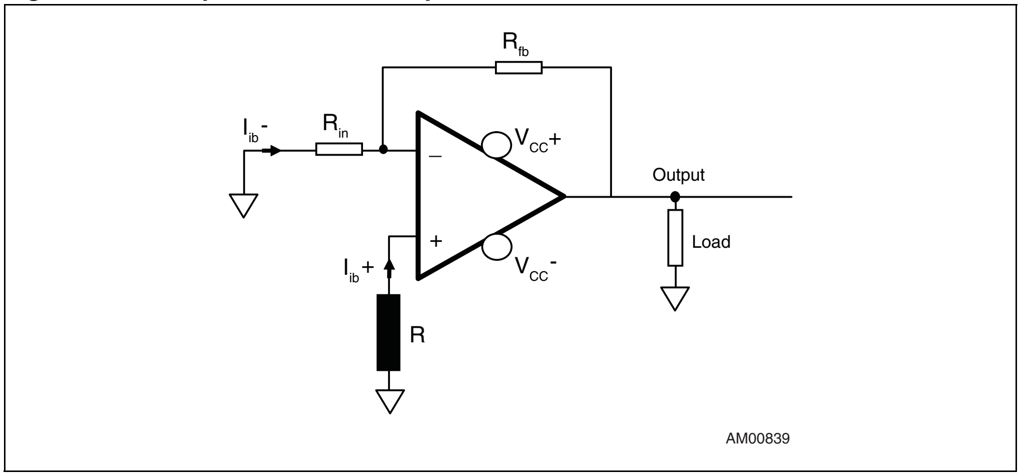
A resistance is necessary to achieve good input biasing, such as resistance *R* shown in *Figure 28*.

The value of this resistance is calculated from the negative and positive input bias current. The aim is to compensate for the offset bias current, which can affect the input offset voltage and the output DC component. Assuming I_{ib-}, I_{ib+}, R_{in}, R_{fb} and a 0 V output, the resistance *R* is:

Equation 11

$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

Figure 28. Compensation of the input bias current



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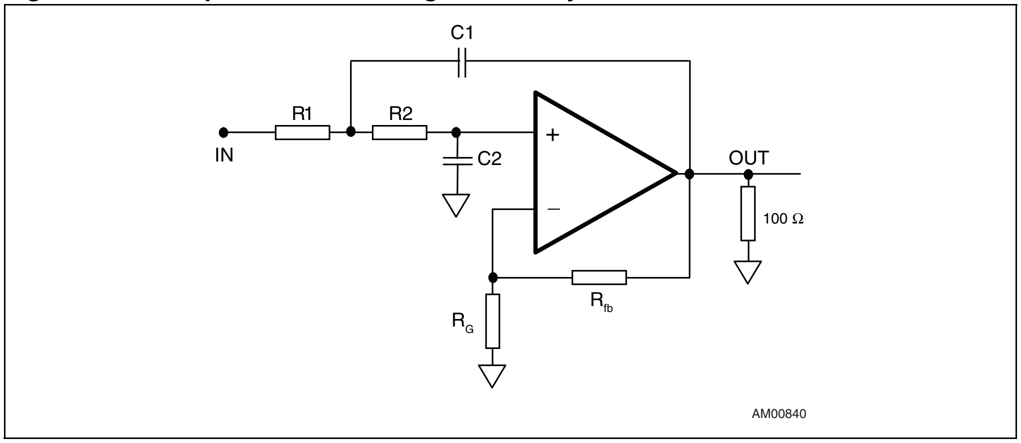
7 Active filtering

Figure 29. Low-pass active filtering, Sallen-Key



From the resistors R_{fb} and R_G we can directly calculate the gain of the filter in a classic non-inverting amplification configuration.

Equation 12

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression is the response of the system.

Equation 13

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

Equation 14

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated by *Equation 15:*

Equation 15

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

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The higher the gain, the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use very stable resistor and capacitor values. In the case of R1= R2 = R:

Equation 16

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

Due to a limited selection of capacitor values in comparison with resistor values, we can set C1= C2 = C, so that:

Equation 17

$$\zeta = \frac{2R_2 - R_1\frac{R_{fb}}{R_g}}{2\sqrt{R_1R_2}}$$

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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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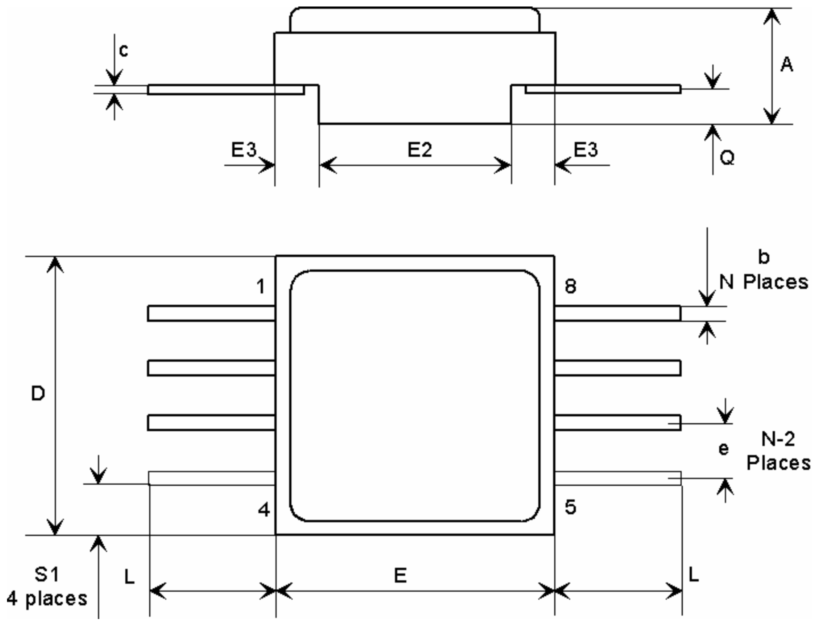
Ceramic Flat-8S package information

Figure 30. Ceramic Flat-8S package outline



1. The upper metallic lid is not electrically connected to any pin, nor to the IC dice inside the package.

Table 7. Ceramic Flat-8S package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L		3.00			0.118	
Q	0.66	0.79	0.92	0.026	0.031	0.092
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

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9 Ordering information

Table 8. Order codes

Order code	Description	Temperature range	Package	Marking	Packing
RHF350K1	Engineering model	-55 °C to +125 °C	Flat-8S	RHF350K1	Conductive strip pack
RHF350K-01V	QMLV-Flight			5962F0723201VXC	

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10 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-May-2009	1	Initial release.
12-Jul-2010	2	Added *Mass* in *Features* on cover page. Added *Table 1: Device summary* on cover page, with full ordering information. Changed temperature limits in *Table 5*.
27-Jul-2011	3	Added Note: on page 18 and in the "Pin connections" diagram on the coverpage.
03-Aug-2012	4	Updated *Table 5*. with values after radiations. Replaced note on page 18 with footnote. Minor corrections throughout document.

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