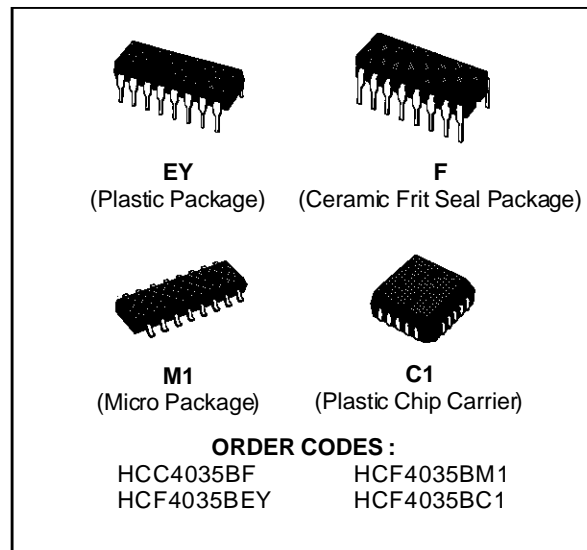


**4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER**

- 4-STAGE CLOCKED SHIFT OPERATION
- SYNCHRONOUS PARALLEL ENTRY ON ALL 4 STAGES
- JK INPUTS ON FIRST STAGE
- ASYNCHRONOUS TRUE/COMPLEMENT CONTROL ON ALL OUTPUTS
- STATIC FLIP-FLOP OPERATION ; MASTER-SLAVE CONFIGURATION
- BUFFERED INPUTS AND OUTPUTS
- HIGH SPEED 12MHz (typ.) AT V<sub>DD</sub> = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURR 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

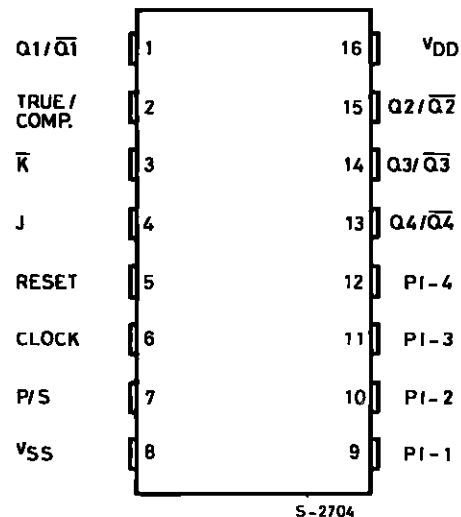
When JK inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.



**DESCRIPTION**

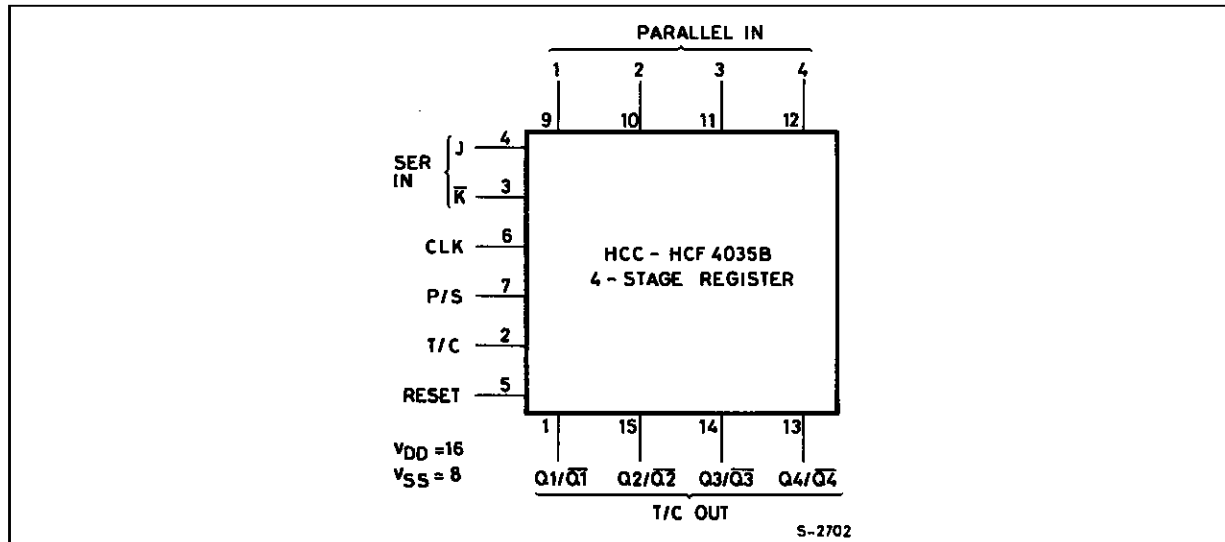
The **HCC4035B** (extended temperature range) and **HCF4035B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4035B** is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transitions. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. JK input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications.

**PIN CONNECTIONS**



# HCC/HCF4035B

## FUNCTIONAL DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}^*$	Supply Voltage : <b>HCC</b> Types <b>HCF</b> Types	- 0.5 to + 20 - 0.5 to + 18	V V
$V_i$	Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
$I_i$	DC Input Current (any one input)	$\pm 10$	mA
$P_{tot}$	Total Power Dissipation (per package) Dissipation per Output Transistor for $T_{op} =$ Full Package-temperature Range	200 100	mW mW
$T_{op}$	Operating Temperature : <b>HCC</b> Types <b>HCF</b> Types	- 55 to + 125 - 40 to + 85	$^{\circ}C$ $^{\circ}C$
$T_{stg}$	Storage Temperature	- 65 to + 150	$^{\circ}C$

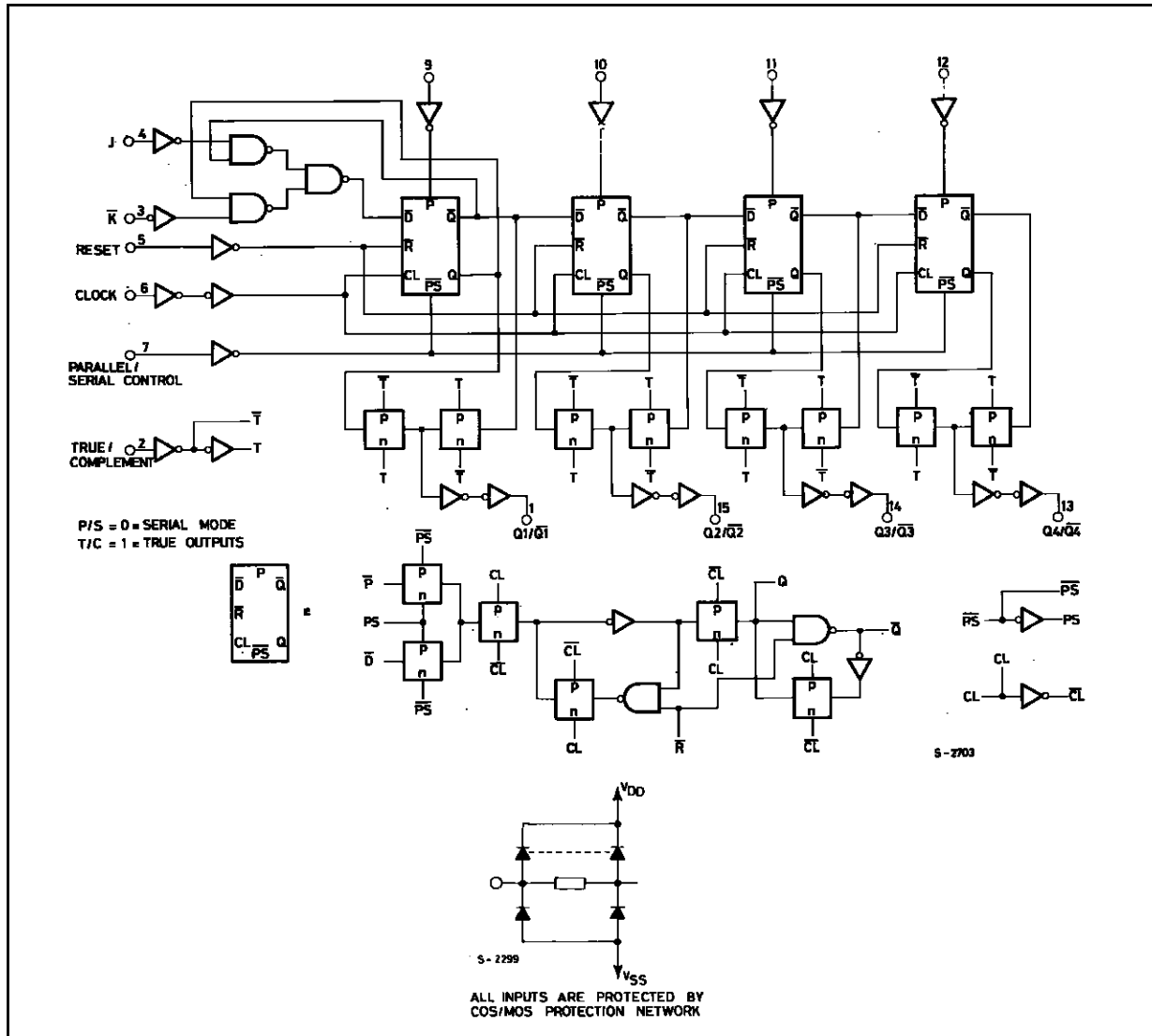
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

\* All voltage values are referred to  $V_{SS}$  pin voltage.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage: <b>HCC</b> Types <b>HCF</b> Types	3 to 18 3 to 15	V V
$V_i$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature: <b>HCC</b> Types <b>HCF</b> Types	-55 to +125 -40 to +85	$^{\circ}C$ $^{\circ}C$

LOGIC DIAGRAM



TRUTH TABLE  
FIRST STAGE

Clock ( $\phi$ )	$t_{n-1}$ (inputs)				$t_n$ (outputs)
	J	$\bar{K}$	R	$Q_{n-1}$	$Q_n$
	0	X	0	0	0
	1	X	0	0	1
	X	0	0	1	0
	1	0	0	$Q_{n-1}$	$\overline{Q_{n-1}}$ Toggle Mode
	X	1	0	1	1
	X	X	0	$Q_{n-1}$	$Q_{n-1}$
X	X	X	1	X	0

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>Low</sub> *		25°C			T <sub>High</sub> *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
V <sub>OH</sub>	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95	V	
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V <sub>OL</sub>	Output Low Voltage		5/0		< 1	5		0.05			0.05		V	
			10/0		< 1	10		0.05			0.05			
			15/0		< 1	15		0.05			0.05			
V <sub>IH</sub>	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5	V	
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V <sub>IL</sub>	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		V	
				9/1	< 1	10		3			3			
				13.5/1.5	< 1	15		4			4			
I <sub>OH</sub>	Output Drive Current	HCC Types	0/ 5	2.5		5	- 2		- 1.6	- 3.2		- 1.15	mA	
			0/ 5	4.6		5	- 0.64		- 0.51	- 1		- 0.36		
			0/10	9.5		10	- 1.6		- 1.3	- 2.6		- 0.9		
			0/15	13.5		15	- 4.2		- 3.4	- 6.8		- 2.4		
		HCF Types	0/ 5	2.5		5	- 1.53		- 1.36	- 3.2		- 1.1		
			0/ 5	4.6		5	- 0.52		- 0.44	- 1		- 0.36		
I <sub>OL</sub>	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage Current	HCC Types	0/18	Any Input		18		$\pm$ 0.1		$\pm 10^{-5}$	$\pm$ 0.1		$\pm$ 1	
			0/15											
		HCF Types	0/15											15
C <sub>I</sub>	Input Capacitance		Any Input						5	7.5		pF		

\* T<sub>Low</sub> = -55°C for HCC device : - 40°C for HCF device.

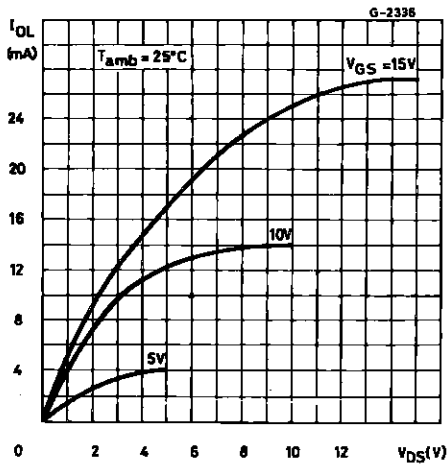
\* T<sub>High</sub> = + 125°C for HCC device : + 85°C for HCF device.

The Noise Margin for both "1" and "0" level is : 1V min. with V<sub>DD</sub> = 5V, 2V min. with V<sub>DD</sub> = 10V, 2.5V min. with V<sub>DD</sub> = 15V.

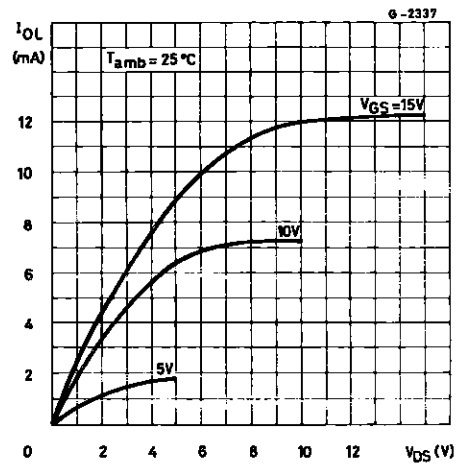
**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$ , typical temperature coefficient for all  $V_{DD} = 0.3\%/^{\circ}\text{C}$ , all input rise and fall time = 20ns)

Symbol	Parameter	Test Conditions		Value			Unit
			$V_{DD}$ (V)	Min.	Typ.	Max.	
<b>CLOCKED OPERATION</b>							
$t_{PLH}, t_{PHL}$	Propagation Delay Time		5		250	500	ns
			10		100	200	
			15		75	150	
$t_{THL}, t_{TLH}$	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
$f_{CL}$	Maximum Clock Input Frequency		5	2	4		MHz
			10	6	12		
			15	8	16		
$t_w$	Clock Pulse Width		5		100	200	ns
			10		45	90	
			15		30	60	
$t_r, t_f$	Clock Input Rise or Fall Time		5		15		$\mu\text{s}$
			10		15		
			15		15		
$t_{setup}$	Data Setup Time J/K Lines		5		110	220	ns
			10		40	80	
			15		30	60	
$t_{setup}$	Data Setup Time Parallel-In-Lines		5		70	140	ns
			10		25	50	
			15		20	40	
<b>RESET OPERATION</b>							
$t_{PLH}, t_{PHL}$	Propagation Delay Time		5		230	460	ns
			10		100	200	
			15		80	160	
$t_w$	Reset Pulse Width		5		125	250	ns
			10		55	110	
			15		40	40	

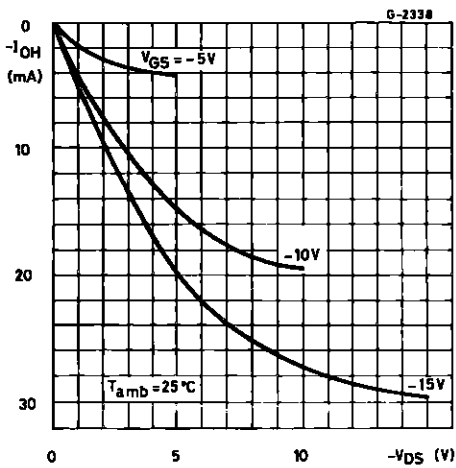
Typical Output Low (sink) Current Characteristics.



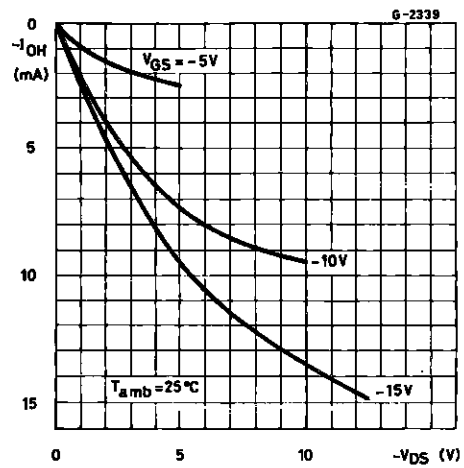
Minimum Output Low (sink) Current Characteristics.



Typical Output High (source) Current Characteristics.

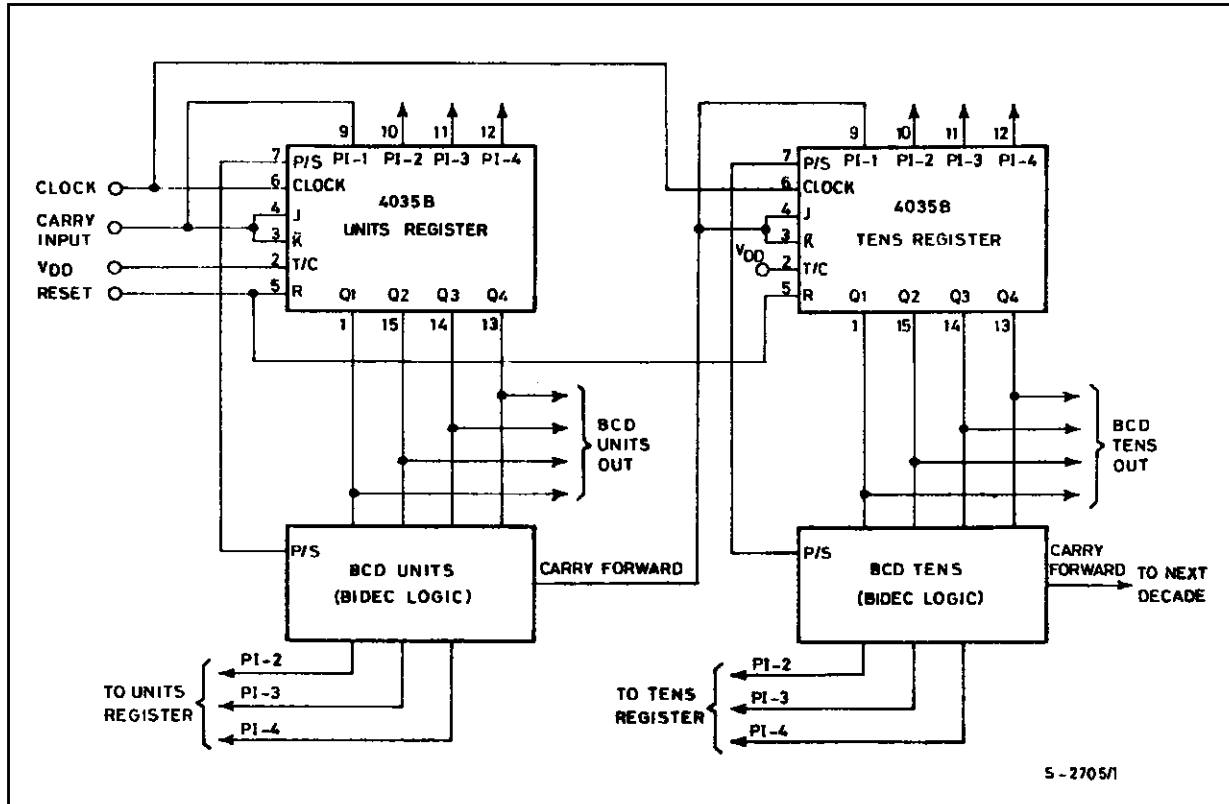


Minimum Output High (source) Current Characteristics.



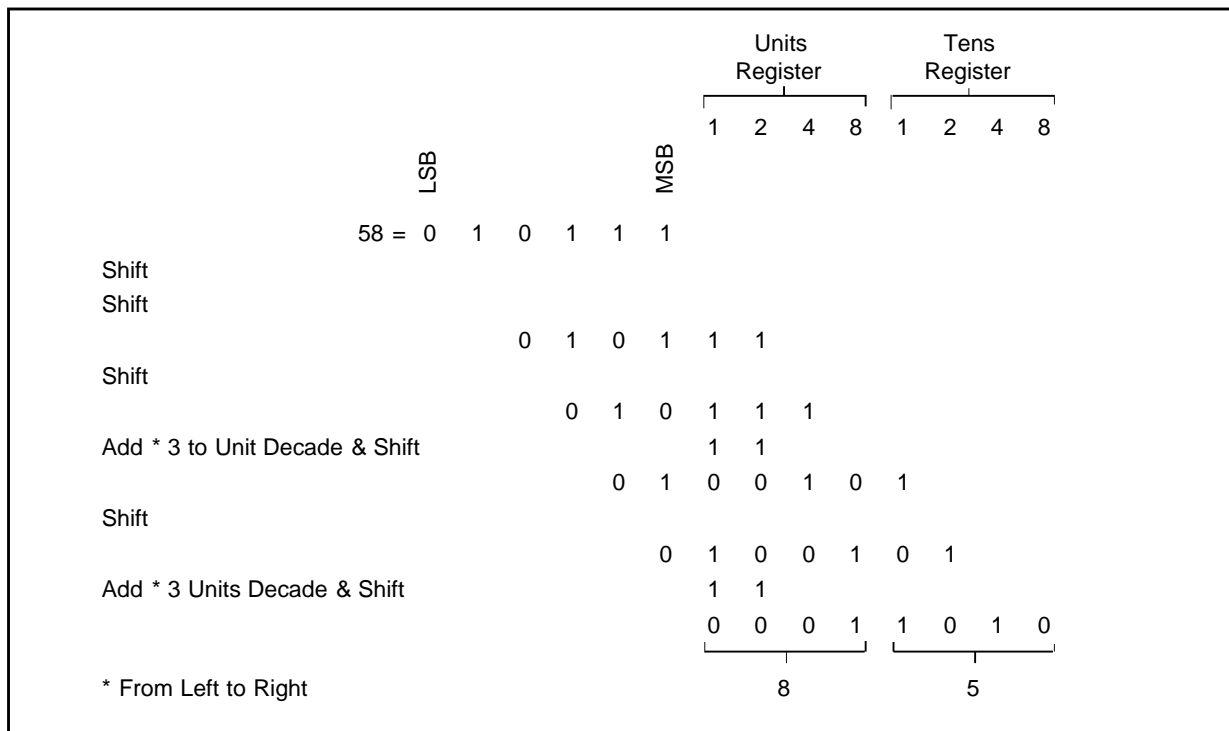
TYPICAL APPLICATIONS

BINARY-TO-BCD CONVERTER



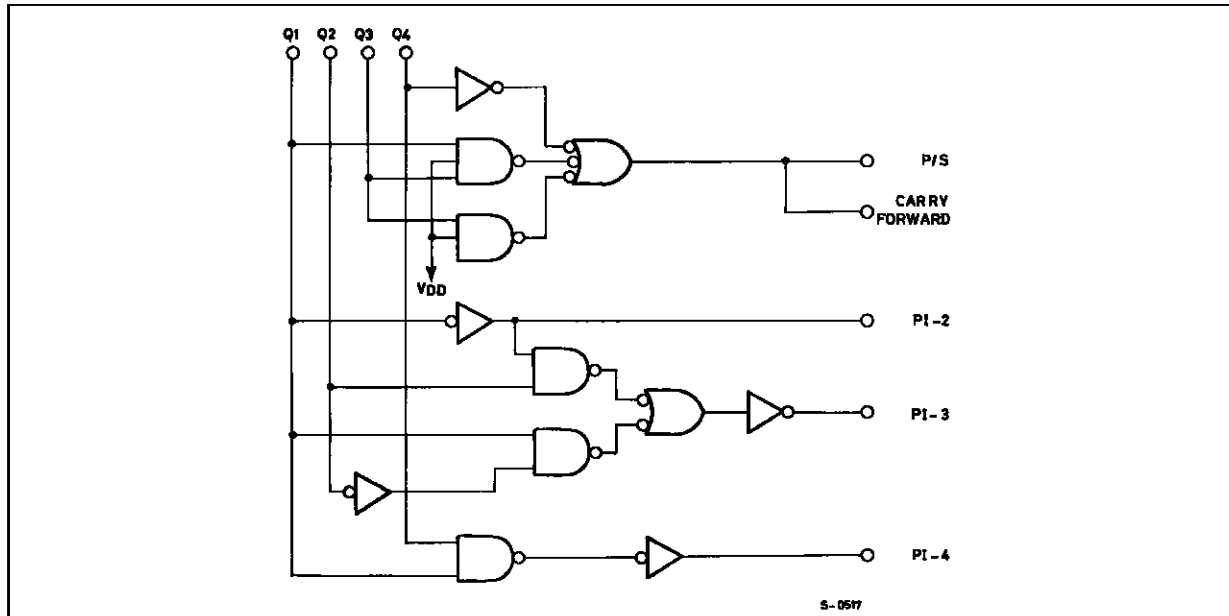
5-2705/1

EXAMPLE OF BINARY-TO-BCD CONVERSION

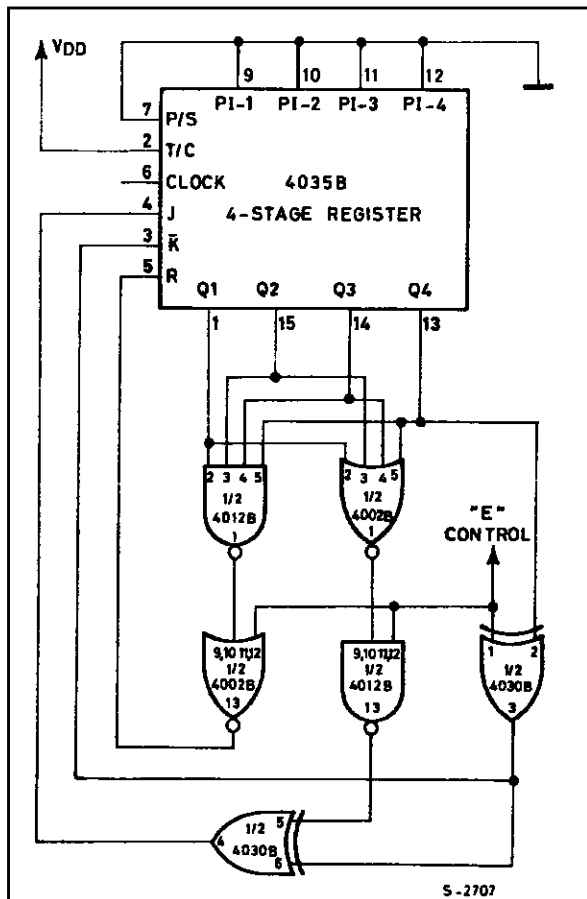


TYPICAL APPLICATIONS

BIDEC LOGIC



DOUBLE SEQUENCE GENERATOR



STATE SEQUENCES

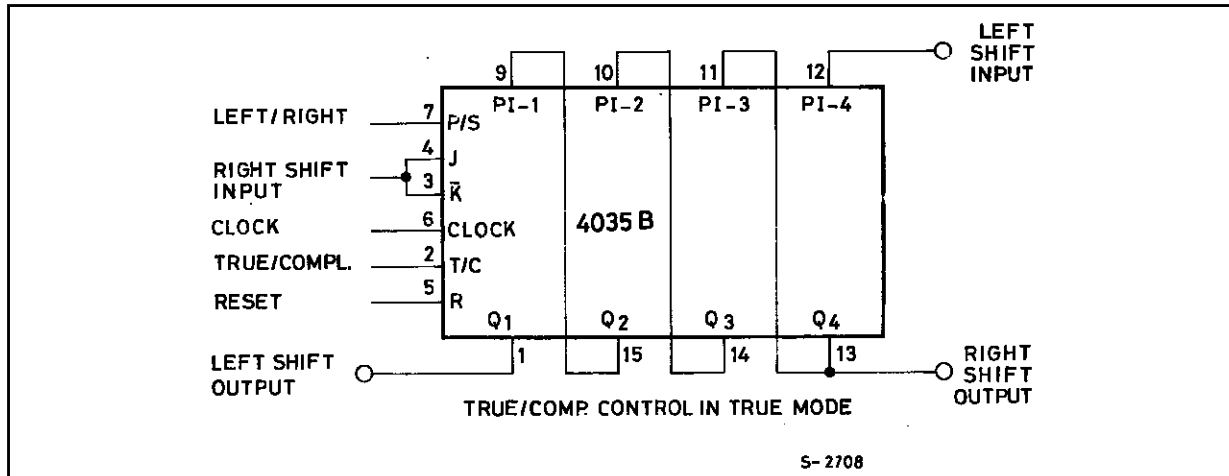
Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E).

	Control = E = 0					1			
	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>		Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
0	A	B	C	D	15	A	B	C	D
1	0	0	0	0	14	0	0	1	1
2	1	0	0	0	13	1	0	1	1
5	0	1	0	0	10	0	1	0	1
10	1	0	1	0	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0



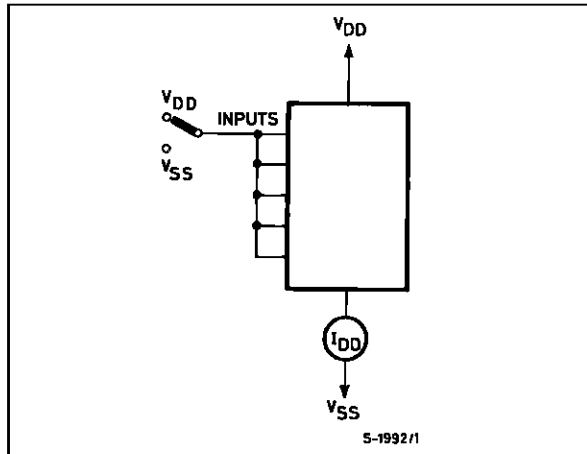
TYPICAL APPLICATIONS

SHIFT LEFT/SHIFT RIGHT REGISTER

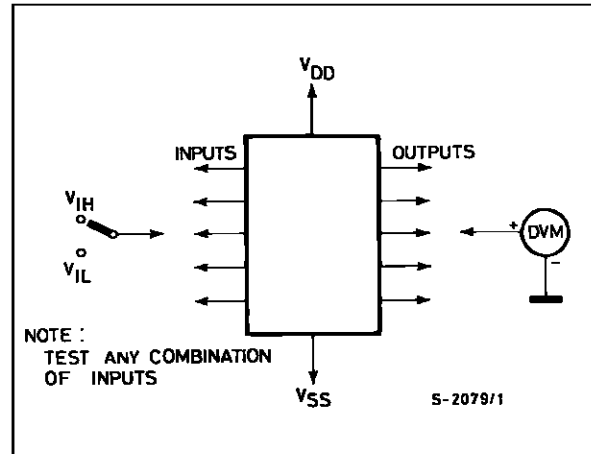


TEST CIRCUITS

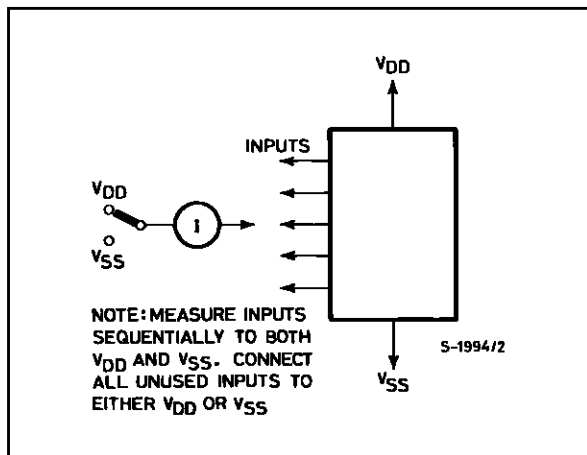
Quiescent Device Current



Input Voltage.



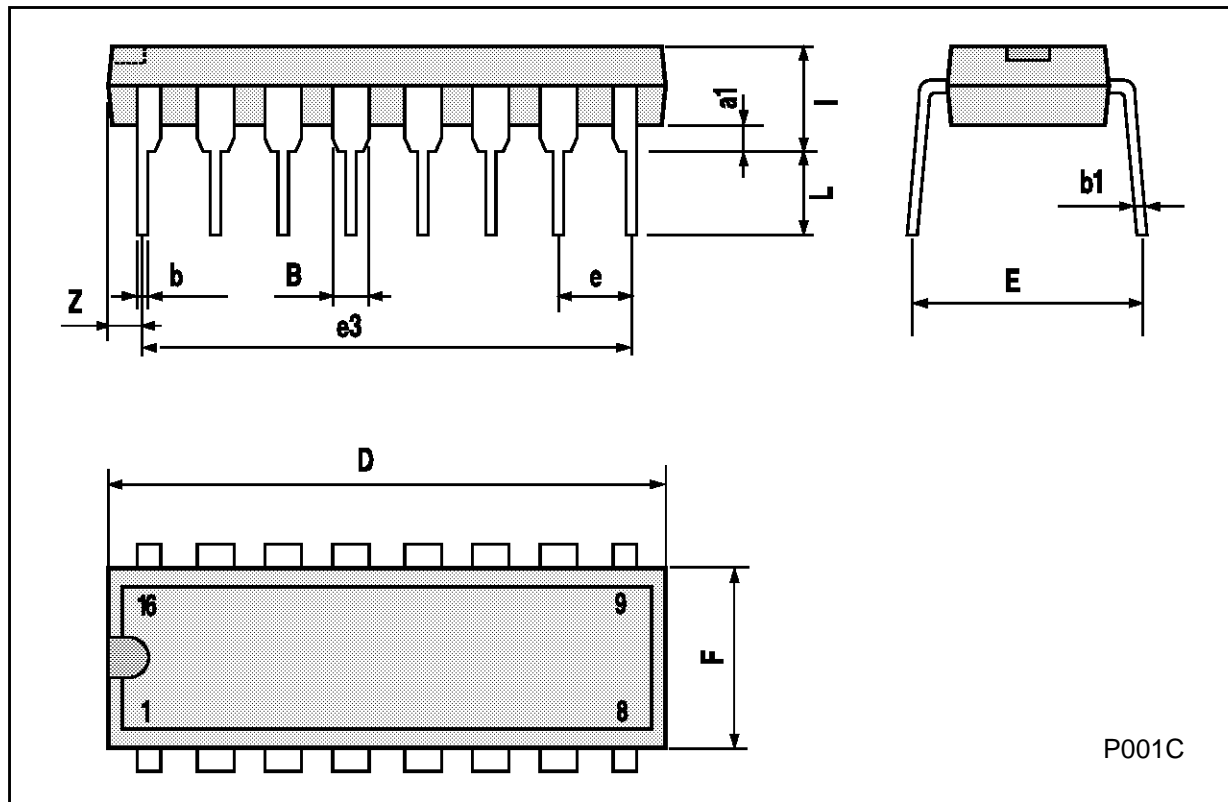
Input Current.



# HCC/HCF4035B

## Plastic DIP16 (0.25) MECHANICAL DATA

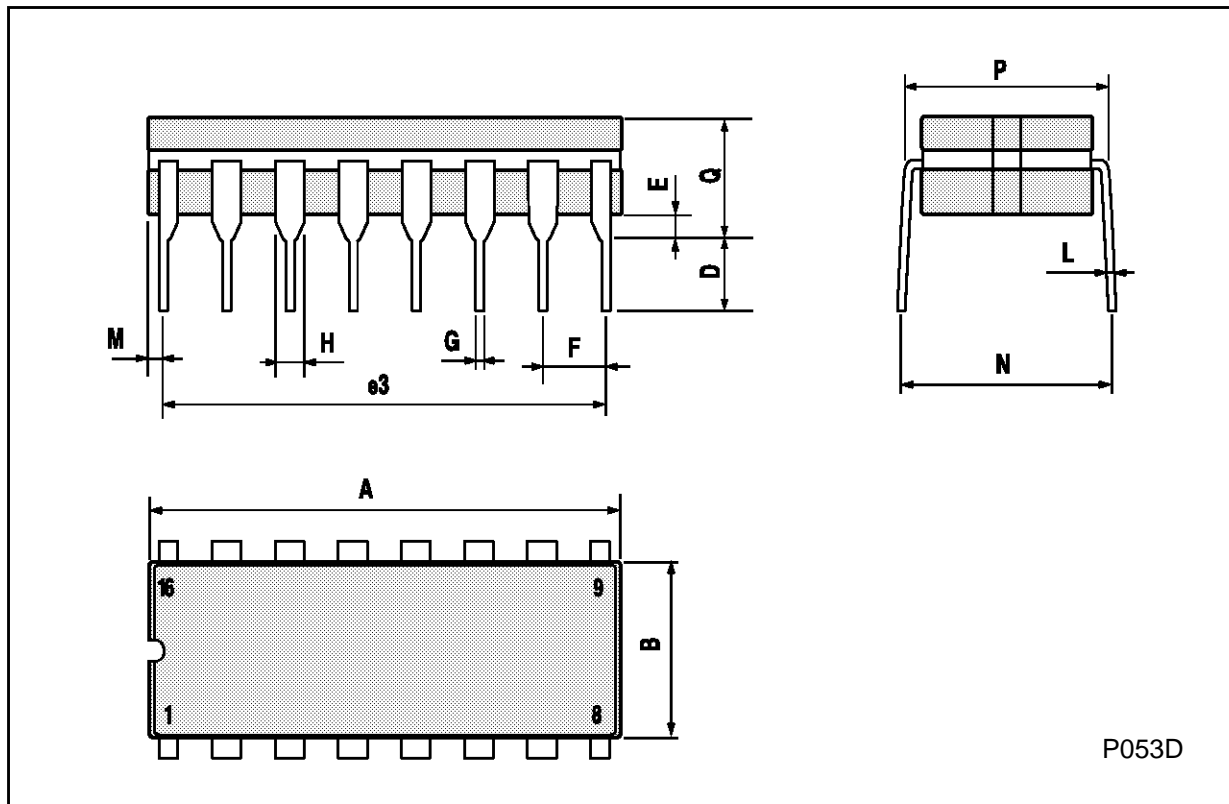
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

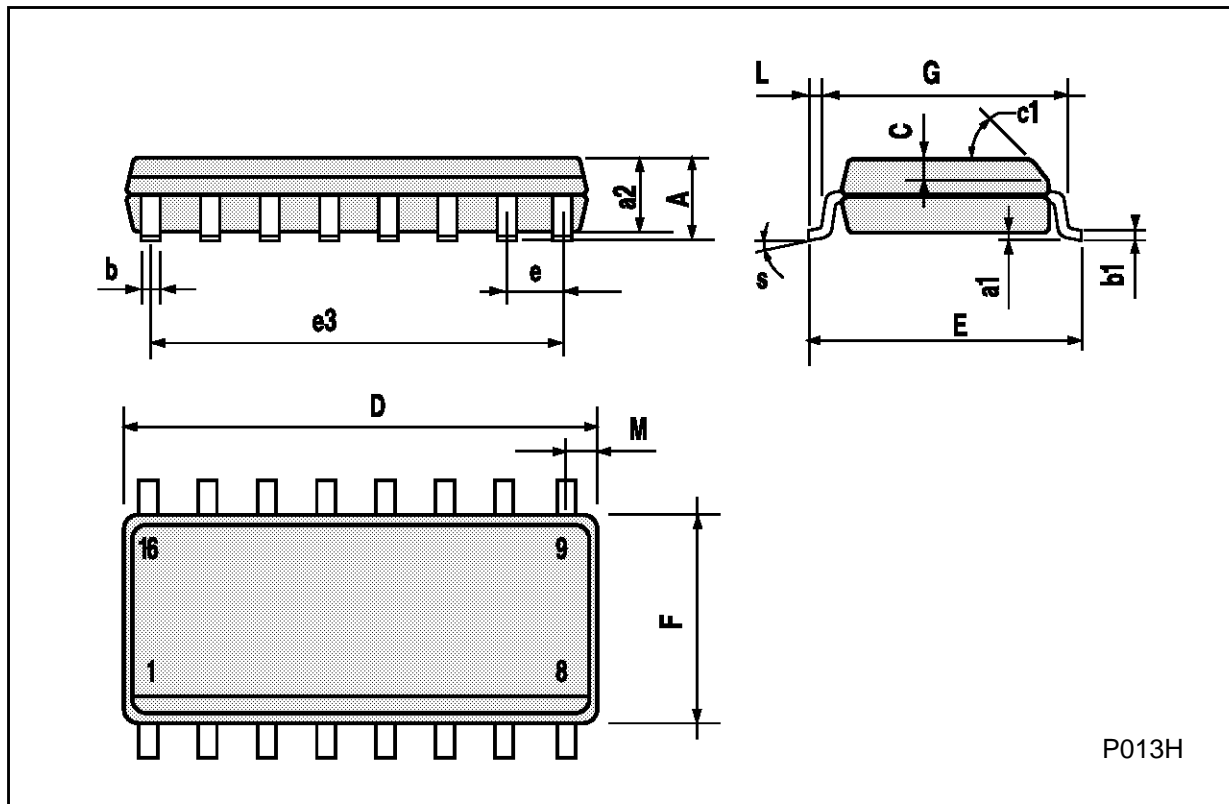
**Ceramic DIP16/1 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



**SO16 (Narrow) MECHANICAL DATA**

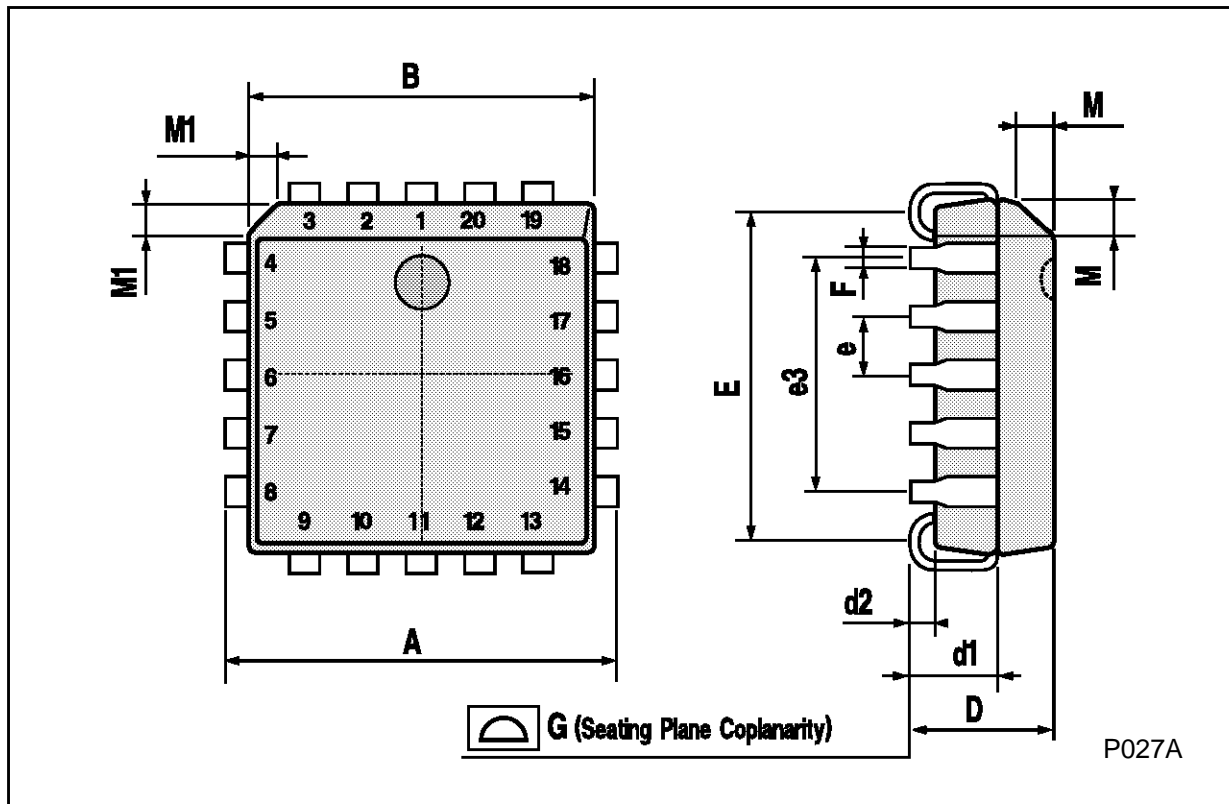
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

**PLCC20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



## HCC/HCF4035B

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