RHF484

## Rad-hard precision quad operational amplifier

Features

- High radiation immunity: 300 kRad TID at high dose rate
- ELDRS-free up to 100 krad
- 300 krad low dose rate on-going
- SEL immune at LET = 120 MeV.cm²/mg at 125°C
- SET characterized
- Hermetic package
- Rail-to-rail input/output
- 8 MHz gain bandwidth product
- Low input offset voltage: 60 µV typ
- Supply current: 2.2 mA typ per amplifier
- Operating from 4 to 14 V
- Input bias current: 6 nA typ
- QLM-V qualified under smd 5962-08222

Applications

- Space probes and satellites
- Harsh environment

Ceramic Flat-14W

Pin connections (top view)

Pin	Signal		Pin	Signal
1	OUT1		14	OUT4
2	-IN1		13	-IN4
3	+IN1		12	+IN4
4	+ VCC		11	- VCC
5	+IN2		10	+IN3
6	-IN2		9	-IN3
7	OUT2		8	OUT3

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Description

The RHF484 is a rail-to-rail precision bipolar quad operational amplifier featuring a low input offset voltage and a wide supply voltage.
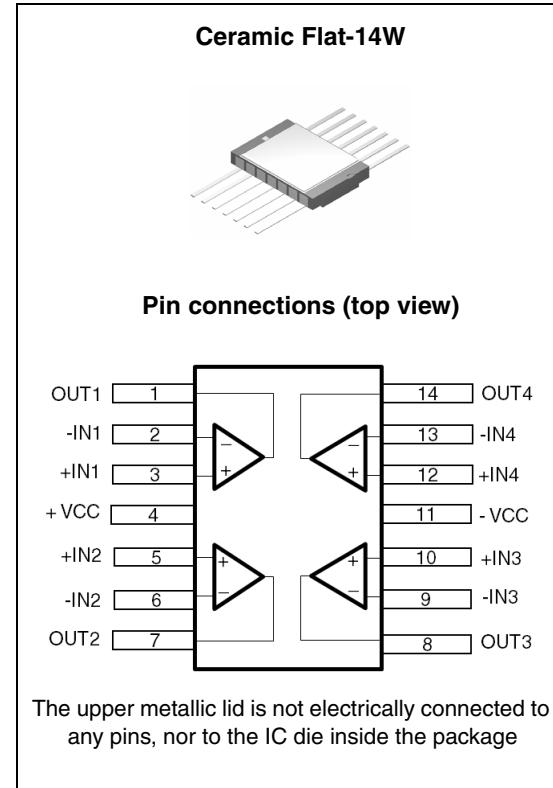
Designed to increase tolerance to radiation, the RHF484 is housed in a hermetic 14-pin flat package, making it an ideal product for space applications and harsh environments.

Table 1.   Device summary

Reference	SMD pin	Quality level	Temp range	Package	Lead finish	Mass	EPPL
RHF484K1		Engineering model	-55°C to +125°C	Flat-14 W	Gold	0.70 g	-
RHF484K-01V	5962F08222	Flight model					-

Note: Contact your ST sales office for information on specific conditions for products in die form.

1 Absolute maximum ratings and operating conditions

Table 2.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage $(+V_{CC})$-$(-V_{CC})$	18	V
V_{id}	Differential input voltage [1]	±1.2	V
V_{in}	Input voltage [2][3]	$-V_{CC}$ -0.3V to $+V_{CC}$ +0.3V	V
I_{in}	Input current	45	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient [4] Flat package, 14 pins	TBD	°C/W
R_{thjc}	Thermal resistance junction to case [4] Flat package, 14 pins	TBD	°C/W
ESD	HBM: human body model [5]	2	kV
T_{Lead}	Lead temperature (soldering, 10 sec)	260	°C
Radiation informations			
Dose	Low dose rate of 0.01 rad.sec^{-1}	100	kRad
	High dose rate of 50-300 rad.sec^{-1}	300	kRad
Heavy ions	SEL immunity (at 125°C)	120	MeV.cm^2/mg
	SET characterized		

1. The differential voltage is the voltage difference between the pins +IN and -IN of a channel.

2. All voltage values, except differential voltage are with respect to network ground terminal.

3. The voltage on either input must never exceed $+V_{CC}$ +0.3 V nor 16 V.

4. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.

5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 3.   Operating conditions

Symbol	Parameter	Value	Unit
$(+V_{CC})$-$(-V_{CC})$	Supply voltage	4 to 14 [1]	V
V_{icm}	Common-mode input voltage range	$-V_{CC}$ to $+V_{CC}$	V
T_{oper}	Operating free-air temperature range	-55 to +125	°C

1. SEL-free, up to 120 MeV.cm²/mg.

2   Electrical characteristics

Table 4. $+V_{CC} = 7$ V, $-V_{CC} = 7$ V, $V_{icm} = 0$ V, $T_{amb} = 25°C$, loads (R_L, C_L) connected to GND (unless otherwise specified)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Offset voltage	Vicm = +7 V	-55°C			700	µV
			+25°C			500	
			+125°C			700	
		Vicm = +0 V	-55°C			500	
			+25°C		60	300	
			+125°C			500	
		Vicm = -7 V	-55°C			700	
			+25°C			500	
			+125°C			700	
DV_{io}	Input offset voltage drift	No load			1		µV/°C
I_{ib}	Input bias current	No load	-55°C			100	nA
			+25°C		6	60	
			+125°C			100	
DI_{ib}	Input offset current temp. drift	No load			100		pA/°C
I_{io}	Input offset current	No load $V_{out} = 0$ V	-55°C			35	nA
			+25°C		2	15	
			+125°C			35	
C_{in}	Differential input capacitance between +IN and -IN		+25°C		8		pF
	Input capacitance between +IN (or -IN) and GND		+25°C		2		
I_{CC}	Supply current per amplifier	No load	-55°C			2.9	mA
			+25°C		2.2	2.9	
			+125°C			2.9	
CMR	Common mode rejection ratio	No load $-V_{CC} <$ Vicm $< +V_{CC}$	-55°C	72			dB
			+25°C	72	105		
			+125°C	72			
SVR	Supply rejection ratio	No load From $+V_{CC} = 2$ V and $-V_{CC} = -2$ V to $+V_{CC} = 7$ V and $-V_{CC} = -7$ V	-55°C	80			dB
			+25°C	90	120		
			+125°C	80			

Table 4. $+V_{CC}$ = 7 V, $-V_{CC}$ = 7 V, V_{icm} = 0 V, T_{amb} = 25°C, loads (R_L,C_L) connected to GND (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
AC performance							
GBP	Gain bandwidth product	Vout = 200 mVpp f = 100 kHz R_L= 1 kΩ C_L= 100 pF	-55°C	3.5			MHz
			+25°C	6	8		
			+125°C	3.5			
F_u	Unity gain frequency	R_L = 1 kΩ, C_L = 100 pF	+25°C		5		MHz
φm	Phase margin	R_L = 1 kΩ, C_L = 100 pF G = +5	+25°C		50		Degrees
A_{VD}	Large signal voltage gain	R_L = 10 kΩ V_{out} = -6.5 V to 6 V	-55°C	60			dB
			+25°C	74	85		
			+125°C	60			
SR	Slew rate	R_L = 1 kΩ Vout = -4.8 V to 4.8 V Vout = 4.8 V to -4.8 V	-55°C	1.7			V/µs
			+25°C	2	3.5		
			+125°C	1.7			
e_n	Equivalent input noise voltage	No load, f = 1kHz	+25°C		7		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent input noise current	No load, f = 1 kHz	+25°C		0.8		$\frac{pA}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion + noise	V_{out} = 13 Vpp, R_L = 1 kΩ, C_L = 100 pF G = -5.1	+25°C		0.01		%
Output characteristics							
V_{OH}	High level output voltage	$+V_{CC}$ =14 V, $-V_{CC}$ = 0 V R_L = 1 kΩ	-55°C	13.5			V
			+25°C	13.6	13.8		
			+125°C	13.5			
		$+V_{CC}$ =14 V, $-V_{CC}$ = 0 V R_L = 10 kΩ	-55°C	13.6			V
			+25°C	13.8	13.9		
			+125°C	13.6			
V_{OL}	Low level output voltage	$+V_{CC}$ =14 V, $-V_{CC}$ = 0 V R_L = 1 kΩ	-55°C			0.3	V
			+25°C		0.12	0.2	
			+125°C			0.3	
		$+V_{CC}$ =14 V, $-V_{CC}$ = 0 V R_L = 10 kΩ	-55°C			0.2	V
			+25°C		0.04	0.08	
			+125°C			0.2	

Table 4. $+V_{CC}$ = 7 V, $-V_{CC}$ = 7 V, V_{icm} = 0 V, T_{amb} = 25°C, loads (R_L,C_L) connected to GND (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
I_{out}[1]	Output sink current	V_{out} = $+V_{CC}$ No load, Vid = -1 V	-55°C	15			mA
			+25°C	20	35		
			+125°C	15			
	Output source current	V_{out} = $-V_{CC}$ No load, Vid = +1 V	-55°C	10			mA
			+25°C	15	30		
			+125°C	10			

1. These tests are performed during a very short period of time. Excessive heating can damage the device. In the application, the junction temperature must never exceed 150°C as specified in *Table 2*.

Table 5. $+V_{CC} = +2$ V, $-V_{CC} = -2$ V, $V_{icm} = 0$ V, $T_{amb} = 25°C$, loads (R_L,C_L) connected to GND (unless otherwise specified)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Offset voltage	Vicm = +2 V	-55°C			700	μV
			+25°C			500	
			+125°C			700	
		Vicm = +0 V	-55°C			500	
			+25°C		60	300	
			+125°C			500	
		Vicm = -2 V	-55°C			700	
			+25°C			500	
			+125°C			700	
DV_{io}	Input offset voltage drift	No load			1		μV/°C
I_{ib}	Input bias current	No load	-55°C			100	nA
			+25°C		11	60	
			+125°C			100	
DI_{ib}	Input offset current temp. drift	No load			100		pA/°C
I_{io}	Input offset current	No load $V_{out} = 0$ V	-55°C			35	nA
			+25°C		2	15	
			+125°C			35	
C_{in}	Differential input capacitance between +IN and -IN		+25°C		8		pF
	Input capacitance between +IN (or -IN) and GND		+25°C		2		
I_{CC}	Supply current per amplifier	No load	-55°C			2.6	mA
			+25°C		2	2.6	
			+125°C			2.6	
CMR	Common mode rejection ratio	No load $-V_{CC} < $ Vicm $ < +V_{CC}$	-55°C	72			dB
			+25°C	72	95		
			+125°C	72			

Table 5. $+V_{CC} = +2$ V, $-V_{CC} = -2$ V, $V_{icm} = 0$ V, $T_{amb} = 25°C$, loads (R_L,C_L) connected to GND (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
AC performance							
GBP	Gain bandwidth product	$V_{out} = 200$ mVpp $f = 100$ kHz $R_L = 1$ kΩ $C_L = 100$ pF	-55°C	3.5			MHz
			+25°C	6	8		
			+125°C	3.5			
F_u	Unity gain frequency	$R_L = 1$ kΩ, $C_L = 100$ pF	+25°C		5		MHz
φm	Phase margin	$R_L = 1$ kΩ, $C_L = 100$ pF $G = +5$	+25°C		50		Degrees
A_{VD}	Large signal voltage gain	$R_L = 10$ kΩ $V_{out} = -1.5$ V to 0.5 V	-55°C	60			dB
			+25°C	70	80		
			+125°C	60			
SR	Slew rate	$R_L = 1$ kΩ $V_{out} = -1.28$ V to 1.28 V $V_{out} = 1.28$ V to -1.28 V	-55°C	1.7			V/µs
			+25°C	2	3.1		
			+125°C	1.7			
e_n	Equivalent input noise voltage	No load, $f = 1$ kHz	+25°C		7.5		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent input noise current	No load, $f = 1$ kHz	+25°C		0.8		$\frac{pA}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion + noise	$V_{out} = 3$ Vpp, $R_L = 1$ kΩ, $C_L = 100$ pF $G = -5.1$	+25°C		0.01		%
Output characteristics							
V_{OH}	High level output voltage	$+V_{CC} = 4$ V, $-V_{CC} = 0$ V $R_L = 1$ kΩ	-55°C	3.75			V
			+25°C	3.8	3.9		
			+125°C	3.75			
		$+V_{CC} = 4$ V, $-V_{CC} = 0$ V $R_L = 10$ kΩ	-55°C	3.75			V
			+25°C	3.85	3.95		
			+125°C	3.75			
V_{OL}	Low level output voltage	$+V_{CC} = 4$ V, $-V_{CC} = 0$ V $R_L = 1$ kΩ	-55°C			0.2	V
			+25°C		0.05	0.1	
			+125°C			0.2	
		$+V_{CC} = 4$ V, $-V_{CC} = 0$ V $R_L = 10$ kΩ	-55°C			0.1	V
			+25°C		0.03	0.07	
			+125°C			0.1	

Table 5. $+V_{CC}$ = +2 V, $-V_{CC}$ = -2 V, V_{icm} = 0 V, T_{amb} = 25°C, loads (R_L,C_L) connected to GND (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
I_{out}[1]	Output sink current	V_{out} = $+V_{CC}$ No load Vid = -1 V	-55°C	15			mA
			+25°C	20	35		
			+125°C	15			
	Output source current	V_{out} = $-V_{CC}$ No load Vid = +1 V	-55°C	10			mA
			+25°C	15	30		
			+125°C	10			

1. These tests are performed during a very short period of time. Excessive heating can damage the device. In the application, the junction temperature must never exceed 150°C as specified in *Table 2*.

Figure 1.   Input offset voltage distribution
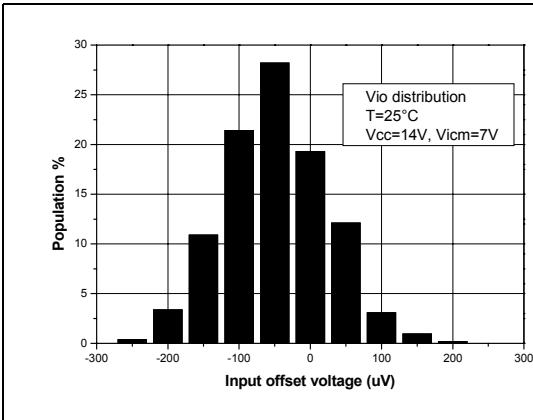
Figure 2.   Input bias current vs. supply voltage
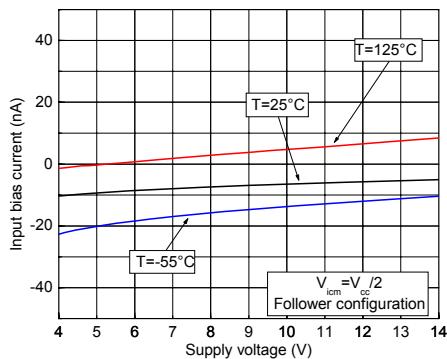
Figure 3.   Input bias current vs. Vicm at V_{CC} = 4 V
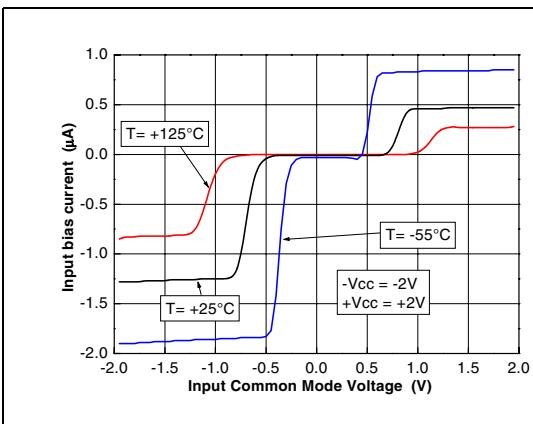
Figure 4.   Input bias current vs. Vicm at V_{CC} = 14 V
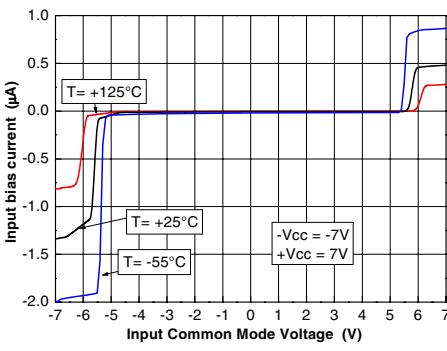
Figure 5.   Supply current vs. Vicm in follower configuration at V_{CC} = 4 V
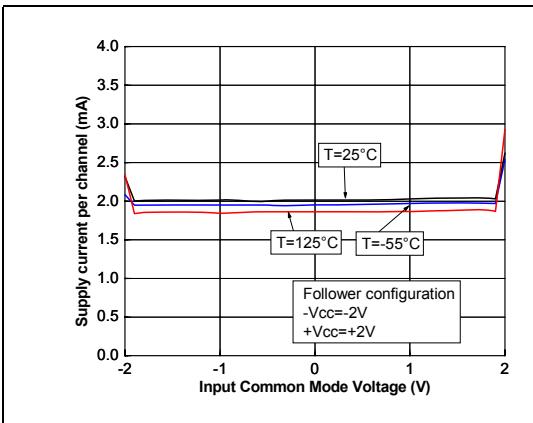
Figure 6.   Supply current vs. Vicm in follower configuration at V_{CC} = 14 V
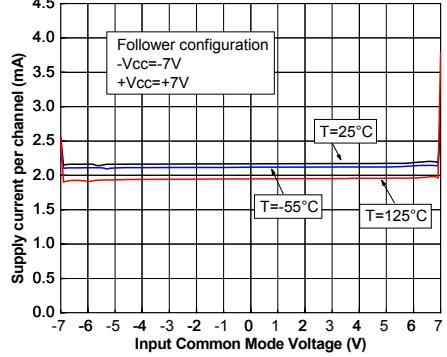
Figure 7. Supply current vs. supply voltage at V$_{icm}$ = V$_{CC}$/2
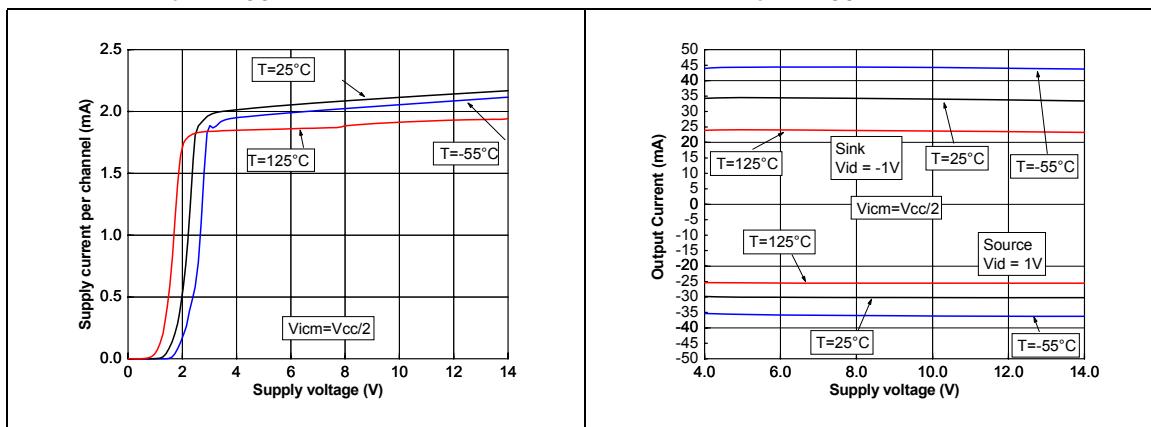
Figure 8. Output current vs. supply voltage at V$_{icm}$ = V$_{CC}$/2
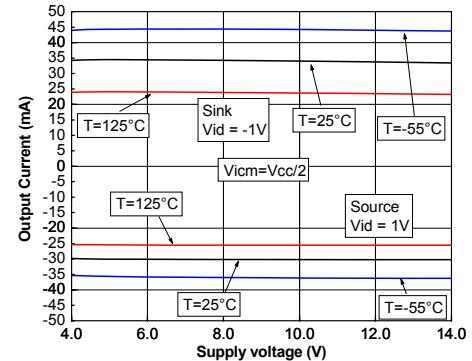
Figure 9. Output current vs. output voltage at V$_{CC}$ = 4 V
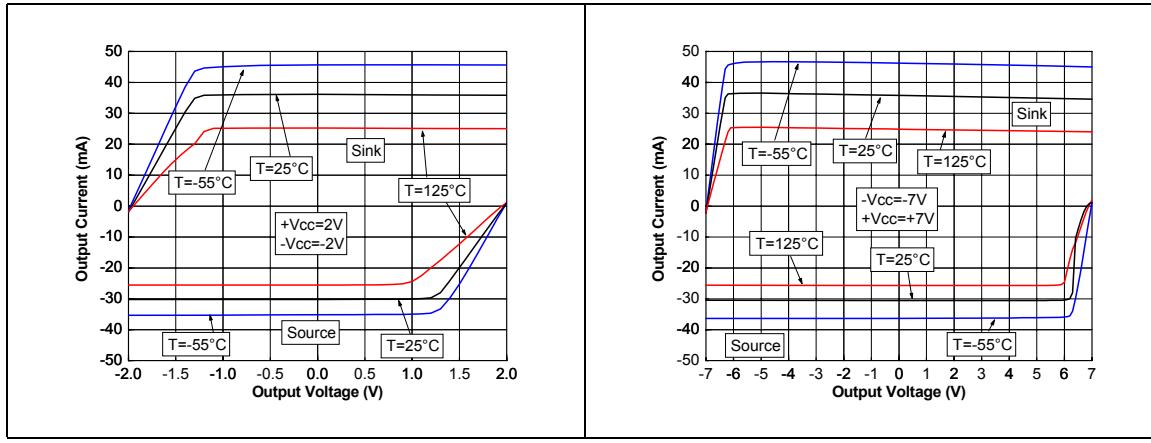
Figure 10. Output current vs. output voltage at V$_{CC}$ = 14 V
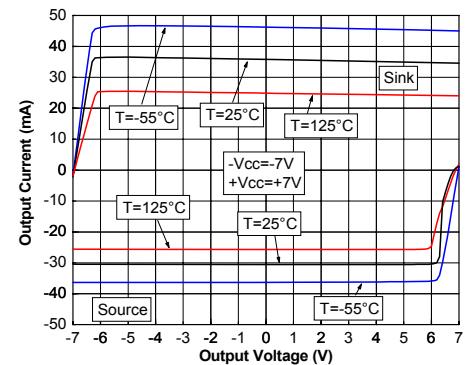
Figure 11. Differential input voltage vs. output voltage at V$_{CC}$ = 4 V
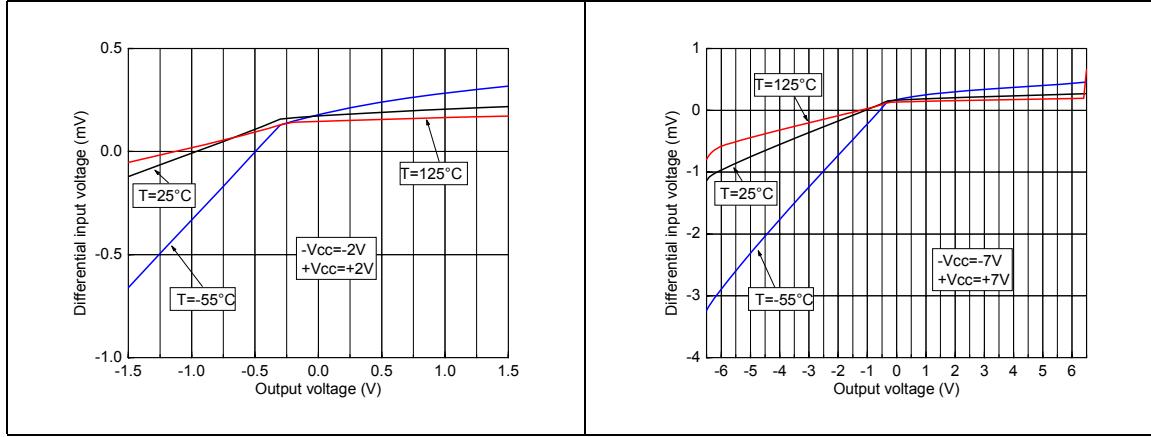
**Figure 12. Differential input voltage vs. output voltage at V$_{CC}$ = 14 V**
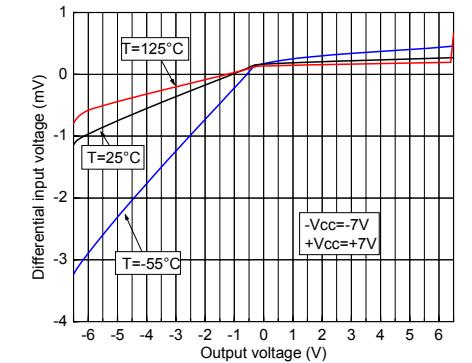
Figure 13.   Noise vs. frequency at V$_{CC}$= 4 V and
V$_{CC}$ = 14 V
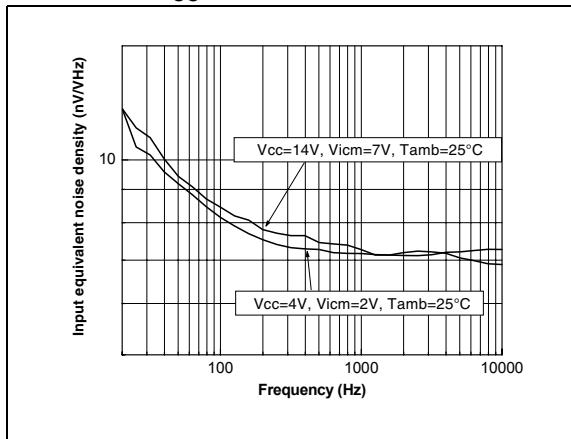
Figure 14.   Voltage gain and phase vs.
frequency at V$_{CC}$ = 4 V, Vicm = 2 V
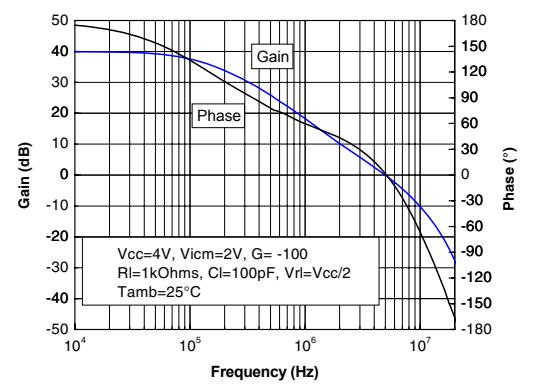
Figure 15.   Voltage gain and phase vs.
frequency at V$_{CC}$ = 4 V, Vicm = 3.5 V
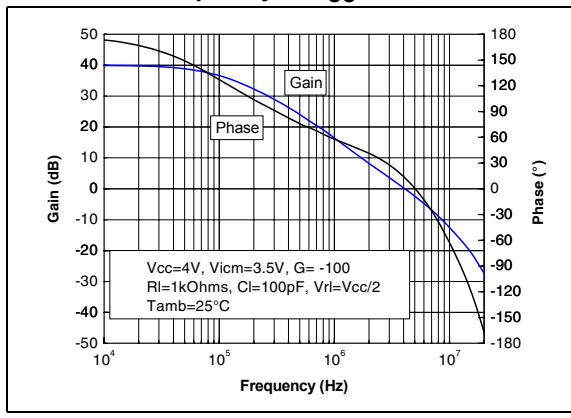
Figure 16.   Voltage gain and phase vs.
frequency at V$_{CC}$ = 4 V, Vicm = 0.5 V
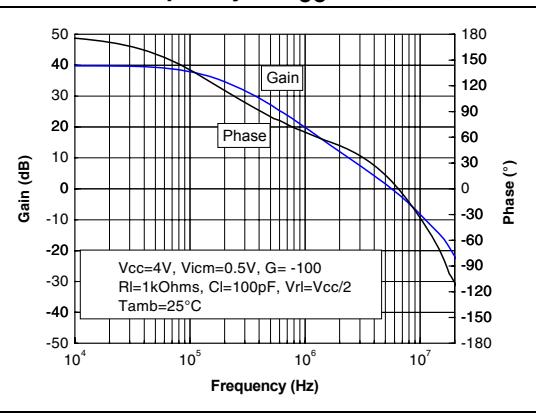
Figure 17.   Voltage gain and phase vs.
frequency at V$_{CC}$ = 14 V, Vicm = 7 V
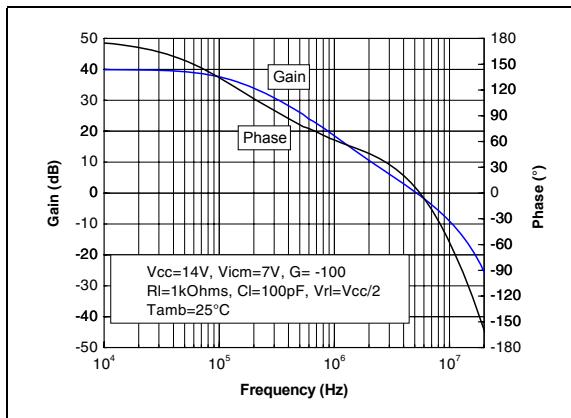
Figure 18.   Voltage gain and phase vs.
frequency at V$_{CC}$ = 14 V,
Vicm = 13.5 V
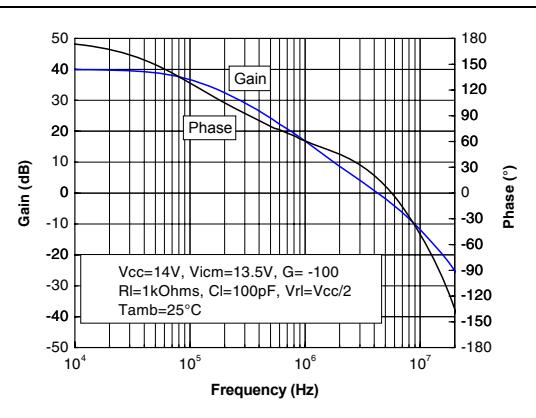
**Figure 19. Voltage gain and phase vs. frequency at V$_{CC}$ = 14 V, Vicm = 0.5 V**
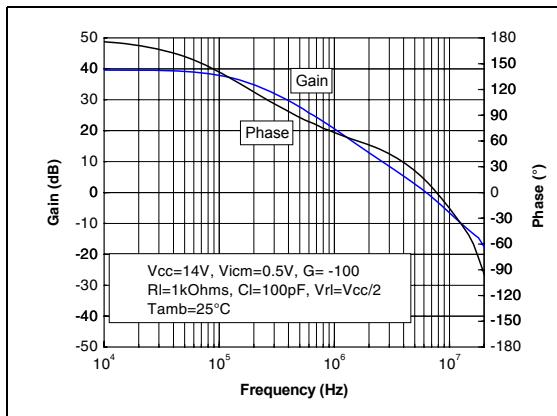

Figure 20. Positive slew rate at V$_{CC}$ = 4 V
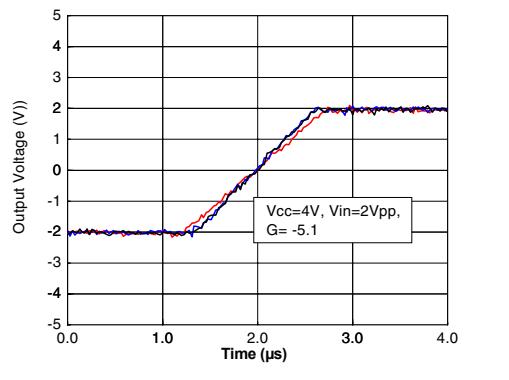

Figure 21. Negative slew rate at V$_{CC}$ = 4 V
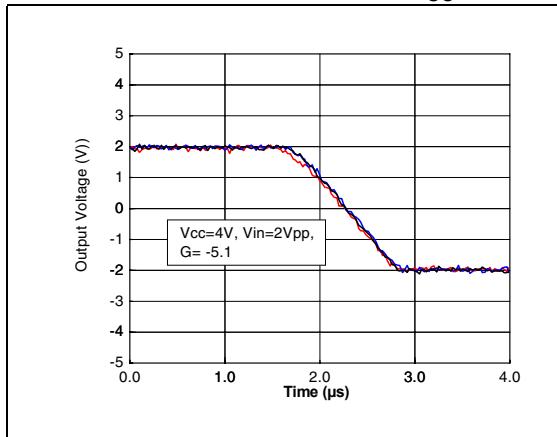


Figure 22. Positive slew rate at V$_{CC}$ = 14 V
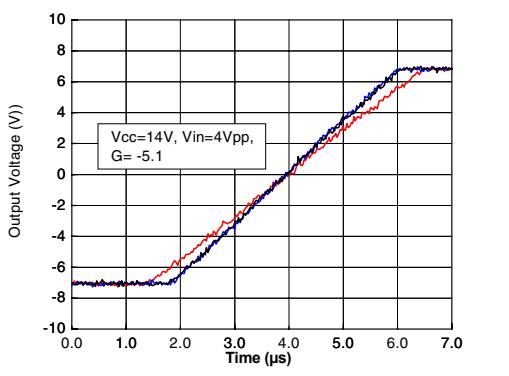
Figure 23. Negative slew rate at V$_{CC}$ = 14 V
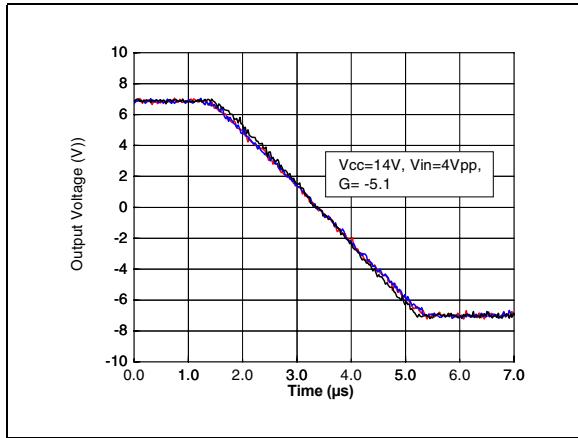
3 Achieving good stability at low gain

At low frequencies, the RHF484 can be used in a low gain configuration as shown in *Figure 24*. At lower frequencies, the stability is not affected by the value of the gain, which can be set close to 1 V/V (0 dB), and is reduced to its simplest expression G1=1+Rfb/Rg. Therefore, an R-C cell is added in the gain network so that the gain is increased (up to 5) at higher frequencies (where the stability of the amplifier could be affected). At higher frequencies, the gain becomes G2=1+Rfb/(Rg//R).

Figure 24. Low gain configuration
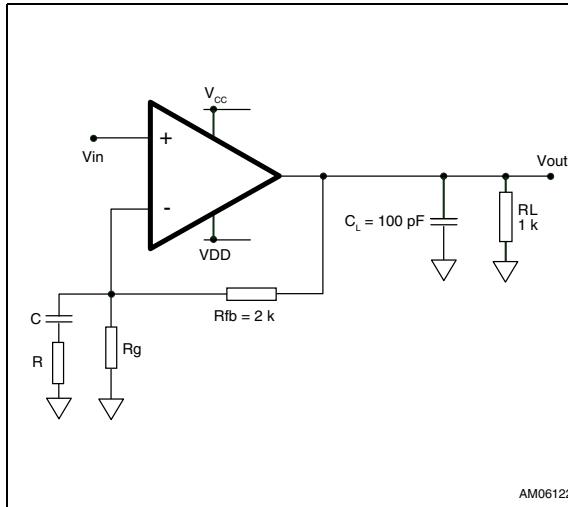
Figure 25. Closed-loop gain
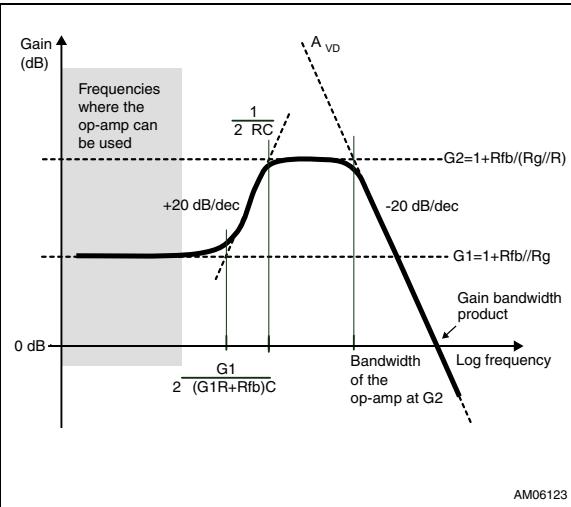
Rg becomes a complex impedance. The closed-loop gain features a variation in frequency and can be expressed as:

$$\text{Gain} = G1 \frac{1 + jC\omega \times \left(\dfrac{G1R + Rfb}{G1}\right)}{1 + jCR\omega}$$

where a pole appears at $1/2\pi RC$ and a zero at $G1/2\pi(G1R+Rfb)C$. The frequency can be plotted as shown in *Figure 25*.

Table 6. External components versus low-frequency gain

G1 (V/V)	R (Ω)	C (nF)	Rg (Ω)	Rfb (Ω)
1.1	510	1	20k	2k
2	510	1	2k	2k
3	510	1	1k	2k
4	510	1	750	2.4k
5	Not connected	Not connected	820	3.3k

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 26. Wide ceramic Flat-14 package mechanical drawing.
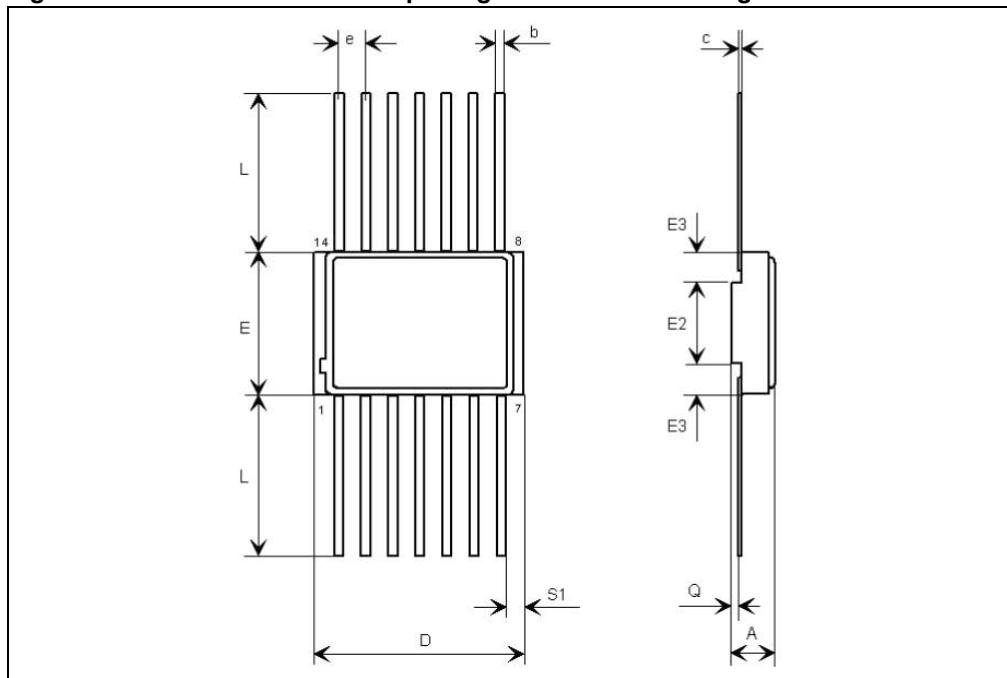
Note: *The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or Vcc will not affect the electrical characteristics.*

Table 7. Wide ceramic Flat-14 W package mechanical data

Ref.	Dimensions					
	Millimeters			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.93	2.11	2.29	.076	.083	.090
b	0.38	0.43	0.48	.015	.017	.019
c	0.10	0.13	0.18	.004	.005	.007
D	9.71	9.91	10.11	.382	0.390	.398
E	7.27	7.42	7.57	.286	.292	.298
E2		5.4			.213	
E3	0.76			.030		
e		1.27			.050	
L	6.3		6.6	.248		.260
Q	0.20		0.28	.008		.011
S1	0.13			.005		

5 Ordering information

Table 8. Order codes

Order code	Description	Temperature range	Package	Marking
RHF484K1	Engineering Samples	-55°C to +125°C	Flat-14 W	RHF484K1
RHF484K-01V	Flight Models			5962F0822201VXC

Note: *Contact your ST sales office for information on specific conditions for products in die form.*

6 Revision history

Table 9.   Document revision history

Date	Revision	Changes
26-Apr-2011	1	Initial release.

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