National Semiconductor

August 1998

54FCT573
Octal D-Type Latch with TRI-STATE® Outputs

General Description

The 'FCT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'FCT373 but has different pinouts.

Features

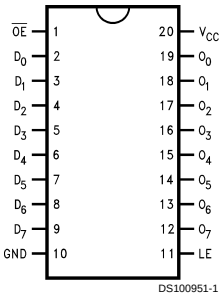
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- TTL input and output level compatible
- CMOS power consumption
- Functionally identical to 'FCT373
- TRI-STATE outputs for bus interfacing
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-8863901

Ordering Code

Military	Package Number	Package Description
54FCT573DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT573FMQB	W20A	20-Lead Cerpack
54FCT573LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

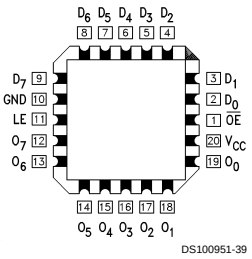
Connection Diagram

Pin Assignment for DIP and Cerpack



DS100951-1

Pin Assignment for LCC



DS100951-39

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Functional Description

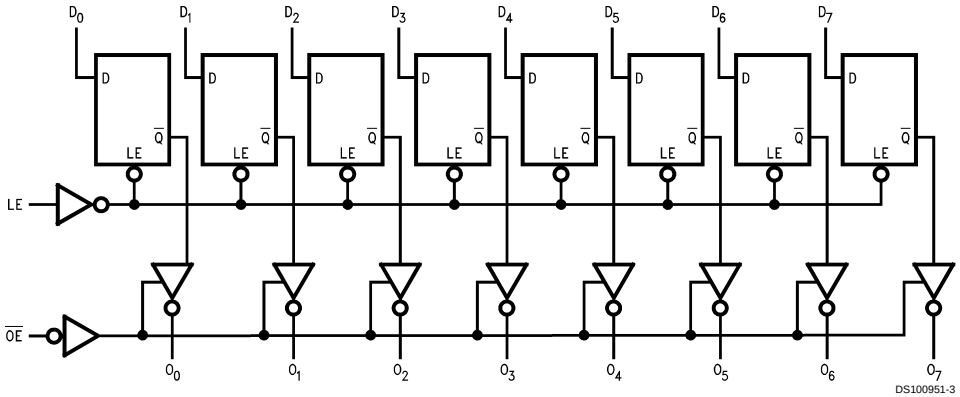
The 'FCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



DS100951-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		FCT573 Min	FCT573 Typ	FCT573 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54FCT	4.3			V	Min	I_{OH} = −300 µA
		54FCT	2.4					I_{OH} = −12 mA
V_{OL}	Output LOW Voltage	54FCT			0.2	V	Min	I_{OL} = 300 µA
		54FCT			0.5			I_{OL} = 32 mA
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.0V
I_{OZH}	Output Leakage Current				50	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current				-60	mA	Max	V_{OUT} = 0.0V
I_{CCQ}	Quiescent Power Supply Current				1.5	mA	Max	V_{IN} < 0.2V or V_{IN} 5.3V, V_{CC} = 5.5V
ΔI_{CC}	Quiescent Power Supply Current				2.0	mA	Max	V_I = 3.4V, V_{CC} = 5.5V
I_{CCD}	Dynamic I_{CC}				0.4	mA/ MHz	Max	Outputs Open, V_{CC} = 5.5V, V_{IN} 5.3V or V_{IN} < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V_{CC}
I_{CC}	Total Power Supply Current				6.0	mA	Max	Outputs Open, f_{CP} = 10 MHz, V_{CC} = 5.5V, V_{IN} 5.3V or V_{IN} < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V_{CC}

AC Electrical Characteristics

Symbol	Parameter	54FCT $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
t_{PLH}	Propagation Delay	1.0	8.5	ns	*Figure 4*
t_{PHL}	D_n to O_n	1.0	8.5		
t_{PLH}	Propagation Delay	1.0	15.0	ns	*Figure 4*
t_{PHL}	LE to O_n	1.0	15.0		
t_{PZH}	Output Enable Time	1.0	13.5	ns	*Figure 6*
t_{PZL}		1.0	13.5		
t_{PHZ}	Output Disable Time	1.0	10.0	ns	*Figure 6*
t_{PLZ}	Time	1.0	10.0		

AC Operating Requirements

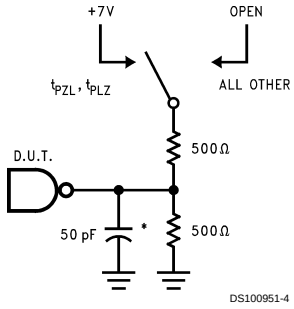
Symbol	Parameter	54FCT $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
$t_s(H)$	Set Time, HIGH	2.0		ns	*Figure 7*
$t_s(L)$	or LOW D_n to LE	2.0			
$t_h(H)$	Hold Time, HIGH	1.5		ns	*Figure 7*
$t_h(L)$	or LOW D_n to LE	1.5			
$t_w(H)$	Pulse Width,	6.0		ns	*Figure 5*
	LE HIGH				

Capacitance

Symbol	Parameter	Max	Units	Conditions ($T_A = 25^\circ C$)
C_{IN}	Input Capacitance	10	pF	$V_{CC} = 0V$
C_{OUT} (Note 3)	Output Capacitance	12	pF	$V_{CC} = 5.0V$

Note 3: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Test Load

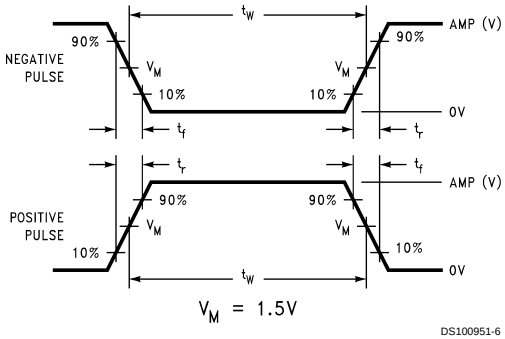


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

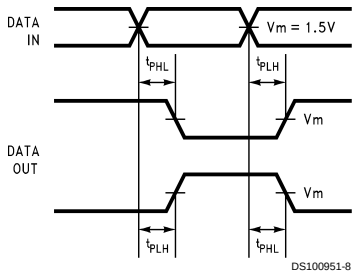


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

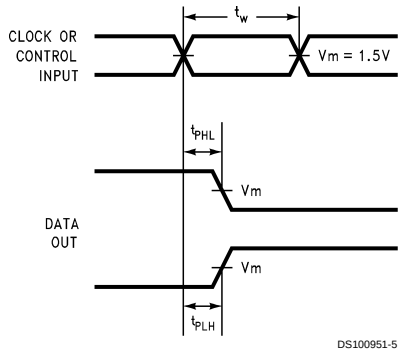


FIGURE 5. Propagation Delay, Pulse Width Waveforms

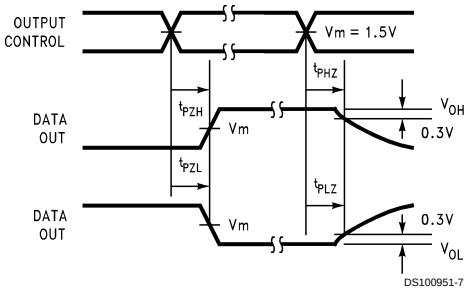


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

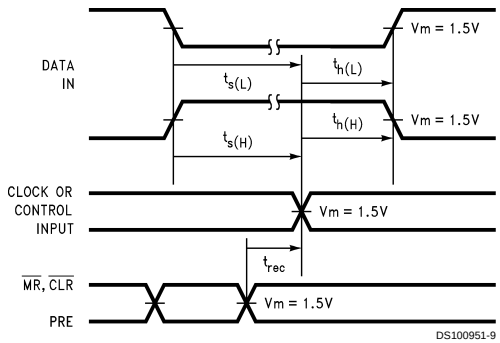
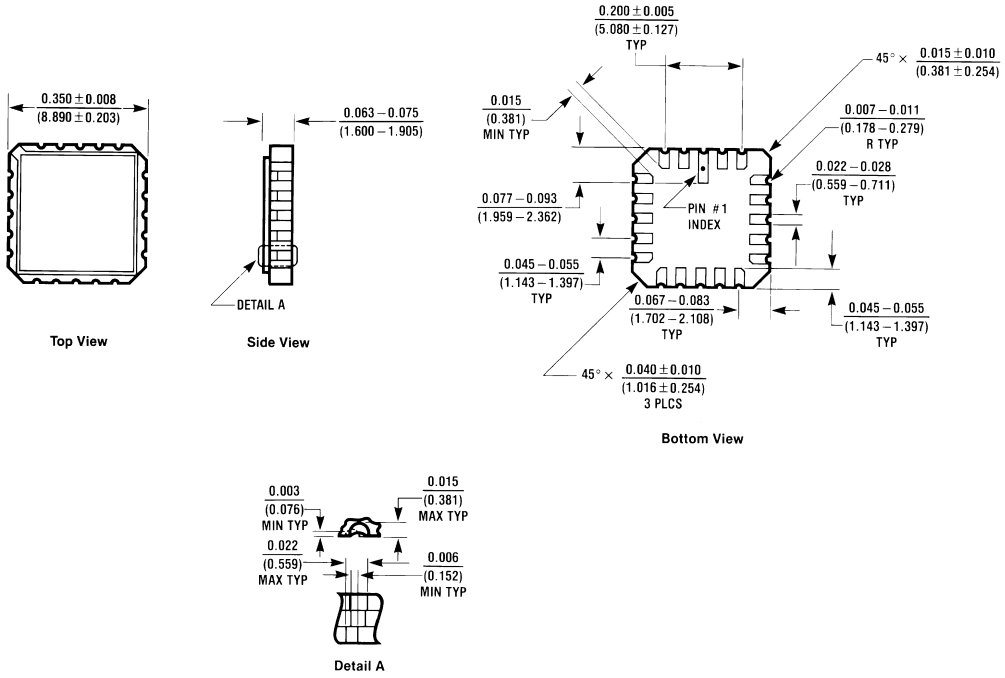
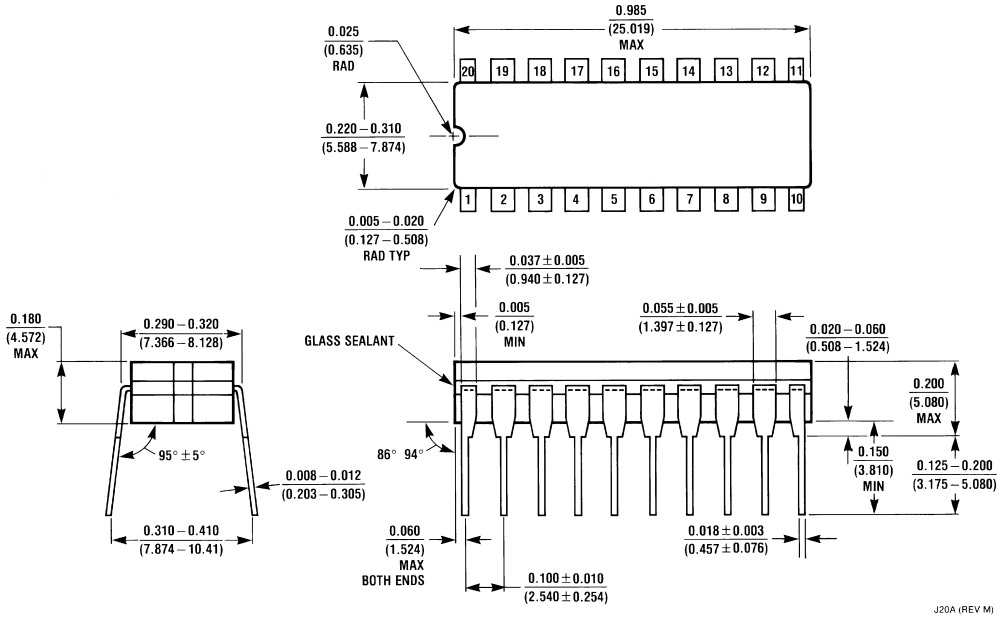


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

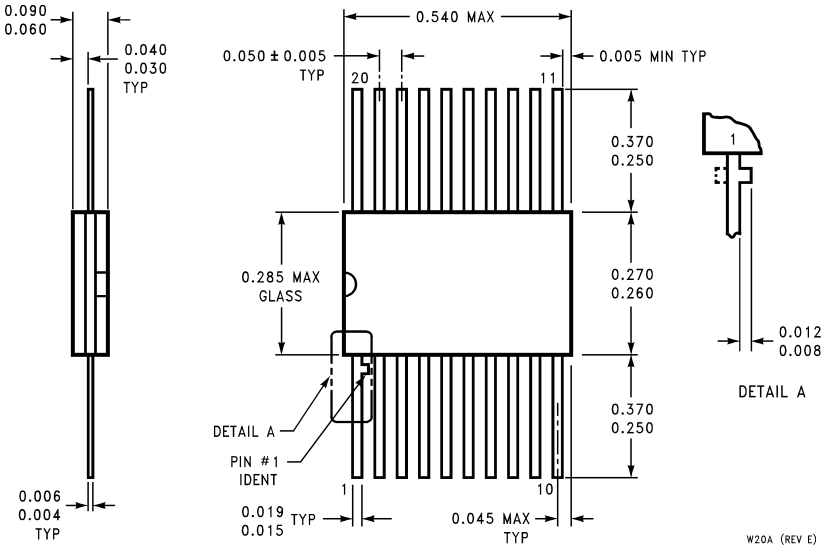


20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



20-Lead Ceramic Dual-In-Line
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpack
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507