RHF1201

Rad-hard 12-bit 0.5 to 50 Msps A/D converter

Features

- Wide sampling range: 0.5Msps to 50Msps
- Optimwatt™ adaptive power: 44mW @ 0.5Msps, 100mW @ 50Msps
- Input range: 2 V_{pp} differential
- SFDR up to 75dB @ F_S = 50Msps, F_{in} = 15MHz
- 2.5V / 3.3V compatible digital I/O
- Built-in reference voltage with external bias capability
- Hermetic package
- Rad-hard: 300 kRad(Si) TID
- Failure immune (SEFI) and latchup immune (SEL) up to 120 MeV-cm^2/mg at 2.7V and 125°C
- Qml-V qualified, smd 5962-05217

Applications

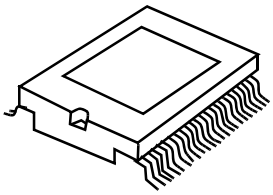
- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics

Description

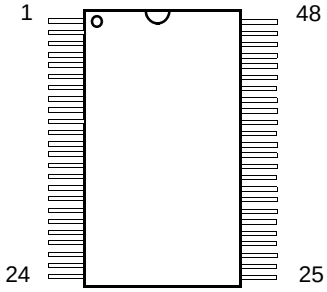
The RHF1201 is a 12-bit 50MHz maximum sampling frequency analog to digital converter using pure (ELDRS-free) CMOS 0.25µm technology combining high performance, radiation robustness and very low power consumption.

The RHF1201 is based on a pipeline structure and digital error correction to provide excellent static linearity and achieve 10.3 effective bits at F_S = 50Msps, and F_{in} = 15MHz.

SO-48 package



Pin connections (top view)



Specifically designed for optimizing power consumption, the RHF1201 can dissipate as little as 100mW at 50Msps, while maintaining a high level of performance.

It integrates a proprietary track-and-hold structure to ensure IF-sampling applications up to 150 MHz.

A voltage reference is integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs to allow common bus sharing. Output data can be coded in two different formats.

A Data Ready signal which is raised when the data is valid on the output can be used for synchronization purposes.

The RHF1201 is available in -55° C to +125° C temperature range, in a small 48-pin hermetic SO-48 package.

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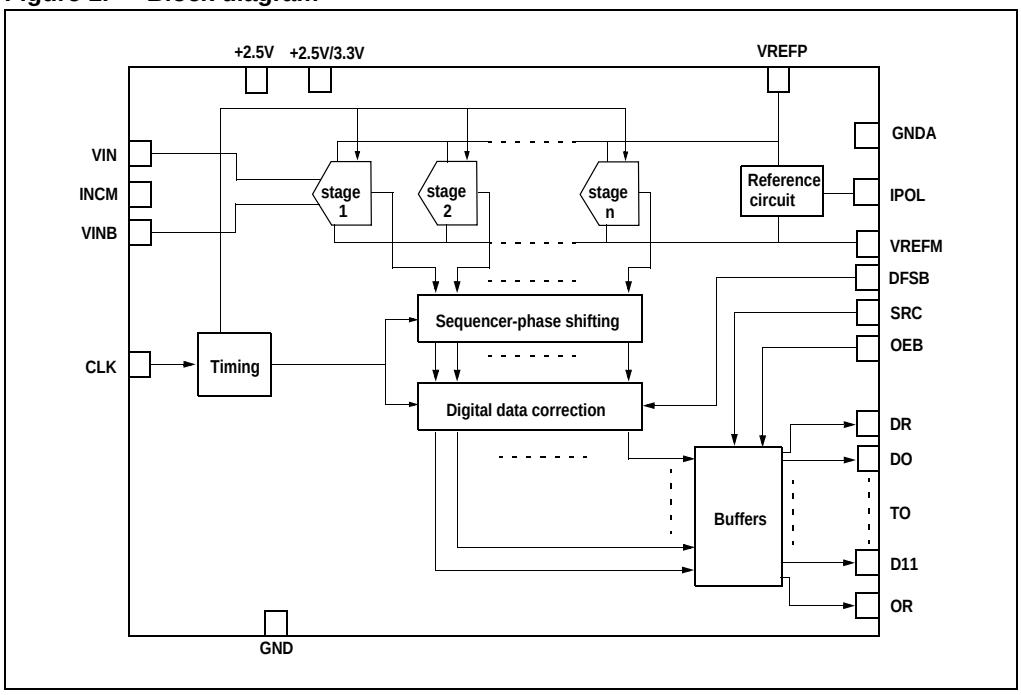
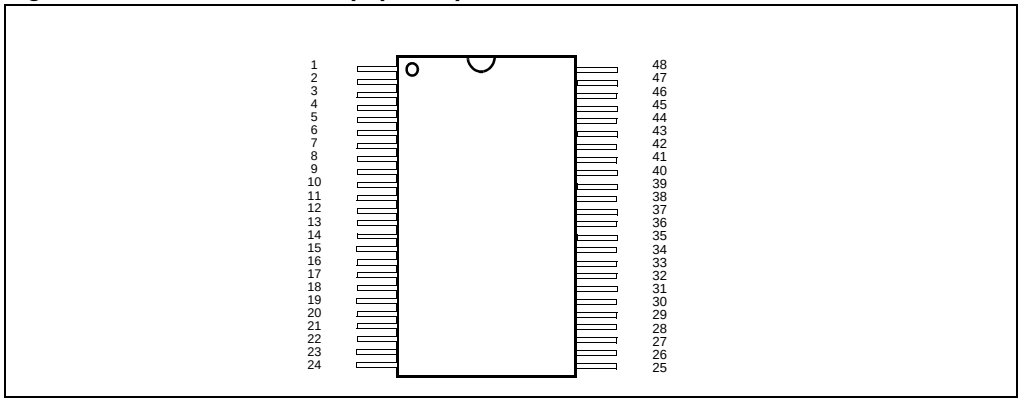
1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections (top view)



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3 Pin descriptions

Table 1. Pin descriptions

Pin	Name	Description	Observation	Pin	Name	Description	Observation
1	GNDBI	Digital buffer ground	0 V	25	SRC	Slew rate control input	2.5 V/3.3 V CMOS input
2	GNDBE	Digital buffer ground	0 V	26	OEB	Output Enable input	2.5 V/3.3 V CMOS input
3	VCCBE	Digital buffer power supply	2.5 V/3.3 V	27	DFSB	Data Format Select input	2.5 V/3.3 V CMOS input
4		NC	Non connected	28	AVCC	Analog power supply	2.5 V
5		NC	Non connected	29	AVCC	Analog power supply	2.5 V
6	OR	Out Of Range output	CMOS output (2.5 V/3.3 V)	30	AGND	Analog ground	0 V
7	D11(MSB)	Most Significant Bit output	CMOS output (2.5 V/3.3 V)	31	IPOL	Analog bias current input	
8	D10	Digital output	CMOS output (2.5 V/3.3 V)	32	VREFP	Top voltage reference	1 V
9	D9	Digital output	CMOS output (2.5 V/3.3 V)	33	VREFM	Bottom voltage reference	0 V
10	D8	Digital output	CMOS output (2.5 V/3.3 V)	34	AGND	Analog ground	0 V
11	D7	Digital output	CMOS output (2.5 V/3.3 V)	35	VIN	Analog input	1 V_{pp}
12	D6	Digital output	CMOS output (2.5 V/3.3 V)	36	AGND	Analog ground	0 V
13	D5	Digital output	CMOS output (2.5 V/3.3 V)	37	VINB	Inverted analog input	1 V_{pp}
14	D4	Digital output	CMOS output (2.5 V/3.3 V)	38	AGND	Analog ground	0 V
15	D3	Digital output	CMOS output (2.5 V/3.3 V)	39	INCM	Input common mode	0.5 V
16	D2	Digital output	CMOS output (2.5 V/3.3 V)	40	AGND	Analog ground	0 V
17	D1	Digital output	CMOS output (2.5 V/3.3 V)	41	AVCC	Analog power supply	2.5 V
18	D0(LSB)	Least Significant Bit output	CMOS output (2.5 V/3.3 V)	42	AVCC	Analog power supply	2.5 V
19	DR	Data Ready output	CMOS output (2.5 V/3.3 V)	43	DV_{CC}	Digital power supply	2.5 V
20		NC	Non connected	44	DV_{CC}	Digital power supply	2.5 V
21		NC	Non connected	45	DGND	Digital ground	0 V
22	VCCBE	Digital Buffer power supply	2.5 V/3.3 V	46	CLK	Clock input	2.5 V compatible CMOS input
23	GNDBE	Digital Buffer ground	0 V	47	DGND	Digital ground	0 V
24	VCCBI	Digital Buffer power supply	2.5 V	48	DGND	Digital ground	0 V

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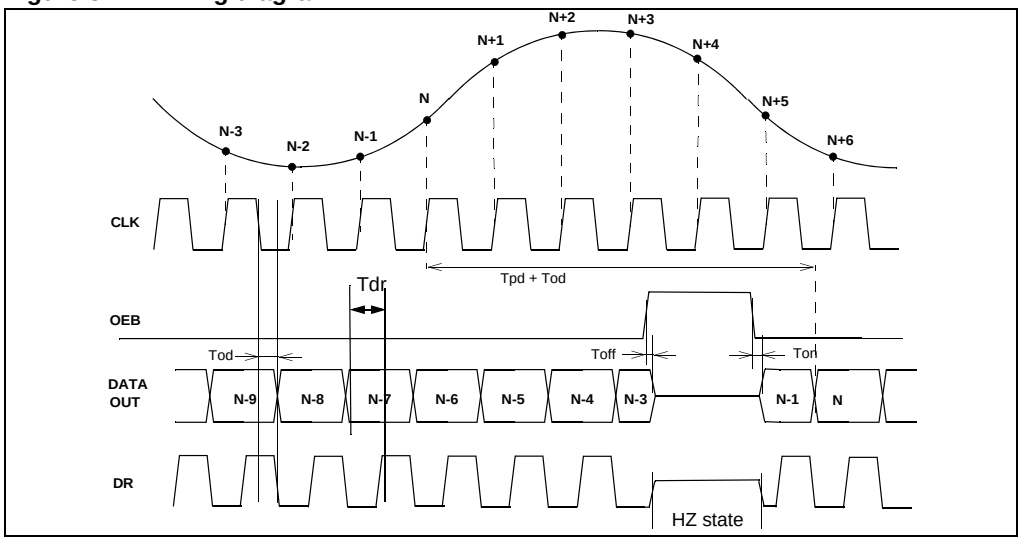
4 Timing characteristics

Table 2. Timing table

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_S	Sampling frequency		0.5		50	MHz
T_{ck}	Sampling clock cycle		20		2000	ns
DC	Clock duty cycle	F_S = 45 Msps	45	50	65	%
T_{C1}	Clock pulse width (high)		10		1800	ns
T_{C2}	Clock pulse width (low)		8		1800	ns
T_{od}	Data output delay (fall of clock to data valid)	10 pF load capacitance	4	5	6	ns
T_{pd}	Data pipeline delay		5.5	5.5	5.5	cycles
T_{dr}	Data ready delay after data change			0.5		cycles
T_{on}	Falling edge of OEB to digital output valid data			1	3	ns
T_{off}	Rising edge of OEB to digital output tri-state			1	3	ns
T_{rD}	Data rising time	SRC = 0 5 pF load capacitance		2.8		ns
		SRC = 1 5pF load capacitance		5.7		ns
T_{fD}	Data falling time	SRC = 0 5pF load capacitance		2		ns
		SRC = 1 5pF load capacitance		4.3		ns

Figure 3. Timing diagram



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5 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage(1)	0 to 3.3	V
DV_{CC}	Digital supply voltage(1)	0 to 3.3	V
V_{CCBI}	Digital buffer supply voltage(1)	0 to 3.3	V
V_{CCBE}	Digital buffer supply voltage(1)	0 to 3.6	V
I_{Dout}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thjc}	Junction - case thermal resistance	22	°C/W
ESD	Electrostatic discharge - HBM	2	kV

1. All voltage values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must never exceed -0.3 V or V_{CC} +0.3 V.

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AV_{CC}	Analog supply voltage		2.3	2.5	2.7	V
DV_{CC}	Digital supply voltage		2.3	2.5	2.7	V
V_{CCBI}	Digital internal buffer supply		2.3	2.5	2.7	V
V_{CCBE}	Digital output buffer supply		2.3	2.5	3.4	V
V_{REFP}	Forced top voltage reference		0.5	1	AV_{CC}	V
V_{REFM}	Bottom internal reference voltage		0	0	0.5	V

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6 Electrical characteristics (unchanged after 300kRad)

Test conditions, unless otherwise specified are: AV_{CC} = DV_{CC} = V_{CCB} = 2.5 V, F_S = 50 Msps, F_{in} = 2 MHz, V_{IN} @ -1 dBSF, V_{REFP} = Internal, V_{REFM} = 0 V, T_{amb} = 25° C

Table 5. Analog inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}-V_{INB}	Full scale reference voltage			2.0		V_{pp}
C_{in}	Input capacitance			7.0		pF
R_{in}	Input resistance					
ERB	Effective resolution bandwidth(1)			95		MHz

1. See *Section 8: Definitions of specified parameters on page 14* for more information.

Table 6. Reference voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{REFP}	Top internal reference voltage	AV_{CC} from 2.3V to 2.7V T_{min} = -55° C to T_{max} = 125° C(1)	0.82	0.95	1.16	V
V_{INCM}	Input common mode voltage	AV_{CC}=2.3 V to AV_{CC}=2.7 V T_{min} = -55° C to T_{max} = 125° C(1)	0.43	052	0.67	V
TempCo	Temperature coefficients	V_{REFP} T_{min} = -55° C to T_{max} = 125° C(1)		0.12		mV/°C
		V_{INCM} T_{min} = -55° C to T_{max} = 125° C(1)		0.12		mV/°C

1. Not fully tested over the temperature range. Guaranteed by sampling.

Table 7. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock input						
V_{IL}	Logic "0" voltage			0	0.8	V
V_{IH}	Logic "1" voltage		2.0	2.5		V
Digital inputs						
V_{IL}	Logic "0" voltage			0	0.25 V_{CCBE}	V
V_{IH}	Logic "1" voltage		0.75 V_{CCBE}	V_{CCBE}		V

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Table 7. Digital inputs and outputs (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Digital outputs						
V_{OL}	Logic "0" voltage	I_{OL} = -1mA		0	0.2	V
V_{OH}	Logic "1" voltage	I_{OH} = 1mA	V_{CCBE} - 0.2			V
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-15		15	µA
C_L	Output load capacitance				15	pF

Table 8. Accuracy

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OE	Offset error	F_{in} = 2 MHz, V_{IN} @ +1 dBFS		±0.3		%
DNL	Differential non linearity(1)	F_{in} = 2 MHz, V_{IN} @ +1 dBFS		±0.5		LSB
INL	Integral non linearity(1)	F_{in} = 2 MHz, V_{IN} @ +1 dBFS		±1.7		LSB
-	Monotonicity and no missing codes		Guaranteed			

1. See *Section 8: Definitions of specified parameters on page 14* for more information.

Table 9. Dynamic characteristics

Symbol	Parameter(1)	Test conditions(2)	Min	Typ	Max	Unit
SFDR	Spurious free dynamic range	F_{in} = 15 MHz		-75	-63	dBc
		F_{in} = 95 MHz		-70		
		F_{in} = 145 MHz		-57		dBc
SNR	Signal to noise ratio	F_{in} = 15 MHz	59	63		dB
		F_{in} = 95 MHz		60		dB
		F_{in} = 145 MHz		59		
THD	Total harmonics distortion	F_{in} = 15 MHz		-76	-64	dB
		F_{in} = 95 MHz		-72		dB
		F_{in} = 145 MHz		-58		
SINAD	Signal to noise and distortion ratio	F_{in} = 15 MHz	59	63		dB
		F_{in} = 95 MHz		60		
		F_{in} = 145 MHz		56.5		dB
ENOB	Effective number of bits	F_{in} = 15 MHz	9.7	10.3		bits
		F_{in} = 95 MHz		9.5		bits
		F_{in} = 145 MHz		9.1		

1. See *Section 8: Definitions of specified parameters on page 14* for more information.
2. V_{REFP} = 1 V with external supply.

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7 Application information

The RHF1201 is a high speed analog to digital converter based on a pipeline architecture and a 0.25 µm CMOS process to achieve the best performance in terms of linearity and power consumption.

The pipeline structure consists of 11 internal conversion stages in which the analog signal is fed and sequentially converted into digital data. Signal input is sampled on the rising edge of the clock.

The first 10 stages of the conversion include at each stage, an analog to digital converter, a digital to analog converter, a Sample and Hold, and an amplifier with a gain of 2. A 1.5 bit conversion resolution is also performed at each stage. The final stage is simply a comparator. Each resulting LSB-MSB couple is then time shifted to recover from the delay caused by the conversion. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple at each stage. The corrected data is output through the digital buffers.

The advantages of such a converter reside in the combination of pipeline architecture and the most advanced technologies. The highest dynamic performances are achieved while consumption remains at the lowest level.

7.1 RHF1201 operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operation modes offered by the RHF1201 are described in the following table.

Table 10. RHF1201 operating modes

Inputs						Outputs		
Analog input differential level			DFSB	OEB	SRC	OR	DR	Most significant bit (MSB)
(V_{IN}-V_{INB})	>	RANGE	H	L	X	H	CLK	D11
-RANGE	>	(V_{IN}-V_{INB})	H	L	X	H	CLK	D11
RANGE>	(V_{IN}-V_{INB})	>-RANGE	H	L	X	L	CLK	D11
(V_{IN}-V_{INB})	>	RANGE	L	L	X	H	CLK	D11 Complemented
-RANGE	>	(V_{IN}-V_{INB})	L	L	X	H	CLK	D11 Complemented
RANGE>	(V_{IN}-V_{INB})	>-RANGE	L	L	X	L	CLK	D11 Complemented
X			X	H	X	HZ	HZ	HZ
X			X	X	H	X	CLK	Low slew rate
X			X	X	L	X	CLK	High slew rate

Data format select (DFSB)

When set to low level (V_{IL}), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing.

When set to high level (V_{IH}), DFSB provides a standard binary output coding.

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Output enable (OEB)

When set to low level (V_{IL}), all digital outputs remain active and are in low impedance state. When set to high level (V_{IH}), all digital output buffers are in high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short T_{on} delay. This mechanism allows the chip select of the device.

Figure 3: Timing diagram on page 5 summarizes this functionality.

Slew rate control (SRC)

When set to high level (V_{IH}), all digital output currents are limited to a clamp value so that digital noise power is reduced to the minimum. When set to low level (V_{IL}), the output edges are twice as fast.

Out of range (OR)

This function is implemented on the output stage in order to set an “Out of Range” flag whenever the digital data is over the full scale range.

Typically, there is a detection of all the data at ’0’ or all the data at ’1’. It sets an output signal OR which is in low level state (V_{OL}) when the data stays within the range, or in high level state (V_{OH}) when the data is out of range.

Data ready (DR)

The Data Ready output is an image of the clock being synchronized on the output data (D0 to D11). This is a very helpful signal that simplifies the synchronization of the measurement equipment or of the controlling DSP.

As all other digital outputs, DR goes into high impedance state when OEB is set to high level as shown in *Figure 3: Timing diagram on page 5*.

7.2 Driving the analog input

7.2.1 Differential inputs

The RHF1201is designed to obtain optimum performance when driven on differential inputs. An RF transformer is an efficient way of achieving this high performance.

Figure 4: Differential input configuration describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs. The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set close to 0.5V. The INCM is de-coupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1 transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source.

Each analog input can drive a 1 V_{pp} amplitude input signal, so the resulting differential amplitude is 2 V_{pp}.

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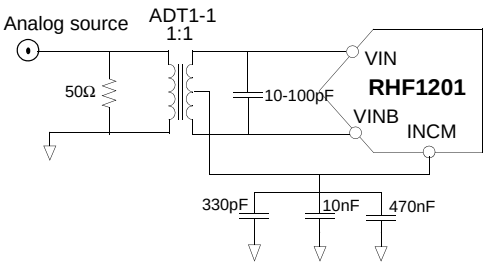
Figure 4. Differential input configuration



7.2.2 Single-ended input configuration

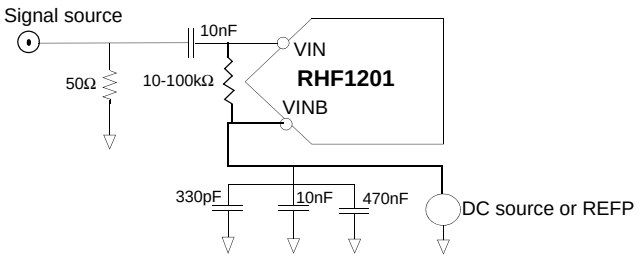
Some applications may require a single-ended input which is easily achieved with the configuration shown in *Figure 5: Single-ended input configuration*.

The lack of accurate differential driving with its common-mode noise and even harmonics cancellation advantages can degrade the rated RHF1201 performance. It is then recommended to use a well de-coupled DC reference to bias the RHF1201 inputs.

In this case, one can use an AC-coupled analog input and set the DC analog level with high value (10 kΩ to 100 kΩ) resistor connected to a proper DC source.

The internal references INCM (0.52 V) or REFP (1 V) can be used as proper DC sources. Using 1 V DC with a single signal of 2 V_{pp} input amplitude gives better SNR performance.

Figure 5. Single-ended input configuration



7.2.3 IF-sampling

The RHF1201 is specifically designed to meet sampling requirements for intermediate frequency input signals. In particular, the Track-and-Hold in the first stage of the pipeline is designed to minimize the linearity limitations as analog frequency increases.This is achieved by making the input impedance independent from the input frequency.

As a result, the RHF1201 can maintain high performance up to an analog frequency of 150 MHz.

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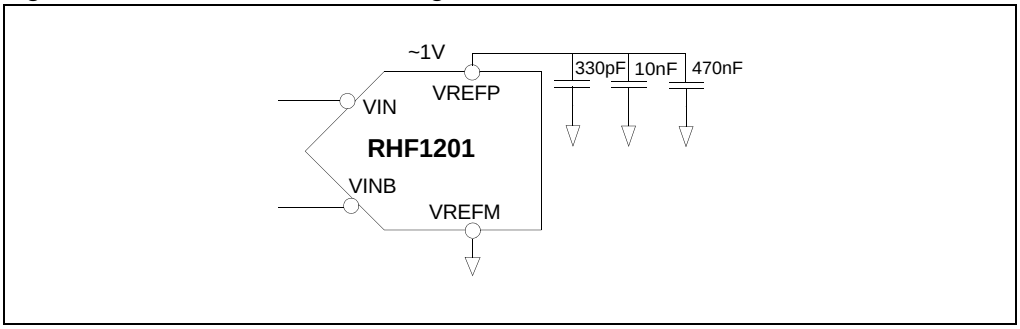
7.3 Reference connection

7.3.1 Internal reference

In the standard configuration, the ADC is biased with the internal reference voltage. The V_{REFM} pin is connected to Analog Ground while V_{REFP} is internally set to a voltage close to 1.0 V. It is recommended to de-couple the V_{REFP} in order to minimize low and high frequency noise. Refer to *Figure 6: Internal reference setting* for the schematics.

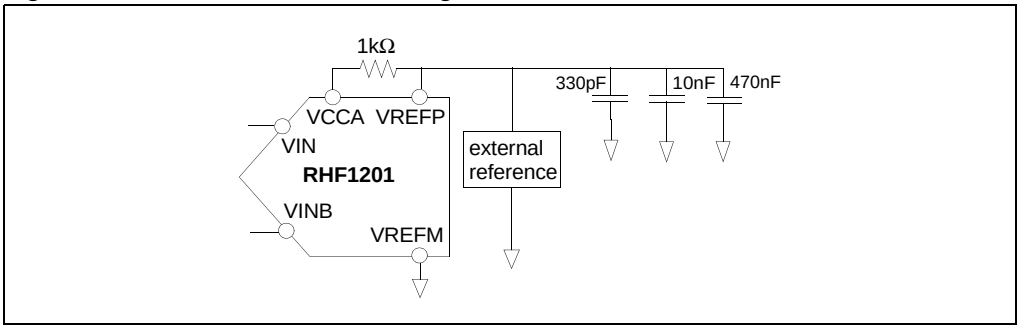
Figure 6. Internal reference setting



7.3.2 External reference

It is possible to use an external reference voltage instead of the internal one for specific applications requiring even better linearity or enhanced temperature behavior. In this case, the amplitude of the external voltage must be at least equal to the internal one (1.0 V). You can use an external voltage reference with the configuration shown in *Figure 7: External reference setting* to obtain optimum performance.

Figure 7. External reference setting



This can be very helpful in multichannel applications for example to maintain a good matching along the sampling frequency range.

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7.4 Clock input

The quality of your converter is very dependent on your clock input accuracy, in terms of aperture jitter; the use of a low jitter crystal controlled oscillator is recommended.

Further points to consider in your implementation are:

- The input signal must be square-shaped with sharp edges of less than 1 ns.
- At 45 Msps, the duty cycle must be between 45% and 65%; in any case, the high level duration of Clock must be longer than 10 ns.
- The clock power supplies must be independent from the ADC output supplies to avoid digital noise modulation on the output.
- When powered-on, the circuit needs several clock periods to reach its normal operating conditions.

7.5 Power consumption optimization

The internal architecture of the RHF1201 makes it possible to optimize power consumption according to the sampling frequency of the application. For this purpose, an External R_{pol} resistor is placed between the IPOL pin and the analog Ground. Therefore, the total dissipation can be adjusted across all the sampling range 0.5 Msps to 50 Msps to fulfil the requirements of applications where power saving is a must.

For low sampling frequency, this value of resistor may be adjusted in order to decrease the analog current without any degradation of dynamic performance.

Table 11 sums up the relevant data.

Table 11. Total power consumption optimization depending on R_{pol} value

F_S (Msps)	0.85	1.7	13.6	45	50
R_{pol} (kΩ)	100	70	35	24	18
Optimized power (mW)	44	47	60	93	100

7.6 Layout precautions

- Use of dedicated ground planes (analog, digital, internal and external buffer ones) on the PCB is recommended for high speed circuit applications to provide low inductance and low resistance common return.
- The separation of the analog signal from the digital output part is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.
- All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.
- Keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes.
- Choose component sizes as small as possible (SMD).

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8 Definitions of specified parameters

Static parameters

Static measurements are performed using the histograms method on a 2 MHz input signal, sampled at 50 Msps, which is high enough to fully characterize the test frequency response. The input level is +1 dBFS to saturate the signal.

Differential non linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral non linearity (INL)

An ideal converter exhibits a transfer function which is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

Dynamic parameters

Dynamic measurements are performed by spectral analysis, applied to an input sine wave of various frequencies and sampled at 50 Msps.

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always an harmonic) and the amplitude of fundamental tone (signal power) over the full Nyquist band. It is expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to noise and distortion ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

The effective number of bits (ENOB) is easily deduced from the SINAD, using the formula:

SINAD = 6.02 $\times$ ENOB + 1.76 dB.

When the applied signal is not full scale (FS), but has an amplitude A_0, the SINAD expression becomes:

SINAD = 6.02 $\times$ ENOB + 1.76 dB + 20 log ($2A_0$/FS)

The ENOB is expressed in bits.

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Effective resolution bandwidth

For a given sampling rate and clock jitter, the analog input frequency at which the SINAD is reduced of 3 dB.

Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output on the output bus. Also called data latency. It is expressed as a number of clock cycles.

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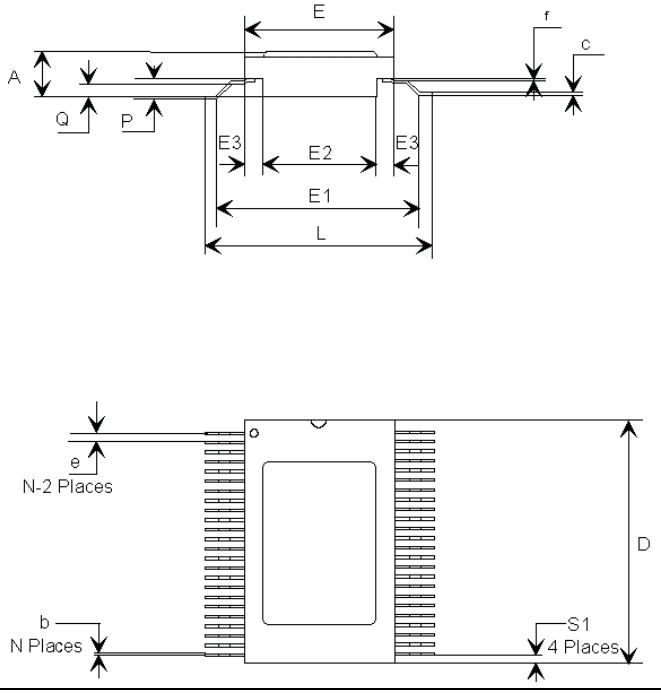
9 Package information

Figure 8. SO-48 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E1		10.90			0.429	
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	12.28	12.58	12.88	0.483	0.495	0.507
P	1.30	1.45	1.60	0.051	0.057	0.063
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024



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10 Ordering information

Part number	Temperature range	Package	Marking
RHF1201KSO1	-55 °C to 125 °C	SO-48	RHF1201KSO1
RHF1201KSO2	-55 °C to 125 °C	SO-48	RHF1201KSO2
RHF1201KSO-01V	-55 °C to 125 °C	SO-48	F0521701VXC

11 Revision history

Date	Revision	Changes
01-Sep-2006	1	Initial release in new format.
29-Jun-2007	2	Updated failure immune and latchup immune value to 120 MeV-cm^2/mg. Updated package mechanical data. Removed reference to non rad-hard components from *Section 7.3.2: External reference on page 12*.

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