

54ABT574

Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT574 is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'ABT374 except for the pinouts.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ABT374

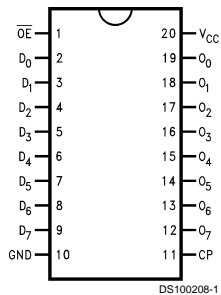
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9322001

Ordering Code

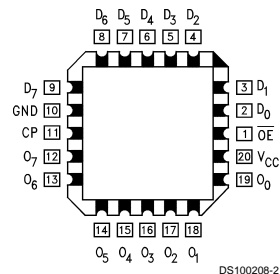
Military	Package Number	Package Description
54ABT574J/883	J20A	20-Lead Ceramic Dual-In-Line
54ABT574W/883	W20A	20-Lead Cerpack
54ABT574E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)
O ₀ -O ₇	TRI-STATE Outputs

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Functional Description

The 'ABT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs are in a high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

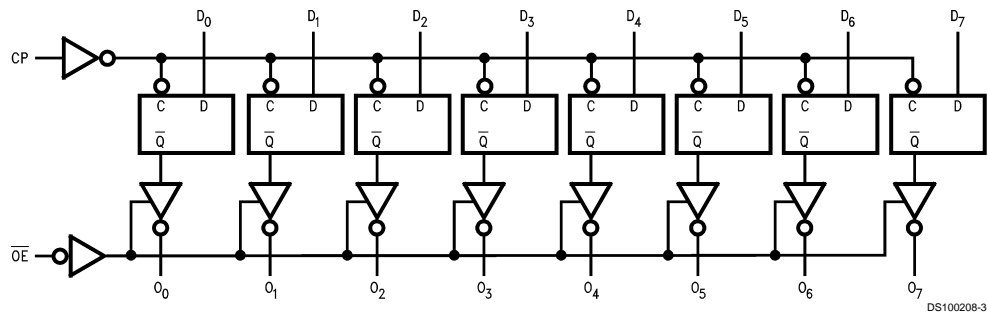
Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H or L	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 NC = No Change

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H or L	L	NC	Z	Hold

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to 5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT574			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA
		54ABT	2.0		V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage	54ABT	0.55		V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4) V _{IN} = V _{CC}
			5		μA	Max	V _{IN} = 7.0V
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		-5		μA	Max	V _{IN} = 0.5V (Note 4) V _{IN} = 0.0V
			-5		μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current		50		μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current		-50		μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Other GND
I _{CCH}	Power Supply Current		50		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		30		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		50		μA	Max	\overline{OE} = V _{CC} All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA	Max	V _I = V _{CC} - 2.1V Enable Input V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
		Outputs TRI-STATE	2.5		mA		
		Outputs TRI-STATE	2.5		mA		
I _{CCD}	Dynamic I _{CC} (Note 4)	No Load		0.30	mA/ MHz	Max	Outputs Open, \overline{OE} = GND, One Bit Toggling (Note 3), 50% Duty Cycle

Note 3: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH}	Propagation Delay	1.5	7.0	ns
t_{PHL}	CP to O_n	1.5	7.4	
t_{PZH}	Output Enable Time	1.0	6.5	ns
t_{PZL}		1.0	7.2	
t_{PHZ}	Output Disable Time	1.0	7.2	ns
t_{PLZ}		1.0	6.7	

AC Operating Requirements

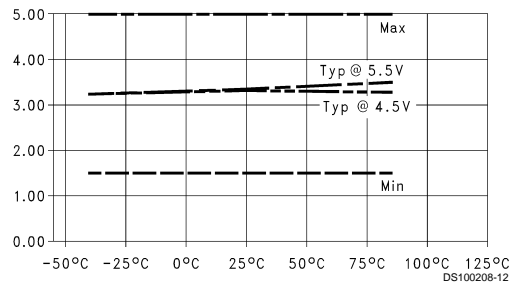
Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
$t_s(\text{H})$	Setup Time, HIGH	1.5		ns
$t_s(\text{L})$	or LOW D_n to CP	2.0		
$t_h(\text{H})$	Hold Time, HIGH	2.0		ns
$t_h(\text{L})$	or LOW D_n to CP	2.0		
$t_w(\text{H})$	Pulse Width, CP,	3.3		ns
$t_w(\text{L})$	HIGH or LOW	3.3		

Capacitance

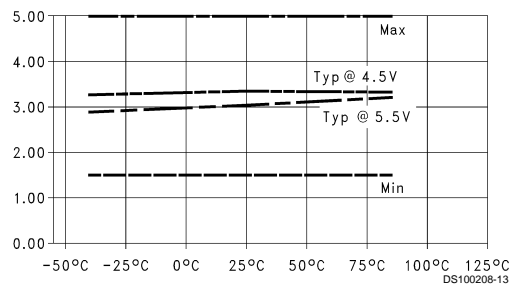
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

T_{PHL} vs Temperature (T_A) $C_L = 50\text{ pF}$,
1 Output Switching, Clock to Output

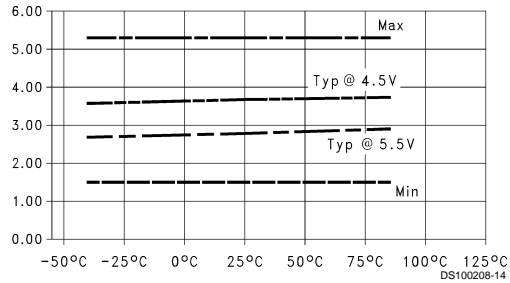


T_{PLH} vs Temperature (T_A) $C_L = 50\text{ pF}$,
1 Output Switching, Clock to Output

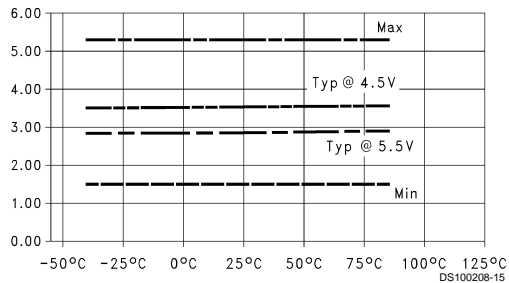


Capacitance (Continued)

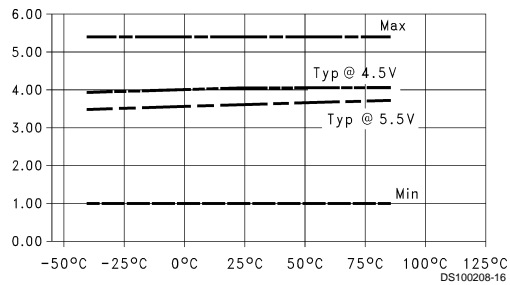
**T_{PZH} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, OE to Output**



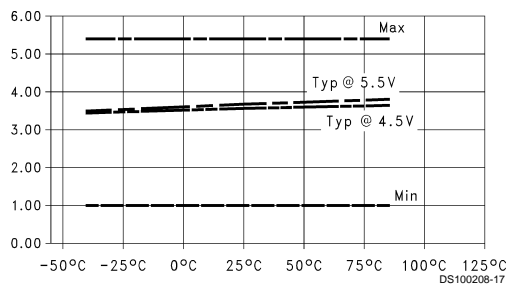
**T_{PZL} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, OE to Output**



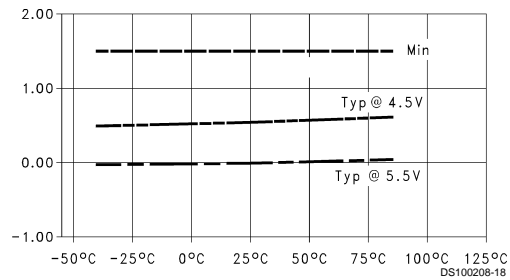
**T_{PHZ} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, OE to Output**



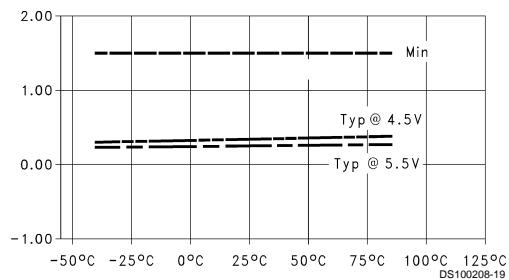
**T_{PLZ} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, OE to Output**



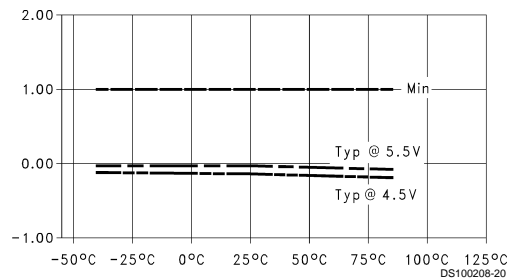
**T_{SET} LOW vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, Data to Clock**



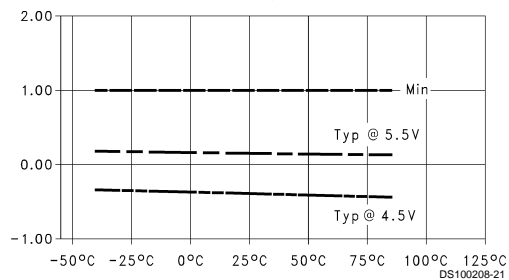
**T_{SET} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, Data to Clock**



**T_{HOLD} HIGH vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, Data to Clock**

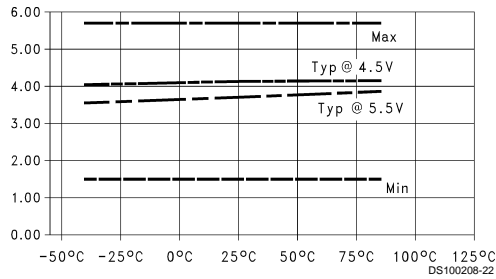


**T_{HOLD} LOW vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching, Data to Clock**

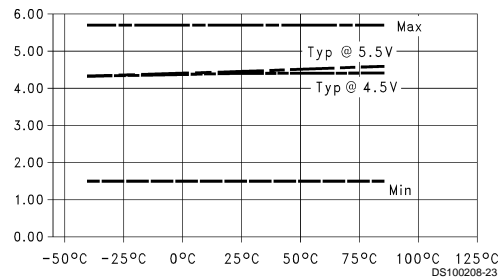


Capacitance (Continued)

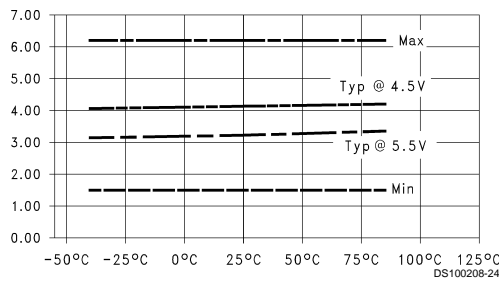
**T_{PLH} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, Clock to Output**



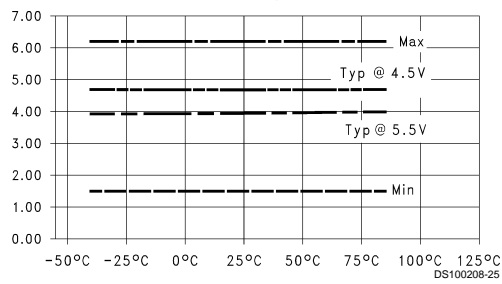
**T_{PHL} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, Clock to Output**



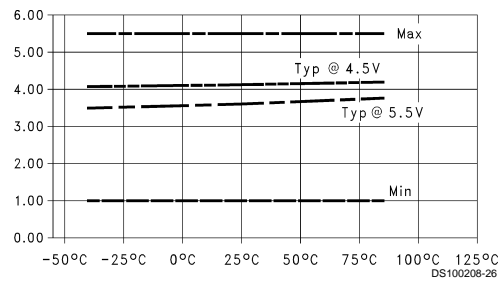
**T_{PZH} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, OE to Output**



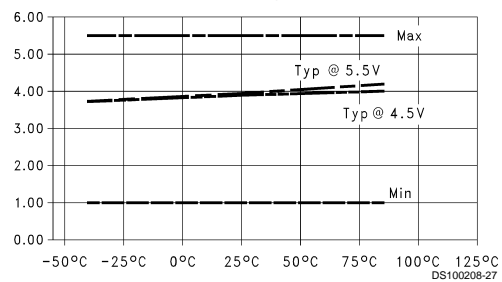
**T_{PZL} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, OE to Output**



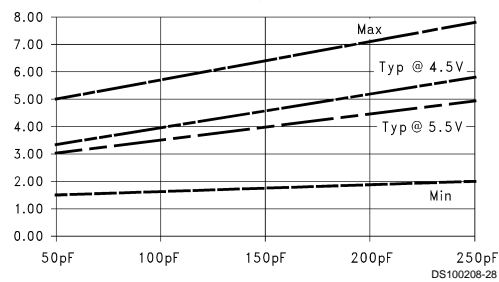
**T_{PHZ} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, OE to Output**



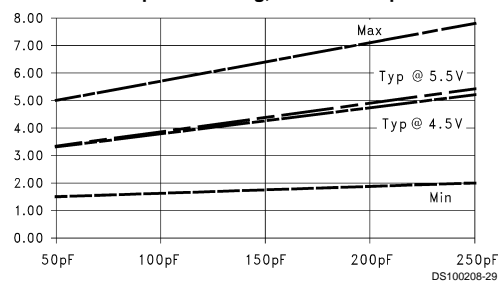
**T_{PLZ} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching, OE to Output**



**T_{PLH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
1 Output Switching, Clock to Output**

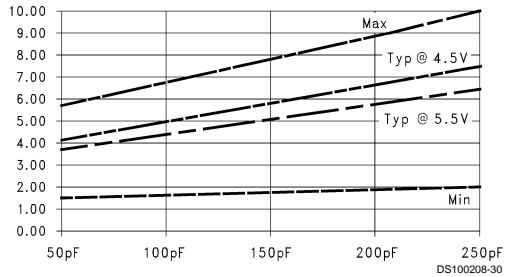


**T_{PHL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
1 Output Switching, Clock to Output**

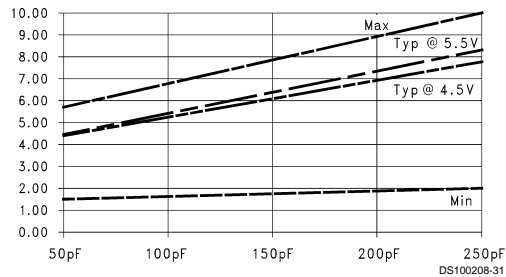


Capacitance (Continued)

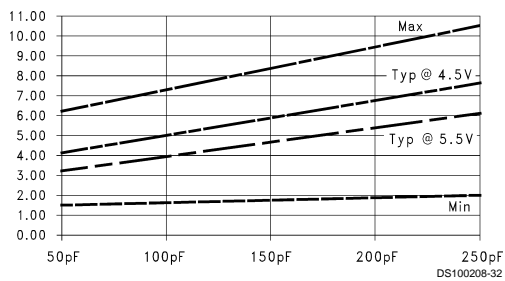
**T_{PLH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching, Clock to Output**



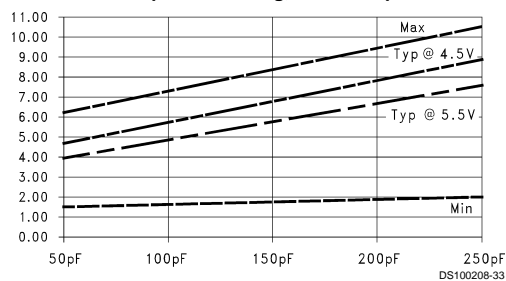
**T_{PHL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching, Clock to Output**



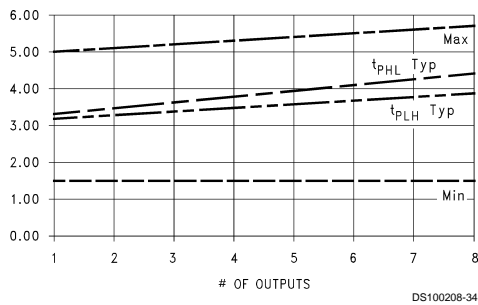
**T_{PZH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching, OE to Output**



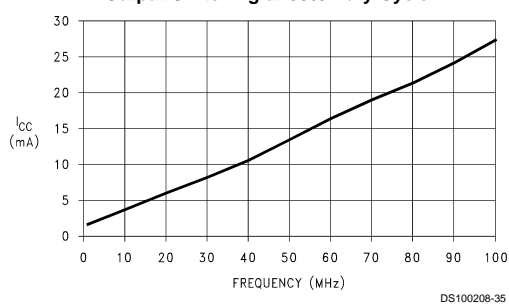
**T_{PZL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching, OE to Output**



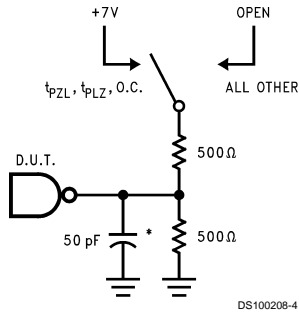
**T_{PLH} and T_{PHL} vs Number Outputs Switching
 $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$,
Outputs In Phase, Clock to Output**



**Typical I_{CC} vs Output Switching Frequency
 $C_L = 0 \text{ pF}$, $V_{CC} = V_{IH} = 5.5\text{V}$,
1 Output Switching at 50% Duty Cycle**



AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

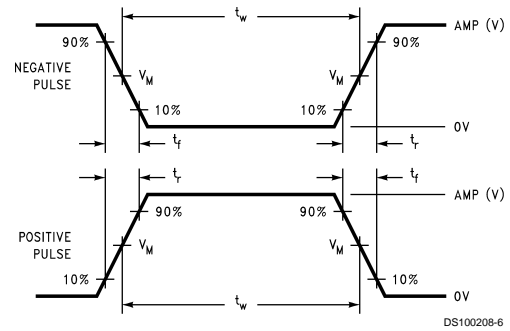


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

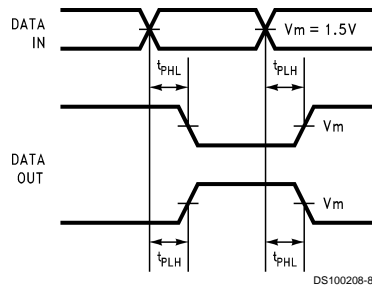


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

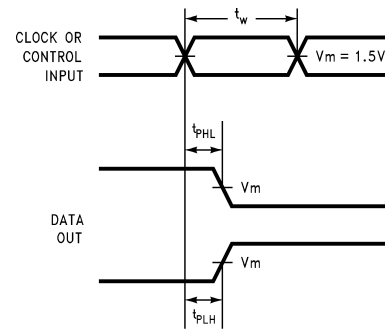


FIGURE 5. Propagation Delay, Pulse Width Waveforms

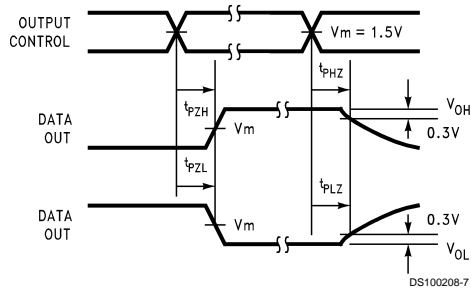


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

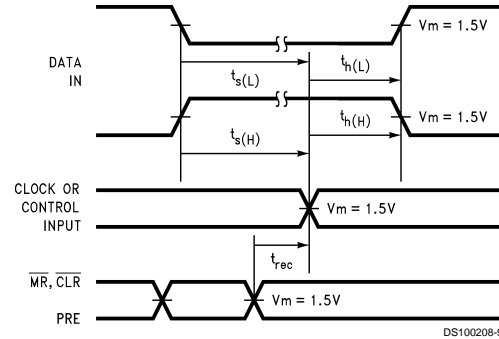
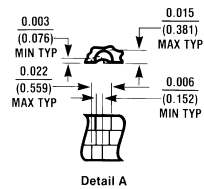
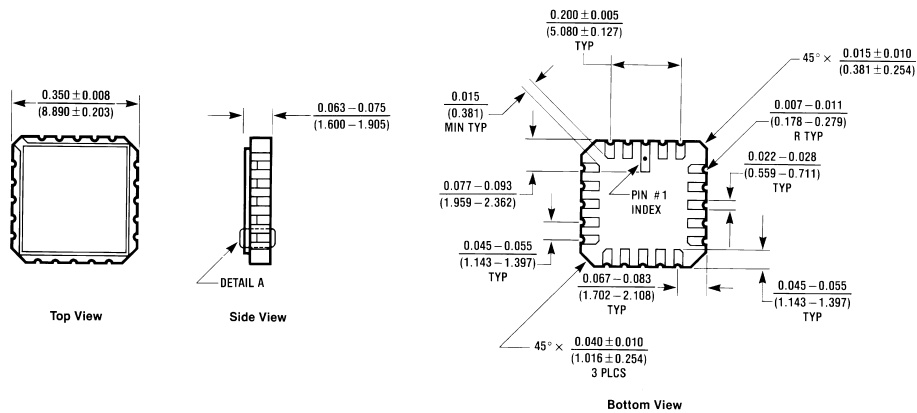


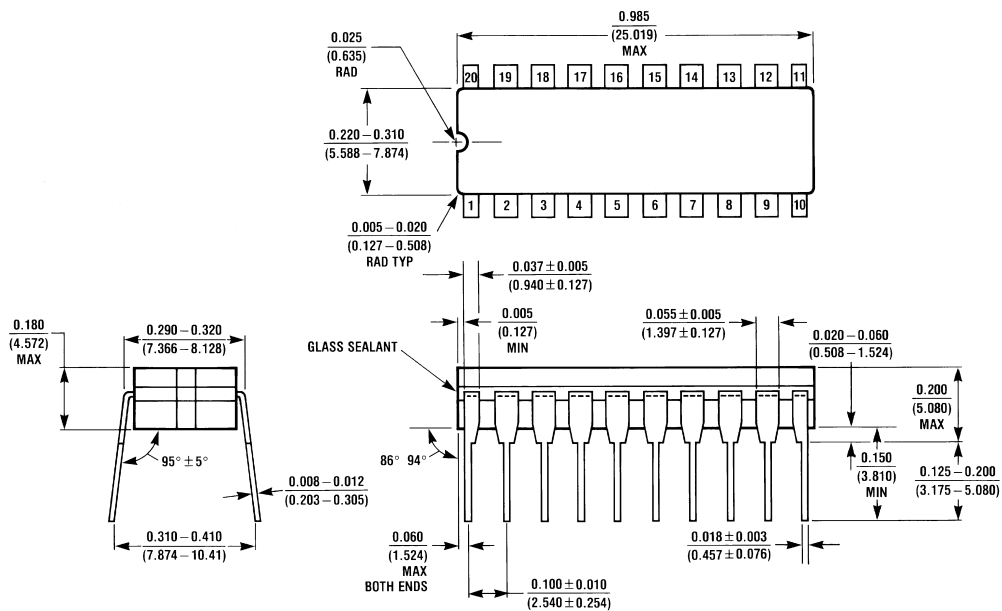
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

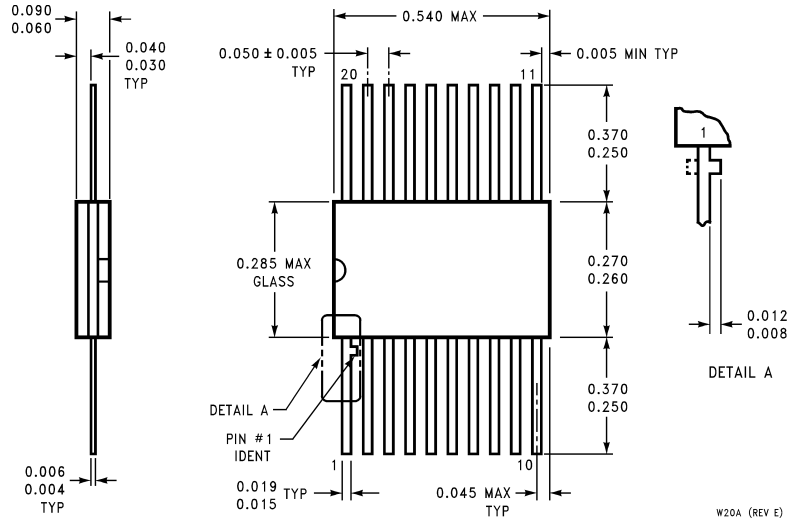
20-Terminal Ceramic Chip Carrier (L)
 NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
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