National Semiconductor

August 1998

# 54ABT541
# Octal Buffer/Line Driver with TRI-STATE® Outputs

## General Description

The 'ABT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541 is similar to the 'ABT244 with broadside pinout.

## Features

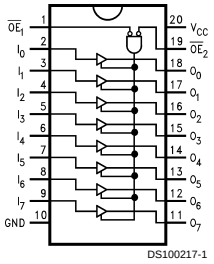
- Non-inverting buffers
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Flow-through pinout for ease of PC board layout
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9471801

## Ordering Code

| Military | Package Number | Package Description |
|---|---|---|
| 54ABT541J-QML | J20A | 20-Lead Ceramic Dual-In-Line |
| 54ABT541W-QML | W20A | 20-Lead Cerpack |
| 54ABT541E-QML | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

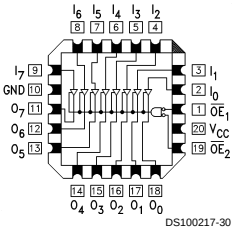
## Connection Diagram

**Pin Assignment**
**DIP and Cerpack**




DS100217-1

**Pin Assignment**
**LCC**




DS100217-30

| Pin Names | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | Output Enable Input (Active Low) |
| $I_0$–$I_7$ | Inputs |
| $O_0$–$O_7$ | Outputs |

## Truth Table

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | I | ABT541 |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |
| L | L | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Storage Temperature | −65˚C to +150˚C |
| Ambient Temperature under Bias | −55˚C to +125˚C |
| Junction Temperature under Bias | |
| Ceramic | −55˚C to +175˚C |
| $V_{CC}$ Pin Potential to | |
| Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Any Output | |
| in the Disabled or | |
| Power-Off State | −0.5V to 5.5V |
| in the HIGH State | −0.5V to $V_{CC}$ |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| DC Latchup Source Current | −500 mA |
| Over Voltage Latchup (I/O) | 10V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | −55˚C to +125˚C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Minimum Input Edge Rate | (ΔV/Δt) |
| Data Input | 50 mV/ns |
| Enable Input | 20 mV/ns |

## DC Electrical Characteristics

| Symbol | Parameter | | ABT541 Min | ABT541 Typ | ABT541 Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54ABT | 2.5 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 54ABT | 2.0 | | | V | Min | $I_{OH}$ = −24 mA |
| $V_{OL}$ | Output LOW Voltage | 54ABT | | | 0.55 | V | Min | $I_{OL}$ = 48 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5 | μA | Max | $V_{IN}$ = 2.7V (Note 4) |
| | | | | | 5 | | | $V_{IN}$ = $V_{CC}$ |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | | −5 | μA | Max | $V_{IN}$ = 0.5V (Note 4) |
| | | | | | −5 | | | $V_{IN}$ = 0.0V |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA<br>All Other Pins Grounded |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | μA | 0 − 5.5V | $V_{OUT}$ = 2.7V; $\overline{OE}_n$ = 2.0V |
| $I_{OZL}$ | Output Leakage Current | | | | −50 | μA | 0 − 5.5V | $V_{OUT}$ = 0.5V; $\overline{OE}_n$ = 2.0V |
| $I_{OS}$ | Output Short-Circuit Current | | −100 | | −275 | mA | Max | $V_{OUT}$ = 0.0V |
| $I_{CEX}$ | Output High Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | | 100 | μA | 0.0 | $V_{OUT}$ = 5.5V; All Others GND |
| $I_{CCH}$ | Power Supply Current | | | | 50 | μA | Max | All Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | | | | 30 | mA | Max | All Outputs LOW |
| $I_{CCZ}$ | Power Supply Current | | | | 50 | μA | Max | $\overline{OE}_n$ = $V_{CC}$;<br>All Others at $V_{CC}$ or Ground |
| $I_{CCT}$ | Additional $I_{CC}$/Input | Outputs Enabled | | | 2.5 | mA | | $V_I$ = $V_{CC}$ − 2.1V |
| | | Outputs TRI-STATE | | | 2.5 | mA | Max | Enable Input $V_I$ = $V_{CC}$ − 2.1V |
| | | Outputs TRI-STATE | | | 50 | μA | | Data Input $V_I$ = $V_{CC}$ − 2.1V;<br>All Others at $V_{CC}$ or Ground |
| $I_{CCD}$ | Dynamic $I_{CC}$ (Note 4) | No Load | | | 0.1 | mA/MHz | Max | Outputs Open, $\overline{OE}_n$ = GND,<br>One Bit Toggling (Note 3),<br>50% Duty Cycle |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Note 3:** For 8 bits toggling, $I_{CCD}$ < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## DC Electrical Characteristics

| Symbol | Parameter | Min | Max | Units | $V_{CC}$ | Conditions $C_L$ = 50 pF, $R_L$ = 500Ω |
|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | | 1.0 | V | 5.0 | $T_A$ = 25°C (Note 5) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | | -1.45 | V | 5.0 | $T_A$ = 25°C (Note 5) |

**Note 5:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol | Parameter | 54ABT $T_A$ = −55°C to +125°C $V_{CC}$ = 4.5V–5.5V $C_L$ = 50 pF | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 1.0 | 5.0 | ns |
| $t_{PHL}$ | Data to Outputs | 1.0 | 5.3 | |
| $t_{PZH}$ | Output Enable Time | 1.1 | 7.2 | ns |
| $t_{PZL}$ | | 1.5 | 7.9 | |
| $t_{PHZ}$ | Output Disable Time | 1.5 | 7.5 | ns |
| $t_{PLZ}$ | | 1.5 | 7.9 | |

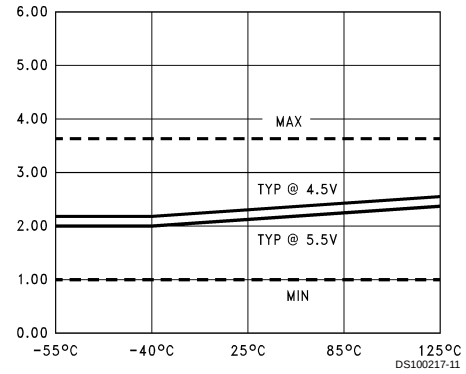
## Capacitance

| Symbol | Parameter | Typ | Units | Conditions $T_A$ = 25°C |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5.0 | pF | $V_{CC}$ = 0.0V |
| $C_{OUT}$ (Note 6) | Output Capacitance | 9.0 | pF | $V_{CC}$ = 5.0V |

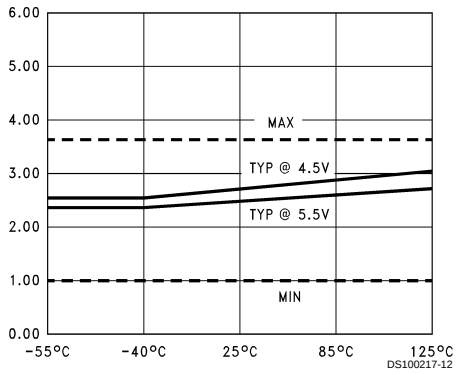
**Note 6:** $C_{OUT}$ is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.

## Capacitance (Continued)

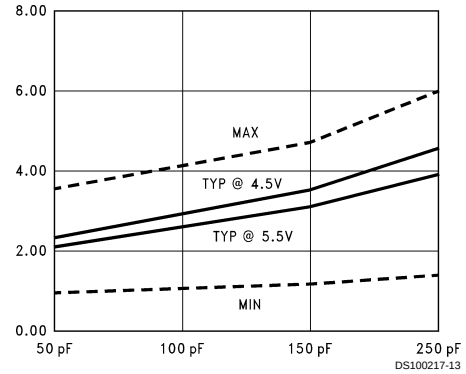
**$t_{PLH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



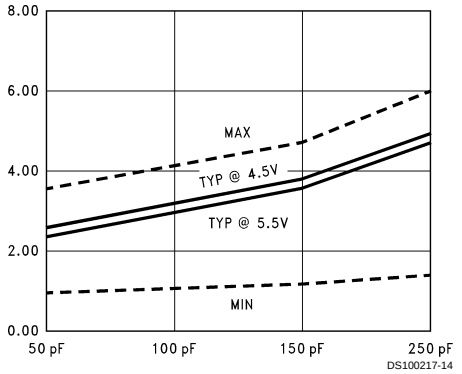

**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



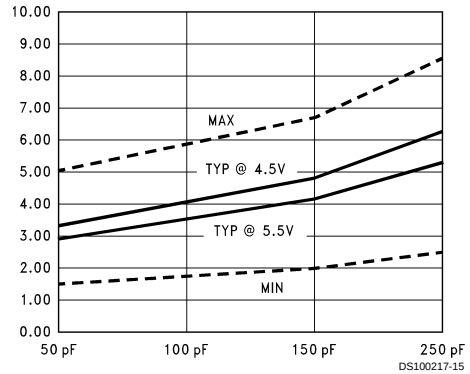

**$t_{PLH}$ vs Load Capacitance**
**1 Output Switching, $T_A$ = 25˚C**



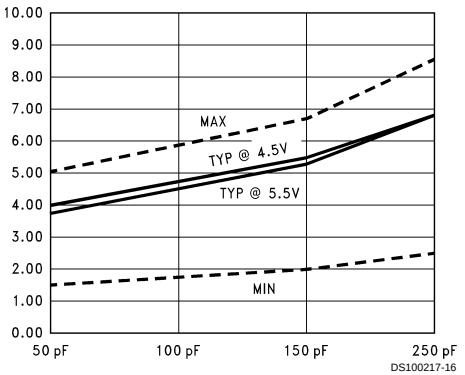

**$t_{PHL}$ vs Load Capacitance**
**1 Output Switching, $T_A$ = 25˚C**




**$t_{PLH}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25˚C**



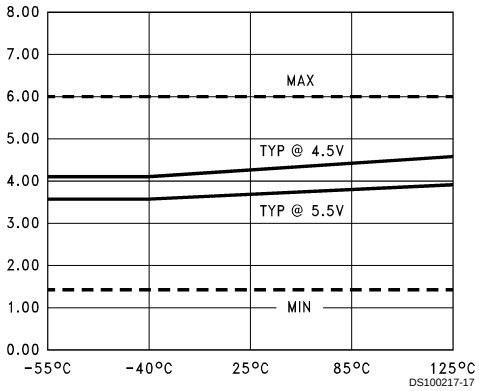

**$t_{PHL}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25˚C**



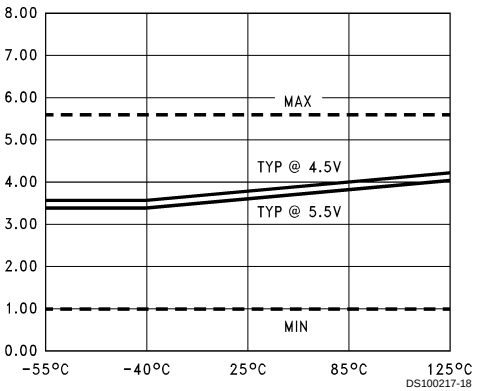

Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## Capacitance (Continued)

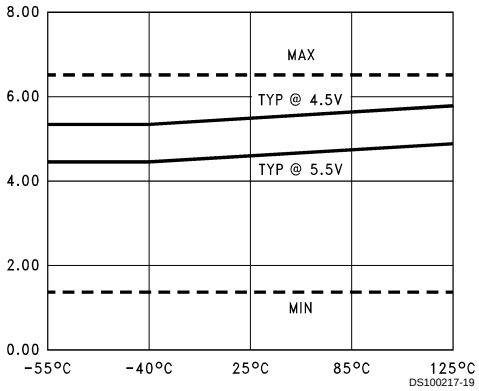
**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



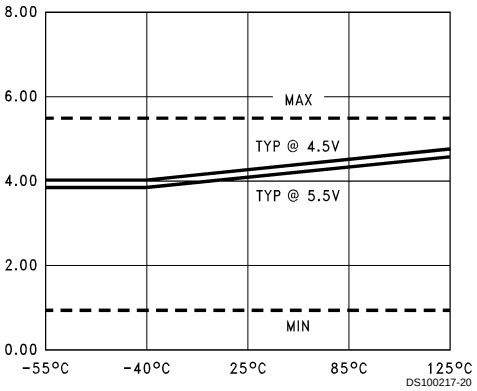

**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



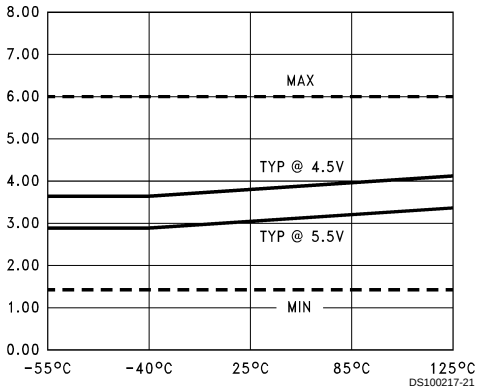

**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**



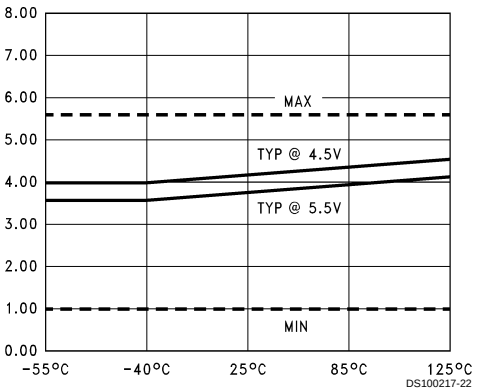

**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**




**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



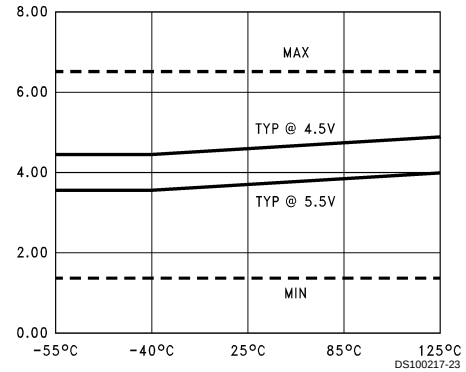

**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**



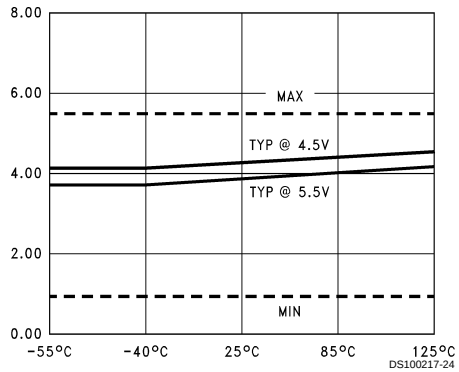

Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## Capacitance (Continued)

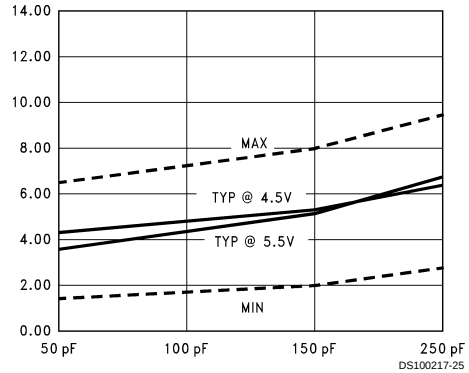
**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**



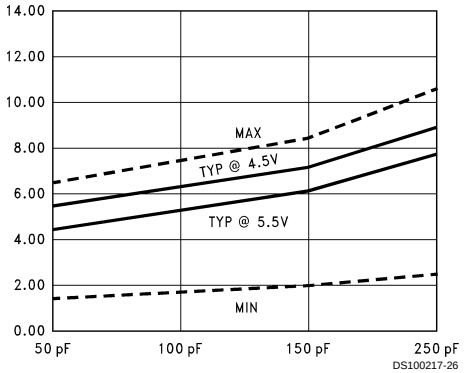

**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**



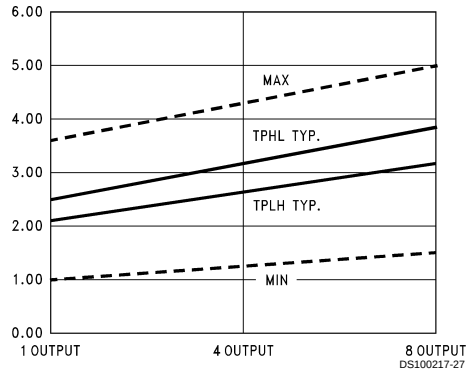

**$t_{PZH}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25˚C**



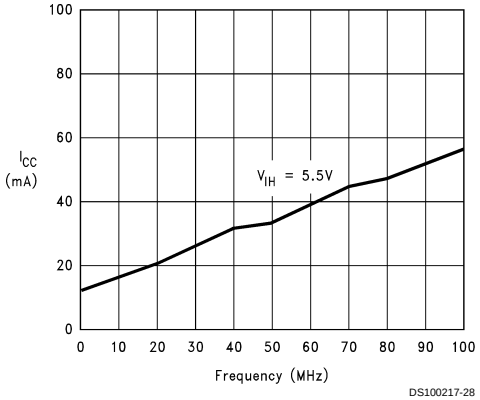

**$t_{PZL}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25˚C**




**$t_{PLH}$ and $t_{PHL}$ vs Number Outputs Switching**
**$V_{CC}$ = 5.0V, $T_A$ = 25˚C, $C_L$ = 50 pF**

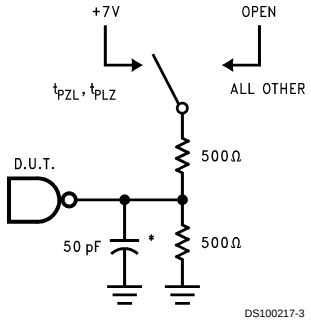



**$I_{CC}$ vs Frequency,**
**Average, $T_A$ = 25˚C,**
**All Outputs Unloaded/Unterminated**




Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## AC Loading




*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**

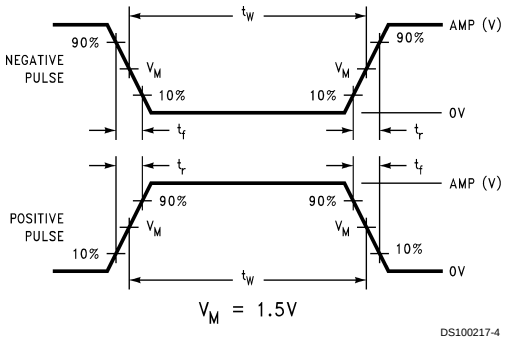



**FIGURE 2. Test Input Signal Levels**

| Amplitude | Rep. Rate | $t_w$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 3. Test Input Signal Requirements**

## AC Waveforms

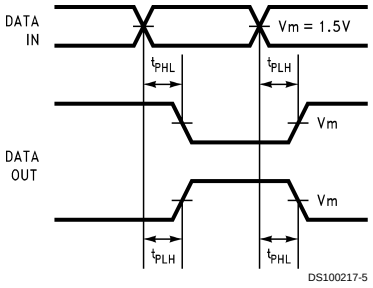



**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

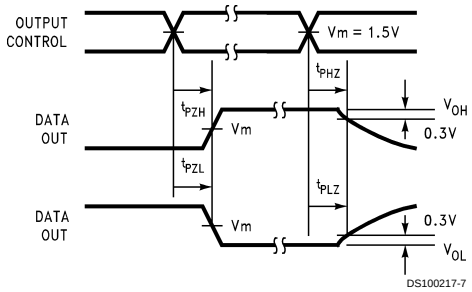
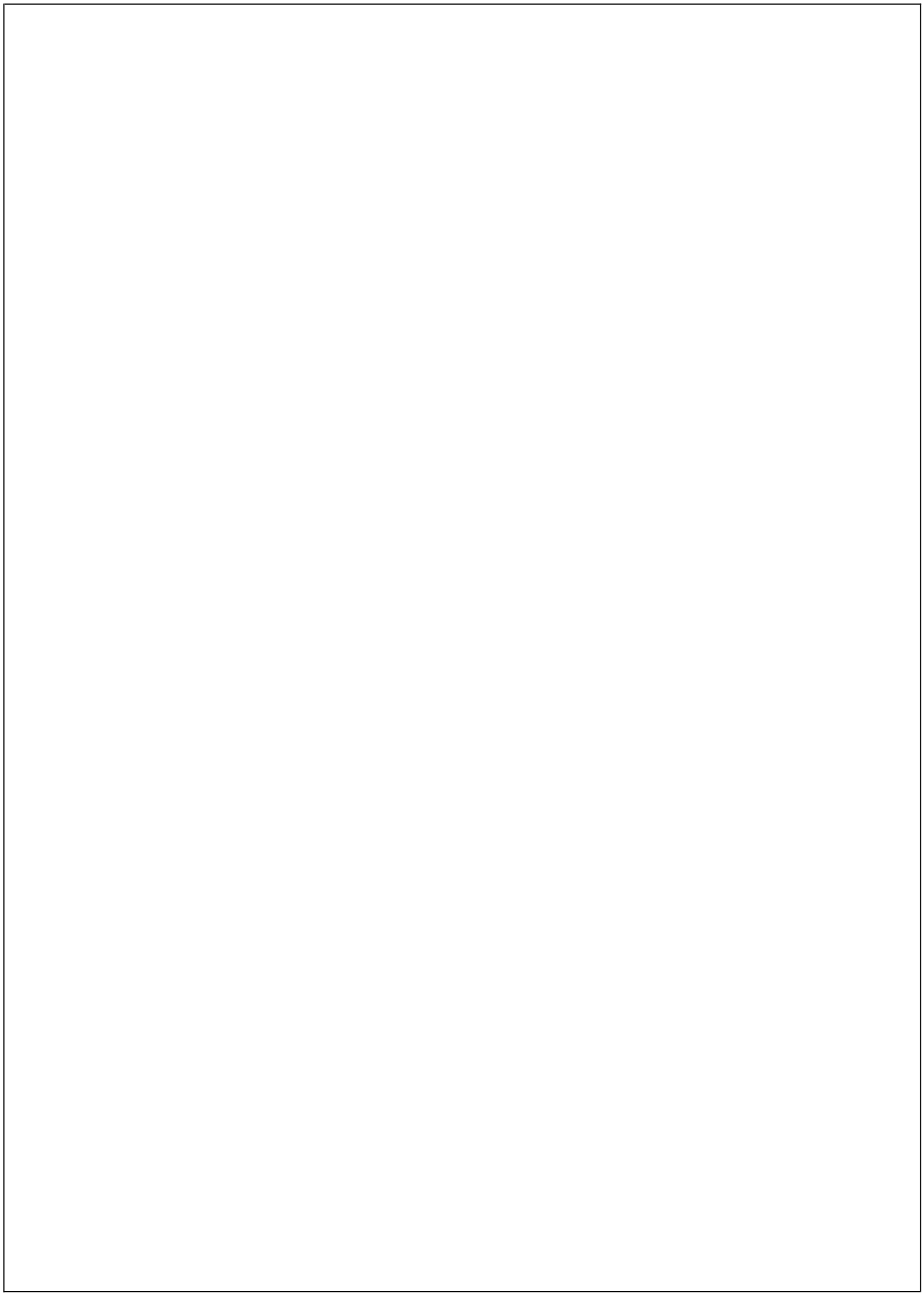
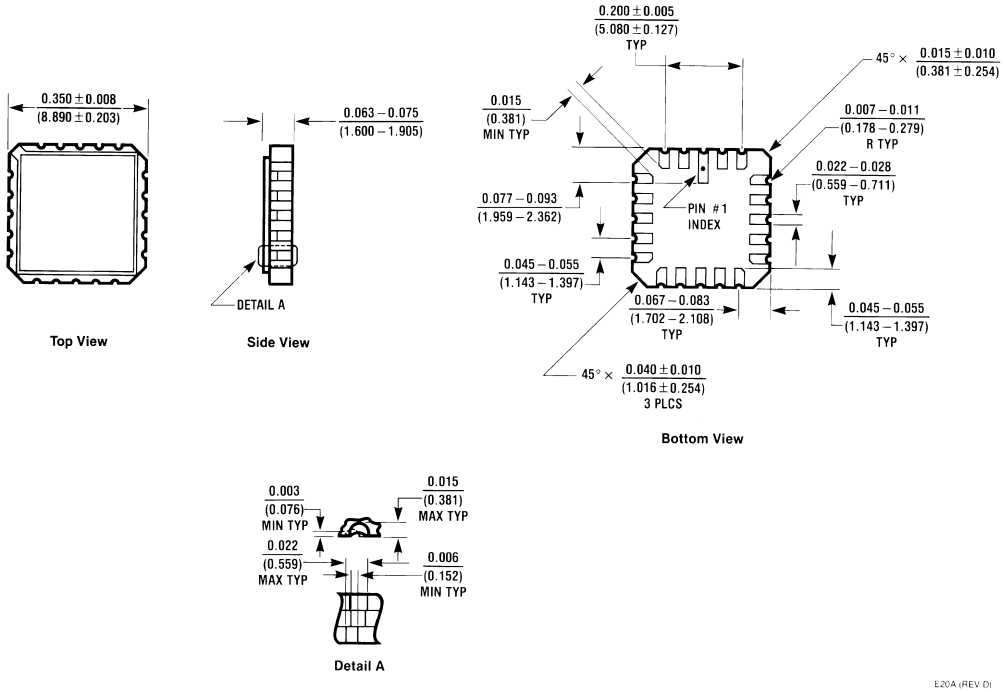


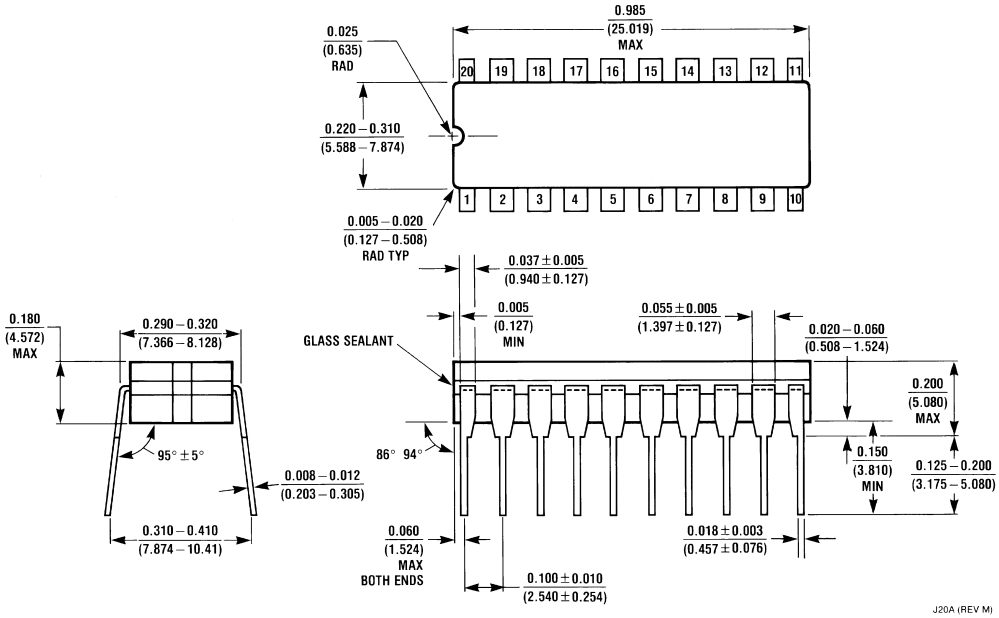

**FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time**



## Physical Dimensions inches (millimeters) unless otherwise noted

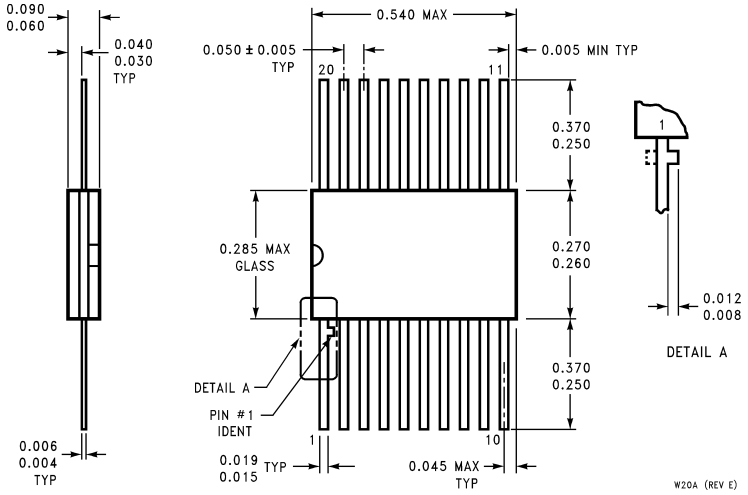



**20-Terminal Ceramic Chip Carrier**
**NS Package Number E20A**




**20-Lead Ceramic Dual-In-Line Package**
**NS Package Number J20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Ceramic Flatpack**
**NS Package Number W20A**

### LIFE SUPPORT POLICY

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