

54F/74F534 Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'F534 is a high speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

Features

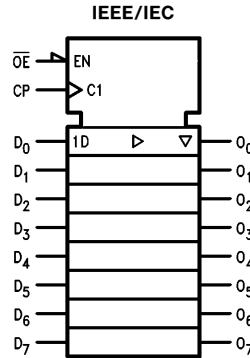
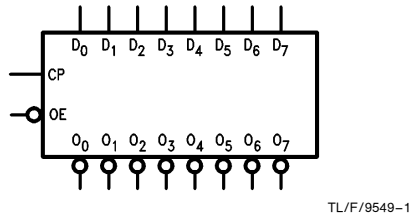
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F534PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F534DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F534SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F534SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F534FM (Note 2)	W20A	20-Lead Cerpack
	54F534LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX, and SJX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols



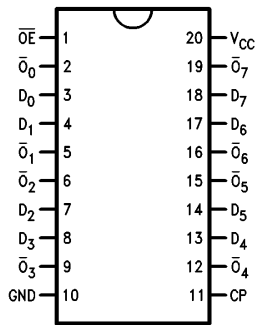
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 - D_7	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{O}_0 - \overline{O}_7	Complementary TRI-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

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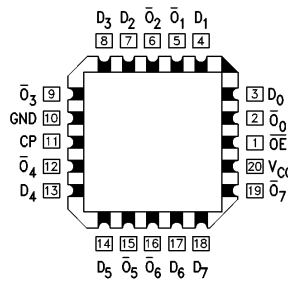
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/9549-2

Pin Assignment
for LCC



TL/F/9549-3

Functional Description

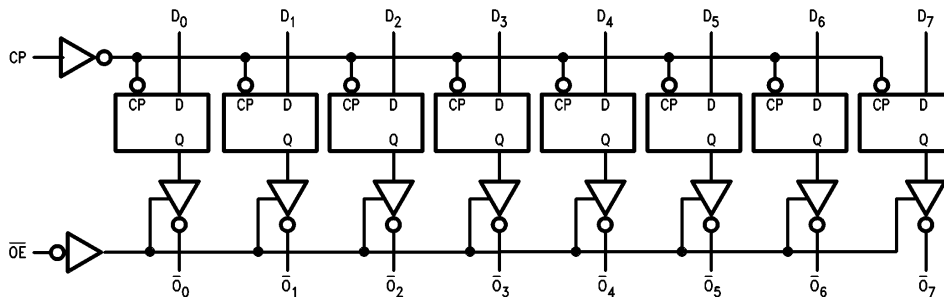
The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Output
CP	OE	D	\overline{O}
—	L	H	L
—	L	L	H
L	L	X	\overline{O}_0
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 — = LOW-to-HIGH Clock Transition
 Z = High Impedance
 \overline{O}_0 = Value stored from previous clock cycle

Logic Diagram



TL/F/9549-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min		I _{OH} = -1 mA
		54F 10% V _{CC}	2.4					I _{OH} = -3 mA
		74F 10% V _{CC}	2.5					I _{OH} = -1 mA
		74F 10% V _{CC}	2.4					I _{OH} = -3 mA
		74F 5% V _{CC}	2.7					I _{OH} = -1 mA
		74F 5% V _{CC}	2.7					I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC}			V	Min		I _{OL} = 20 mA
		74F 10% V _{CC}						I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F			μA	Max		V _{IN} = 2.7V
		74F						
I _{BVI}	Input HIGH Current Breakdown Test	54F			μA	Max		V _{IN} = 7.0V
		74F						
I _{CEX}	Output HIGH Leakage Current	54F			μA	Max		V _{OUT} = V _{CC}
		74F						
V _{ID}	Input Leakage Test	74F	4.75		V	0.0		I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			μA	0.0		V _{IOD} = 1.50 μA All Other Pins Grounded
I _{IL}	Input LOW Current				mA	Max		V _{IN} = 0.5V
I _{OZH}	Output Leakage Current				μA	Max		V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current				μA	Max		V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current				mA	Max		V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test				μA	0.0V		V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current				mA	Max		V _O = HIGH Z

AC Electrical Characteristics

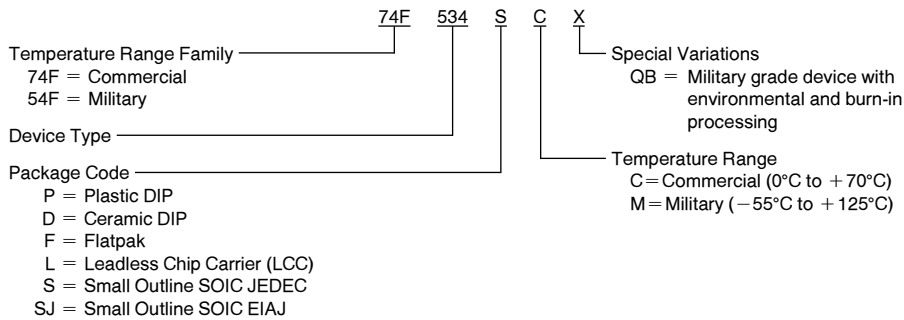
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100			60		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to \bar{O}_n	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
t _{PZH} t _{PZL}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.3	7.0	1.5	8.0	1.5	8.0	ns
		1.5	4.3	5.5	1.5	7.5	1.5	6.5	

AC Operating Requirements

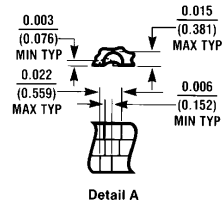
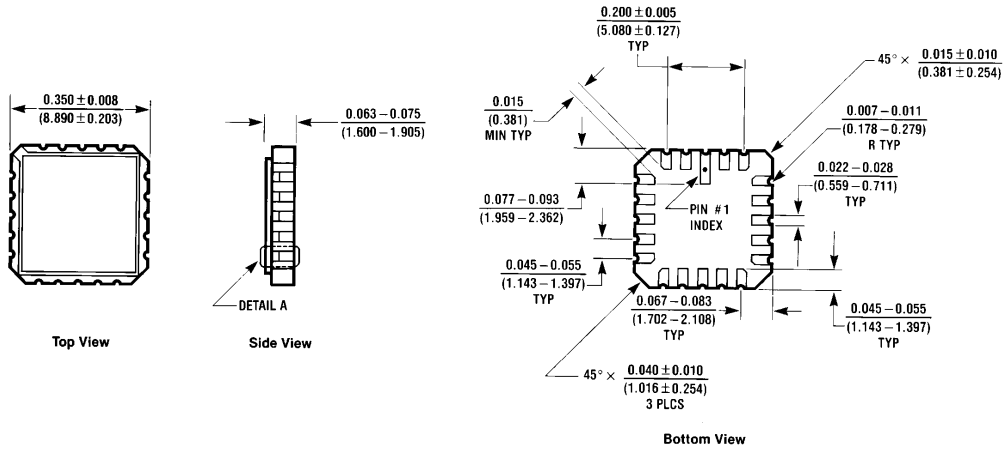
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to CP	2.0		2.0		2.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to CP	2.0		2.0		2.0		
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	7.0		7.0		7.0		ns
		6.0		6.0		6.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

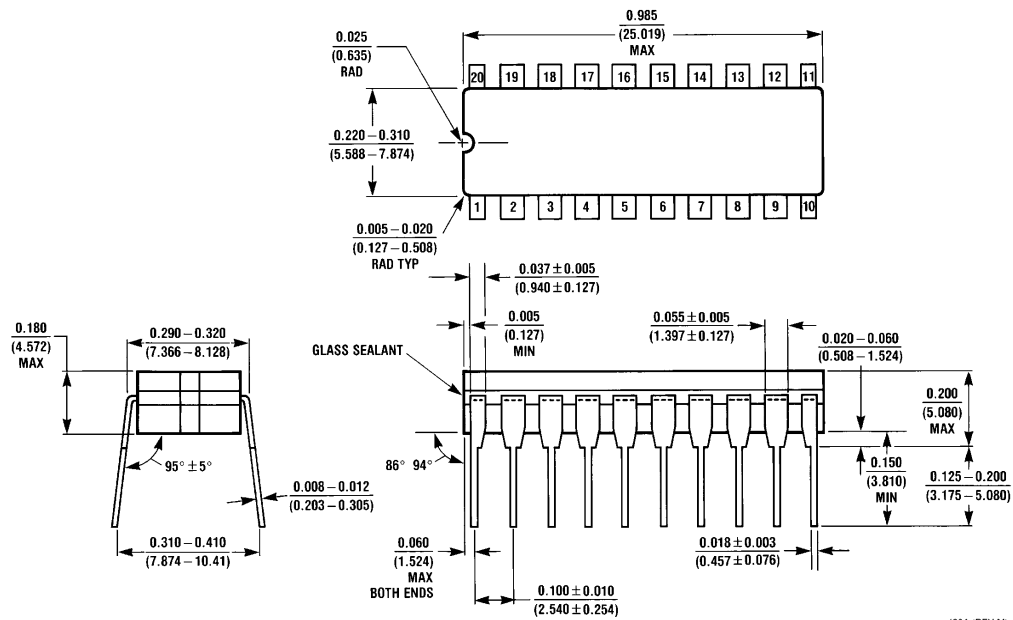


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A

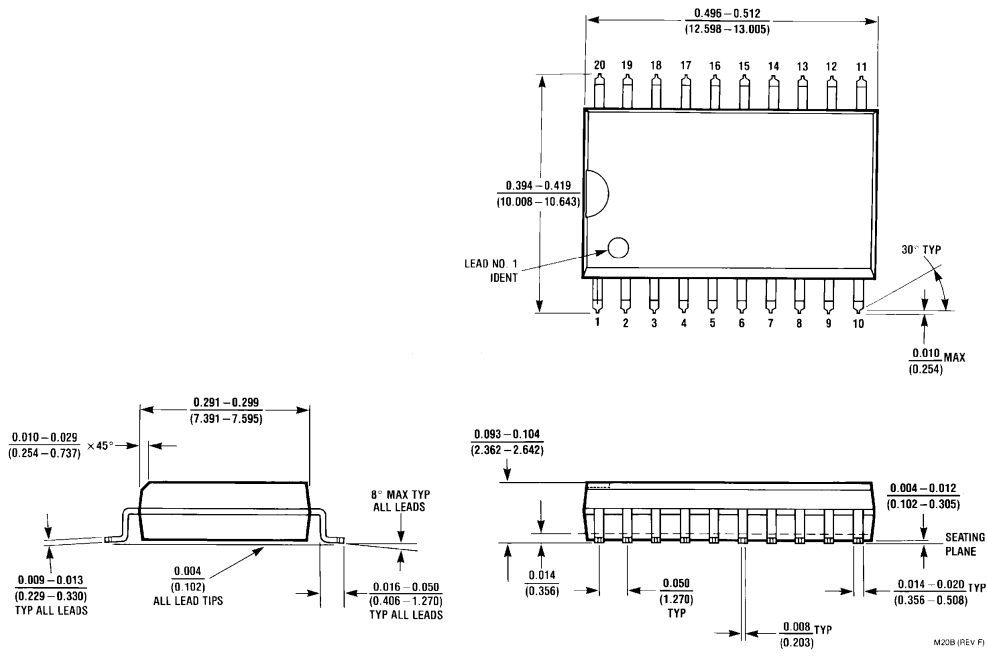
E20A (REV D)



20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A

J20A (REV M)

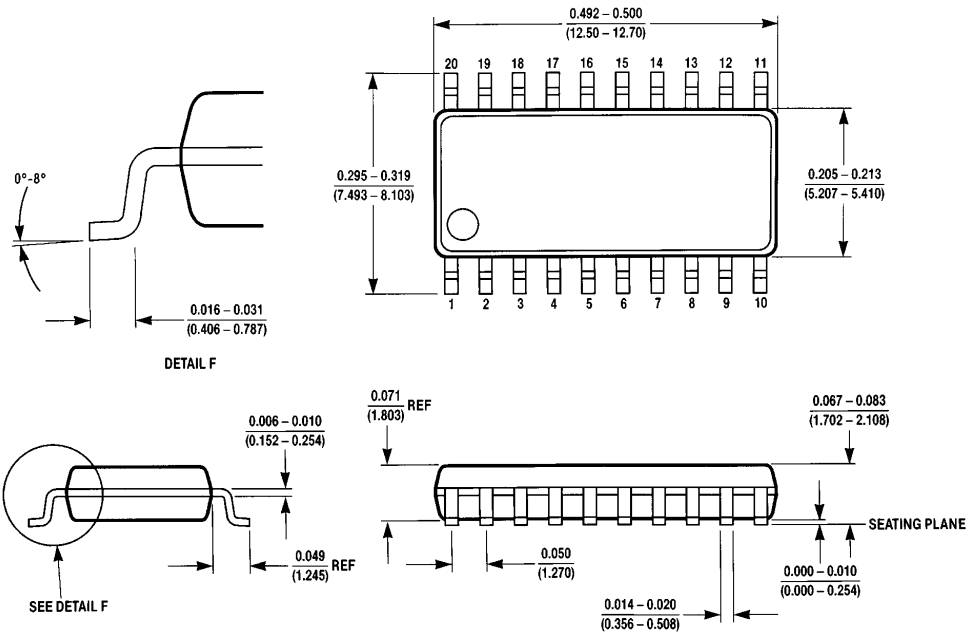
Physical Dimensions inches (millimeters) (Continued)



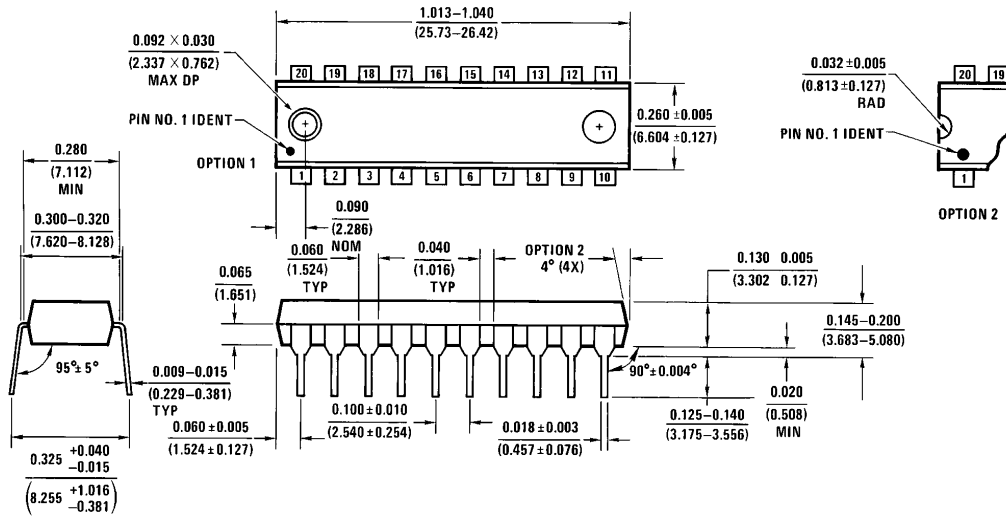
**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B**

M20B (REV F)

Physical Dimensions inches (millimeters) (Continued)



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M200**



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A**

Physical Dimensions inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

W20A (REV E)

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