National Semiconductor

November 1994

54F/74F251A
8-Input Multiplexer with TRI-STATE® Outputs

General Description

The 'F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

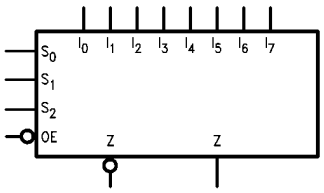
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting TRI-STATE outputs

Commercial	Military	Package Number	Package Description
74F251APC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F251ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F251ASC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F251ASJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F251AFM (Note 2)	W16A	16-Lead Cerpack
	54F251ALL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



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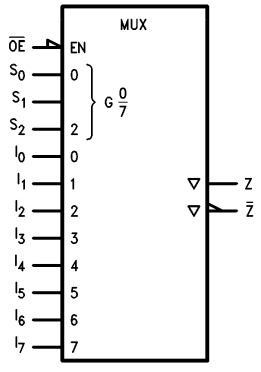
IEEE/IEC



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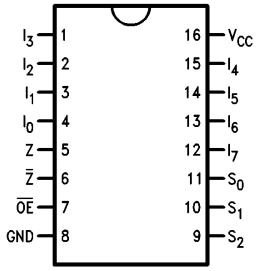
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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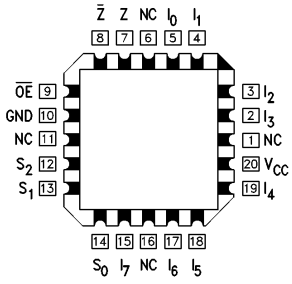
Pin Assignment for LCC



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RRD-B30M75/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0-S_2	Select Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
I_0-I_7	Multiplexer Inputs	1.0/1.0	20 μA/−0.6 mA
Z	TRI-STATE Multiplexer Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output	150/40 (33.3)	−3 mA/24 mA (20 mA)

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE}\bullet(I_0\bullet\overline{S}_0\bullet\overline{S}_1\bullet\overline{S}_2 + I_1\bullet S_0\bullet\overline{S}_1\bullet\overline{S}_2 + I_2\bullet\overline{S}_0\bullet S_1\bullet\overline{S}_2 + I_3\bullet S_0\bullet S_1\bullet\overline{S}_2 + I_4\bullet\overline{S}_0\bullet\overline{S}_1\bullet S_2 + I_5\bullet S_0\bullet\overline{S}_1\bullet S_2 + I_6\bullet\overline{S}_0\bullet S_1\bullet S_2 + I_7\bullet S_0\bullet S_1\bullet S_2)$$

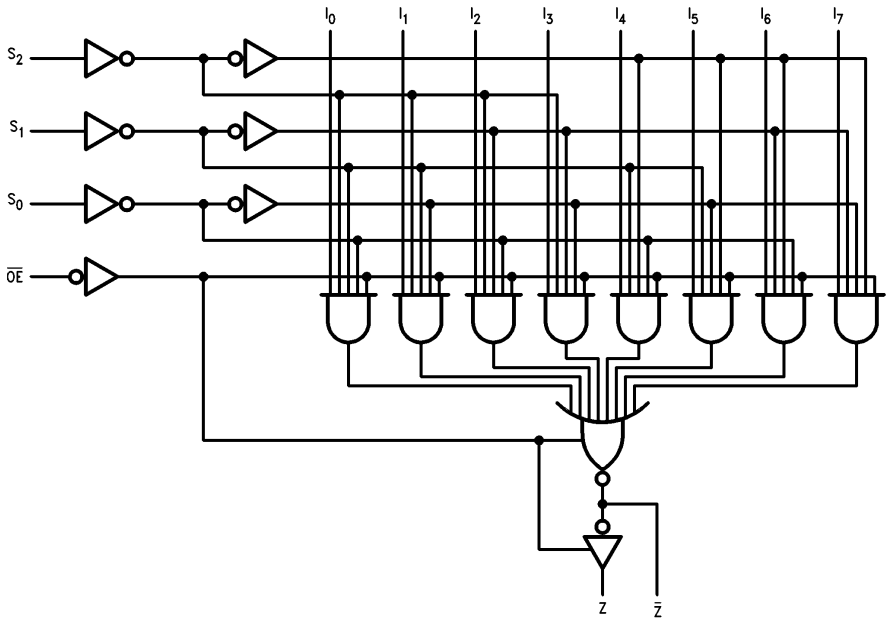
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCL}	Power Supply Current			15	22	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			16	24	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	3.5 3.2	6.0 5.0	9.0 7.5	3.5 3.2	11.5 8.0	3.5 3.2	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to Z	4.5 4.0	7.5 6.0	10.5 8.5	3.5 3.0	14.0 10.5	4.5 4.0	12.5 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	3.0 1.5	5.0 2.5	6.5 4.0	2.5 1.5	8.0 6.0	3.0 1.5	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	3.5 3.5	5.0 5.5	7.0 7.0	2.5 3.5	9.0 9.0	2.5 3.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$	2.5 2.5	4.3 4.3	6.0 6.0	2.0 2.5	7.0 7.5	2.5 2.5	7.0 6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{Z}$	2.5 1.5	4.0 3.0	5.5 4.5	2.5 1.5	6.0 5.0	2.5 1.5	6.0 4.5	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z	3.5 3.5	5.0 5.5	7.0 7.5	3.0 3.5	8.5 9.0	3.0 3.5	7.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z	2.0 1.5	3.8 3.0	5.5 4.5	2.0 1.5	5.5 5.5	2.0 1.5	5.5 4.5	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 251A S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

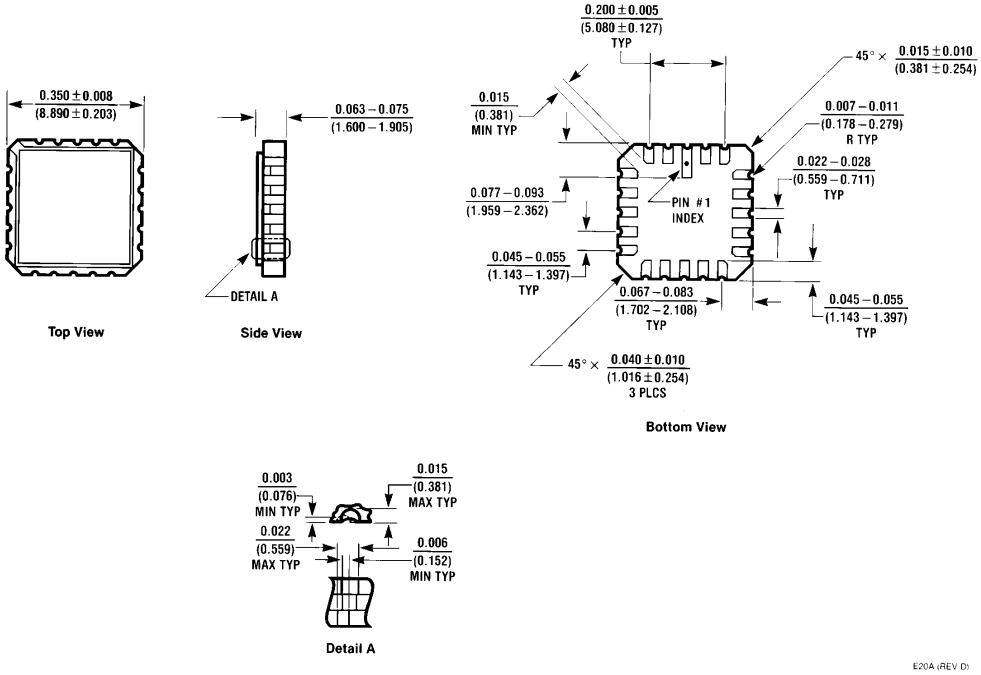
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier (LCC)
- S = Small Outline SOIC JEDEC
- SJ = Small Outline SOIC EIAJ

Special Variations
- QB = Military grade device with environmental and burn-in processing
- X = Devices shipped in 13″ reel

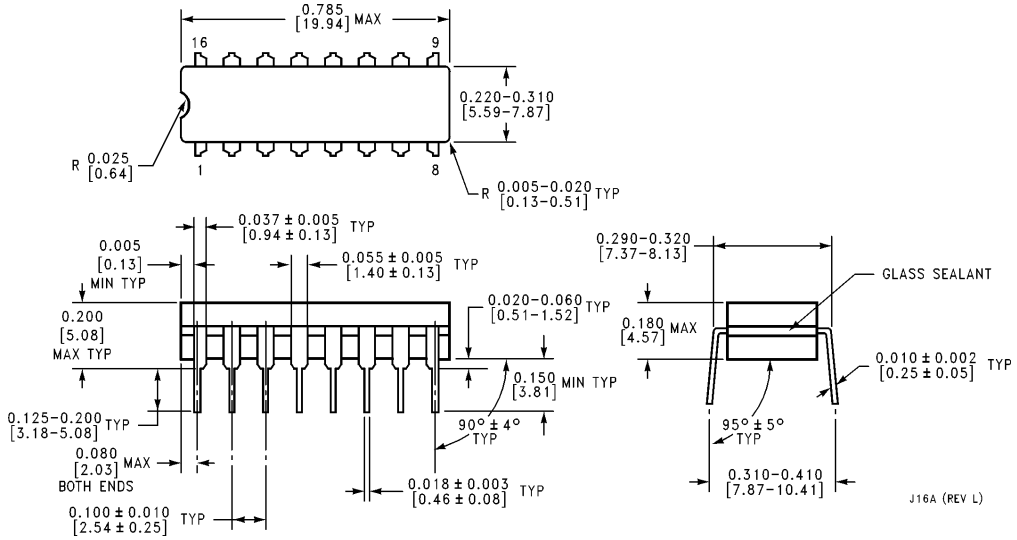
Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

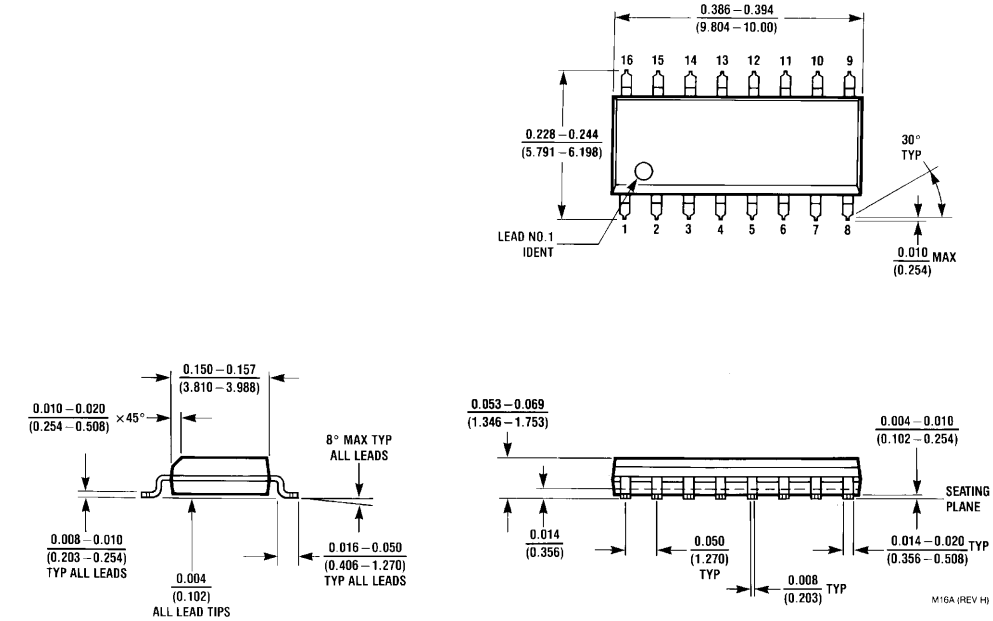


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

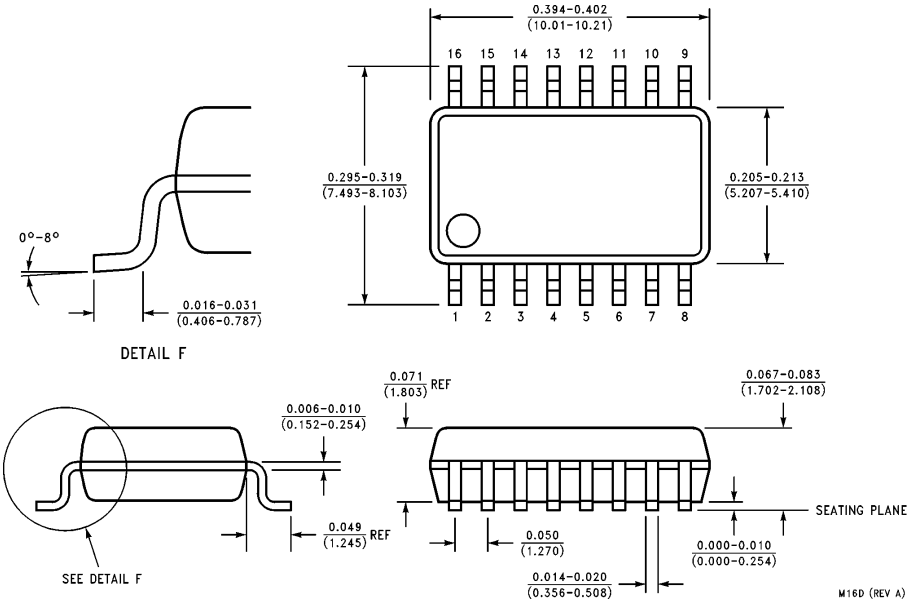


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

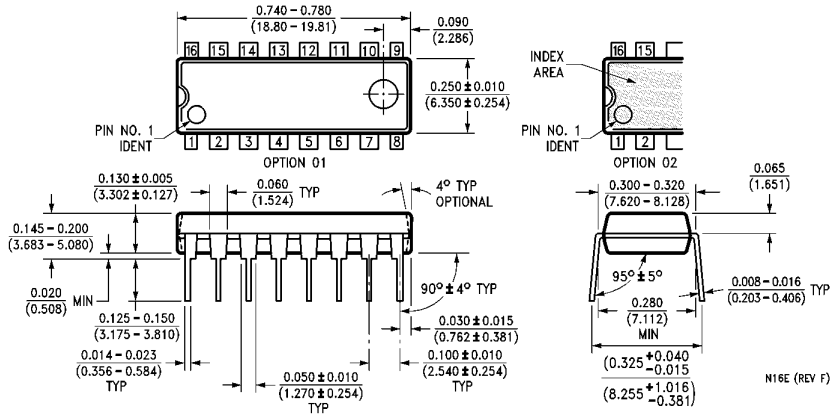


16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

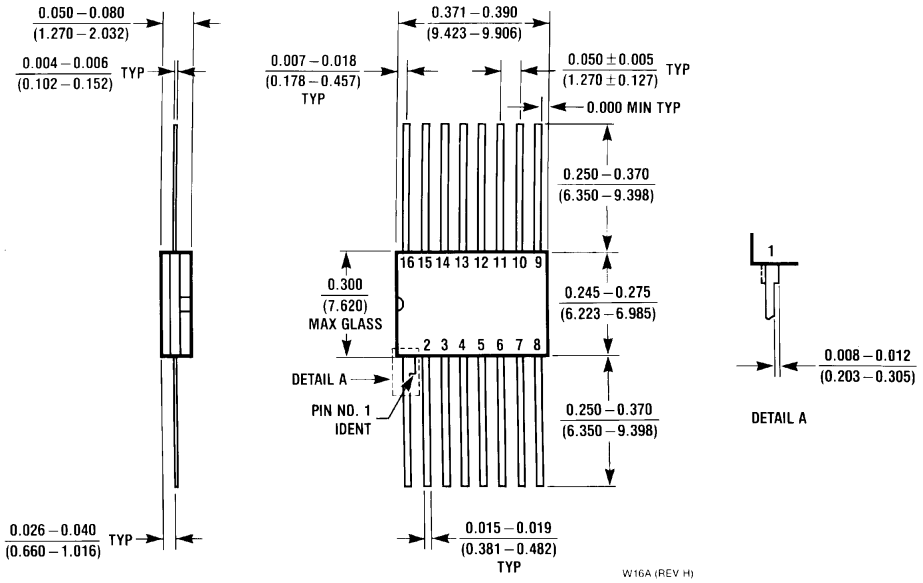


16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D



16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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