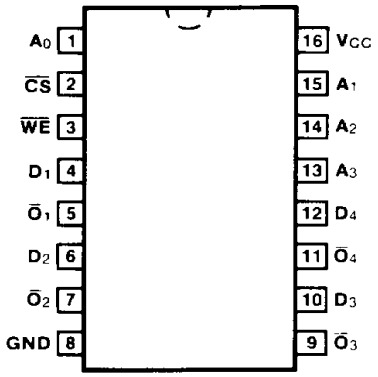
54S/74S289
54LS/74LS289

64-BIT RANDOM ACCESS MEMORY
(With Open-Collector Outputs)

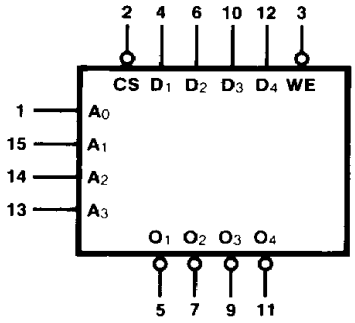
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '289 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74S289PC, 74LS289PC		9B
Ceramic DIP (D)	A	74S289DC, 74LS289DC	54S289DM, 54LS289DM	6B
Flatpak (F)	A	74S289FC, 74LS289FC	54S289FM, 54LS289FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.63/0.16	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
$D_1 - D_4$	Data Inputs	0.63/0.16	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/10	OC*/10 (5.0)

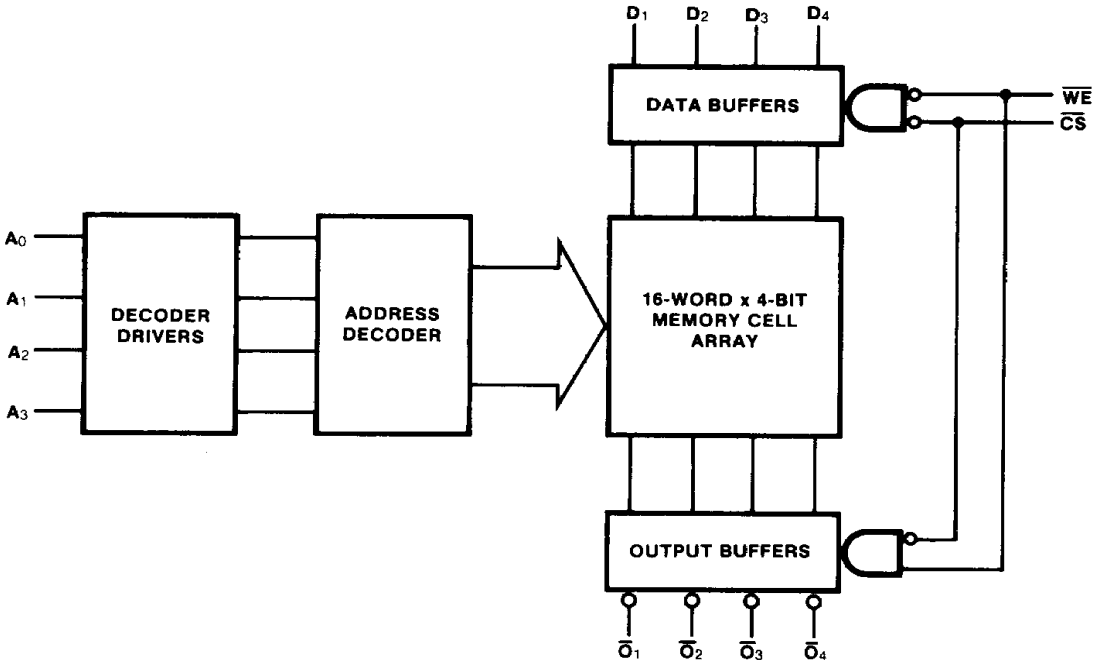
*OC — Open Collector

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	XM		0.5		0.4	V	V_{CC} = Min, I_{OL} = 16 mA ('S289), I_{OL} = 8.0 mA (54LS289), I_{OL} = 16 mA (74LS289)
		XC		0.45		0.5		
I_{OH}	Output HIGH Current			40		20	μA	V_{OH} = 2.4 V, V_{CC} = Min
				100		100		V_{OH} = 5.5 V, V_{CC} = Min
I_{CC}	Power Supply Current			105		40	mA	V_{CC} = Max

AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S C_L = 30 pF, R_L = * Min	54/74S Max	54/74LS C_L = 15 pF, R_L = 2 kΩ Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Access Time, HIGH or LOW, A_n to $\overline{O}_n$	XM		50		37**	ns	Figs. 3-2, 3-20
		XC		35		37**		
t_{PHL}	Access Time $\overline{CS}$ to $\overline{O}_n$	XM		25		10**	ns	Figs. 3-2, 3-5
		XC		17		10**		
t_{PLH}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM		20			ns	
		XC		17				
t_{PHL}	Recovery Time $\overline{WE}$ to $\overline{O}_n$	XM		40		30**	ns	Figs. 3-2, 3-4
		XC		35		30**		
t_{PLH}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM		30			ns	
		XC		25				

AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0		10**		ns	Fig. 3-21
		0		10**			
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0		0**		ns	
		0		0**			
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	20		25**		ns	Fig. 3-13
		20		25**			
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to WE	0		0*		ns	
		0		0*			
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-13
t_w (L)	$\overline{WE}$ Pulse Width LOW	20		25**		ns	Fig. 3-14

*R_L = 300 Ω to V_{CC} and 600 Ω to Gnd.
**Typical Value