119-Bump BGA
Commercial Temp
Industrial Temp

8Mb Pipelined and Flow Through Synchronous NBT SRAMs

100 MHz–66 MHz
3.3 V V_{DD}
2.5 V and 3.3 V V_{DDQ}

Features

- 512K x 18 and 256K x 36 configurations
- User-configurable Pipelined and Flow Through mode
- NBT (No Bus Turn Around) functionality allows zero wait
- Read-Write-Read bus utilization
- Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- IEEE 1149.1 JTAG-compatible Boundary Scan
- On-chip write parity checking; even or odd selectable
- ZQ mode pin for user selectable high/low output drive strength.
- x16/x32 mode with on-chip parity encoding and error detection
- Pin-compatible with 2M, 4M and 16M devices
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- LBO pin for Linear or Interleave Burst mode
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- Clock Control, registered, address, data, and control
- ZZ Pin for automatic power-down
- JEDEC-standard 119-Bump BGA package

		-11	-100	-80	-66
Pipeline 3-1-1-1	t_{Cycle}	10 ns	10 ns	12.5 ns	15 ns
	t_{KQ}	4.5 ns	4.5 ns	4.8 ns	5 ns
	I_{DD}	210 mA	210 mA	190 mA	170 mA
Flow Through 2-1-1-1	t_{KQ}	11 ns	12 ns	14 ns	18 ns
	t_{Cycle}	15 ns	15 ns	15 ns	20 ns
	I_{DD}	150 mA	150 mA	130 mA	130 mA

Functional Description

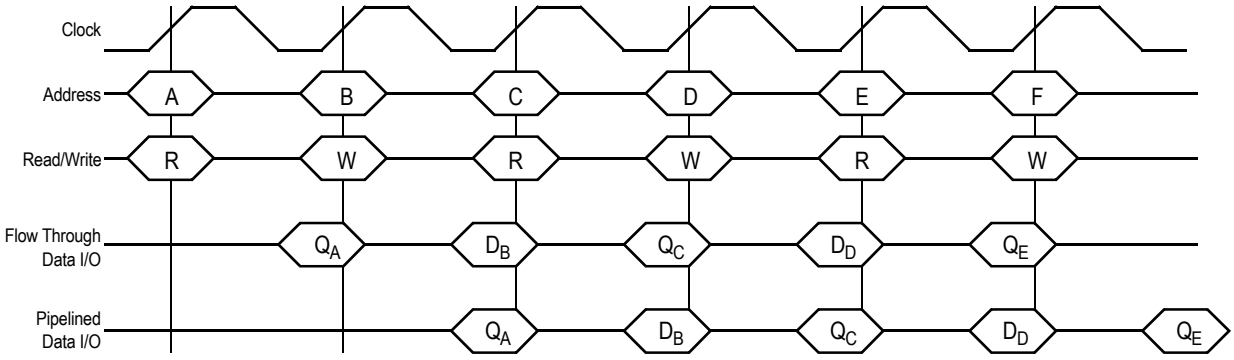
The GS882Z818/36B is an 8Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control (LBO) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

The GS882Z818/36B may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, in addition to the rising-edge-triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge-triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS882Z818/36B is implemented with GSI's high performance CMOS technology and is available in a JEDEC-Standard 119-bump BGA package.

Flow Through and Pipelined NBT SRAM Back-to-Back Read/Write Cycles



GS882Z36 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_7	NC	A_8	A_9	V_{DDQ}
B	NC	E_2	A_4	ADV	A_{15}	$\overline{E}_3$	NC
C	NC	A_5	A_3	V_{DD}	A_{14}	A_{16}	NC
D	DQ_{C4}	DQ_{PC9}	V_{SS}	ZQ	V_{SS}	DQ_{PB9}	DQ_{B4}
E	DQ_{C3}	DQ_{C8}	V_{SS}	$\overline{E}_1$	V_{SS}	DQ_{B8}	DQ_{B3}
F	V_{DDQ}	DQ_{C7}	V_{SS}	$\overline{G}$	V_{SS}	DQ_{B7}	V_{DDQ}
G	DQ_{C2}	DQ_{C6}	$\overline{B}_C$	A_{17}	$\overline{B}_B$	DQ_{B6}	DQ_{B2}
H	DQ_{C1}	DQ_{C5}	V_{SS}	$\overline{W}$	V_{SS}	DQ_{B5}	DQ_{B1}
J	V_{DDQ}	V_{DD}	DP	V_{DD}	$\overline{QE}$	V_{DD}	V_{DDQ}
K	DQ_{D1}	DQ_{D5}	V_{SS}	CK	V_{SS}	DQ_{A5}	DQ_{A1}
L	DQ_{D2}	DQ_{D6}	$\overline{B}_D$	NC	$\overline{B}_A$	DQ_{A6}	DQ_{A2}
M	V_{DDQ}	DQ_{D7}	V_{SS}	$\overline{CKE}$	V_{SS}	DQ_{A7}	V_{DDQ}
N	DQ_{D3}	DQ_{D8}	V_{SS}	A_1	V_{SS}	DQ_{A8}	DQ_{A3}
P	DQ_{D4}	DQ_{PD9}	V_{SS}	A_0	V_{SS}	DQ_{PA9}	DQ_{A4}
R	NC	A_2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A_{13}	$\overline{PE}$
T	NC	NC	A_{10}	A_{11}	A_{12}	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

GS882Z18 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_7	NC	A_8	A_9	V_{DDQ}
B	NC	E_2	A_4	ADV	A_{15}	$\overline{E}_3$	NC
C	NC	A_5	A_3	V_{DD}	A_{14}	A_{16}	NC
D	DQ_{B1}	NC	V_{SS}	ZQ	V_{SS}	DQ_{A9}	NC
E	NC	DQ_{B2}	V_{SS}	$\overline{E}_1$	V_{SS}	NC	DQ_{A8}
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_{A7}	V_{DDQ}
G	NC	DQ_{B3}	$\overline{B}_B$	A_{17}	NC	NC	DQ_{A6}
H	DQ_{B4}	NC	V_{SS}	$\overline{W}$	V_{SS}	DQ_{A5}	NC
J	V_{DDQ}	V_{DD}	DP	V_{DD}	$\overline{QE}$	V_{DD}	V_{DDQ}
K	NC	DQ_{B5}	V_{SS}	CK	V_{SS}	NC	DQ_{A4}
L	DQ_{B6}	NC	NC	NC	$\overline{B}_A$	DQ_{A3}	NC
M	V_{DDQ}	DQ_{B7}	V_{SS}	$\overline{CKE}$	V_{SS}	NC	V_{DDQ}
N	DQ_{B8}	NC	V_{SS}	A_1	V_{SS}	DQ_{A2}	NC
P	NC	DQ_{B9}	V_{SS}	A_0	V_{SS}	NC	DQ_{A1}
R	NC	A_2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A_{13}	$\overline{PE}$
T	NC	A_{10}	A_{11}	NC	A_{12}	A_{18}	ZZ
U	V_{DDQ}					NC	V_{DDQ}

GS882Z18/36 BGA Pin Description

Pin Location	Symbol	Type	Description
P4, N4	A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A2, A3, A5, A6, B3, B5, C2, C3, C5, C6, G4, R2, R6, T3, T5	An	I	Address Inputs
T4	An	I	Address Inputs (x36 Version)
T2, T6	NC	—	No Connect (x36 Version)
T2, T6	An	I	Address Inputs (x18 Version)
K7, L7, N7, P7, K6, L6, M6, N6, P6 H7, G7, E7, D7, H6, G6, F6, E6, D6 H1, G1, E1, D1, H2, G2, F2, E2, D2 K1, L1, N1, P1, K2, L2, M2, N2, P2	DQ_{A1}–DQ_{PA9} DQ_{B1}–DQ_{PB9} DQ_{C1}–DQ_{PC9} DQ_{D1}–DQ_{PD9}	I/O	Data Input and Output pins (x36 Version)
L5, G5, G3, L3	$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low (x36 Version)
P7, N6, L6, K7, H6, G7, F6, E7, D6 D1, E2, G2, H1, K2, L1, M2, N1, P2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
L5, G3	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low (x18 Version)
P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3, T4	NC	—	No Connect (x18 Version)
K4	CK	I	Clock Input Signal; active high
M4	$\overline{CKE}$	I	Clock Input Buffer Enable; active low
H4	$\overline{W}$	I	Write Enable—Writes all enabled bytes; active low
E4	$\overline{E}_1$	I	Chip Enable; active low
B2	E_2	I	Chip Enable; active high
B6	$\overline{E}_3$	I	Chip Enable; active low
F4	$\overline{G}$	I	Output Enable; active low
B4	ADV	I	Burst address counter advance enable; active high
T7	ZZ	I	Sleep Mode control; active high
R5	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
R3	$\overline{LBO}$	I	Linear Burst Order mode; active low
R7	$\overline{PE}$	I	Parity Bit Enable; active low (High = x16/32 Mode, Low = x18/36 Mode)
J3	DP	I	Data Parity Mode Input; 1 = Even, 0 = Odd
J5	$\overline{QE}$	O	Parity Error Out; Open Drain Output
D4	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
B1, C1, R1, T1, L4, B7, C7, U6	NC	—	No Connect

GS882Z18/36 BGA Pin Description

Pin Location	Symbol	Type	Description
U2	TMS	I	Scan Test Mode Select
U3	TDI	I	Scan Test Data In
U5	TDO	O	Scan Test Data Out
U4	TCK	I	Scan Test Clock
J2, C4, J4, R4, J6	V_{DD}	I	Core power supply
D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5	V_{SS}	I	I/O and Core Ground
A1, F1, J1, M1, U1, A7, F7, J7, M7, U7	V_{DDQ}	I	Output driver power supply

BPR2000.002.14

Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{CKE}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/$\overline{Load}$ pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2, and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte “a”	L	L	H	H	H
Write Byte “b”	L	H	L	H	H
Write Byte “c”	L	H	H	L	H
Write Byte “d”	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{CKE}$ is asserted Low, all three chip enables ($\overline{E1}$, E2, and $\overline{E3}$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the Output pins.

Write operation occurs when the RAM is selected, CKE is active and the Write input is sampled low at the rising edge of clock.

The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A Write Cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

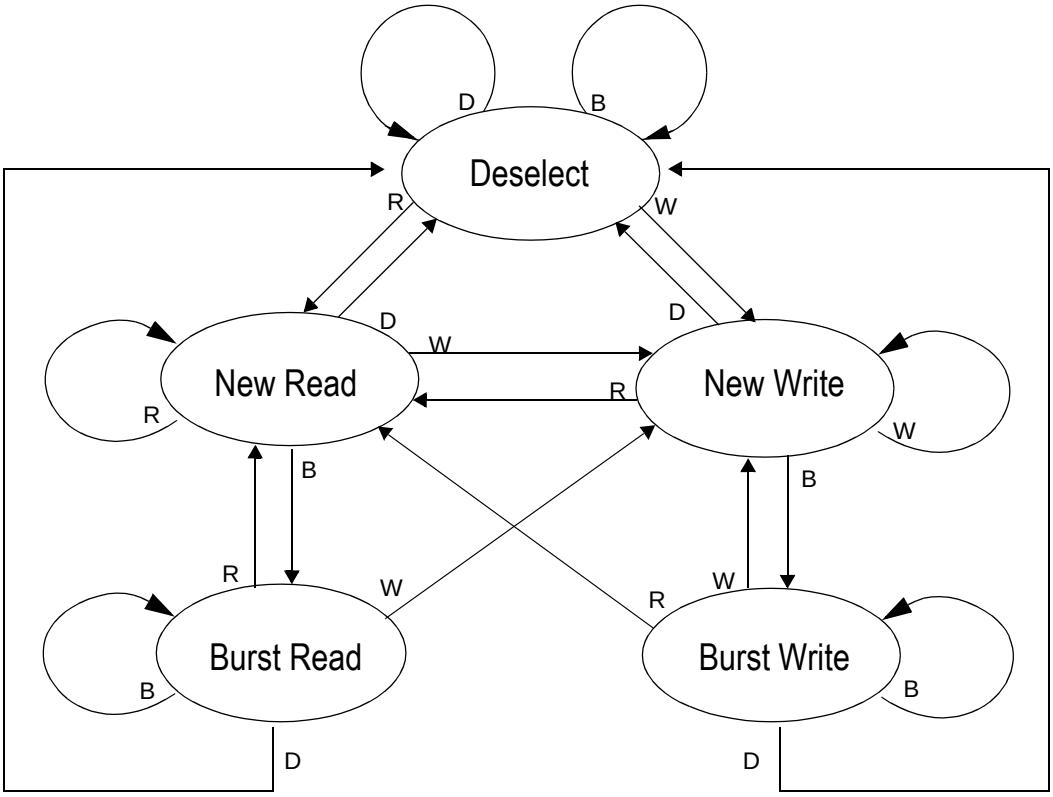
Write operations are initiated in the same way as well, but differ in that the write pipeline is one cycle shorter, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

Synchronous Truth Table

Operation	Type	Address	$\overline{E}_1$	E_2	$\overline{E}_3$	ZZ	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{G}$	$\overline{CKE}$	CK	DQ	Notes
Deselect Cycle, Power Down	D	None	H	X	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	X	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	D	None	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
Read Cycle, Begin Burst	R	External	L	H	L	L	L	H	X	L	L	L-H	Q	
Read Cycle, Continue Burst	B	Next	X	X	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/Read, Begin Burst	R	External	L	H	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy Read, Continue Burst	B	Next	X	X	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L	H	L	L	L	L	L	X	L	L-H	D	3
Write Cycle, Continue Burst	B	Next	X	X	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/Write Abort, Begin Burst	W	None	L	H	L	L	L	L	H	X	L	L-H	High-Z	2,3
Write Abort, Continue Burst	B	Next	X	X	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ignore, Stall		Current	X	X	X	L	X	X	X	X	H	L-H	-	4
Sleep Mode		None	X	X	X	H	X	X	X	X	X	X	High-Z	

Notes:
1. Continue Burst cycles, whether read or write, use the same control inputs; a Deselect continue cycle can only be entered into if a Deselect cycle is executed first
2. Dummy read and write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active, so no Write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during Write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

Pipeline and Flow Through Read-Write Control State Diagram



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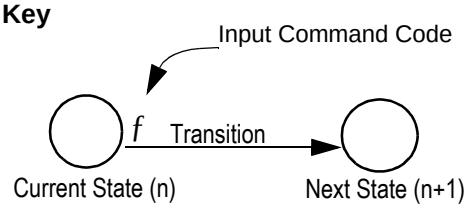
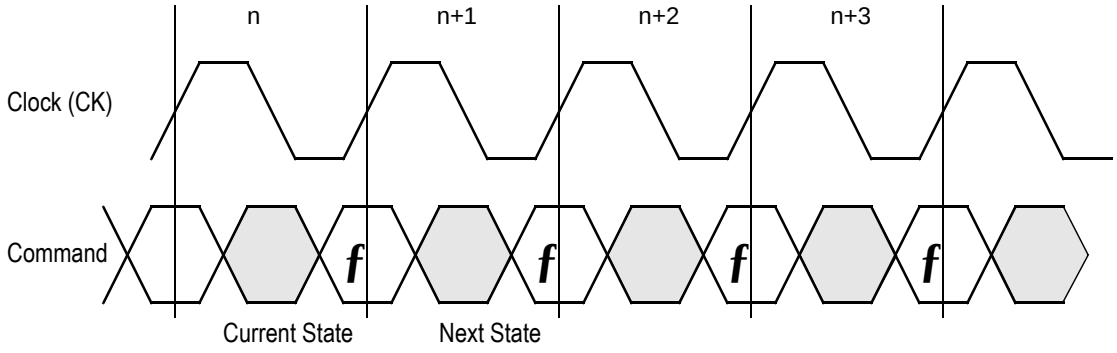


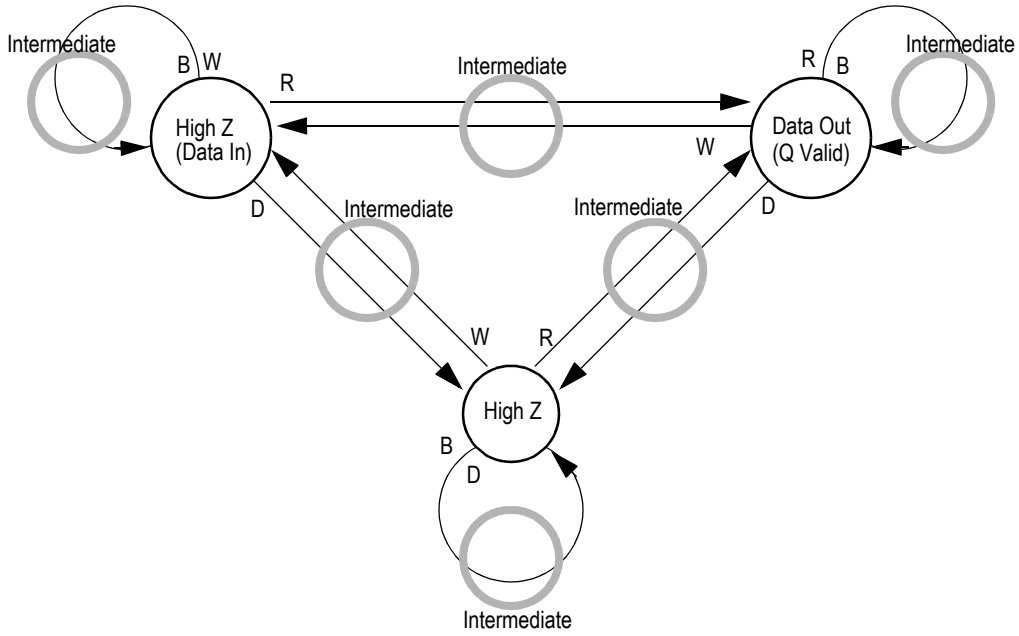
Notes

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B and D represent input command codes, as indicated in the Synchronous Truth Table.



Current State and Next State Definition for Pipelined and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram



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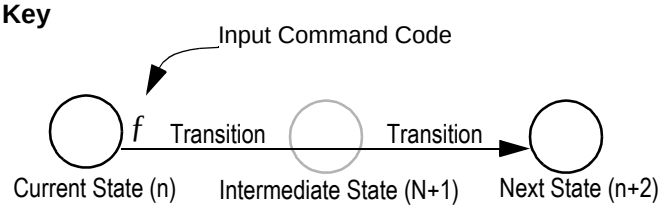

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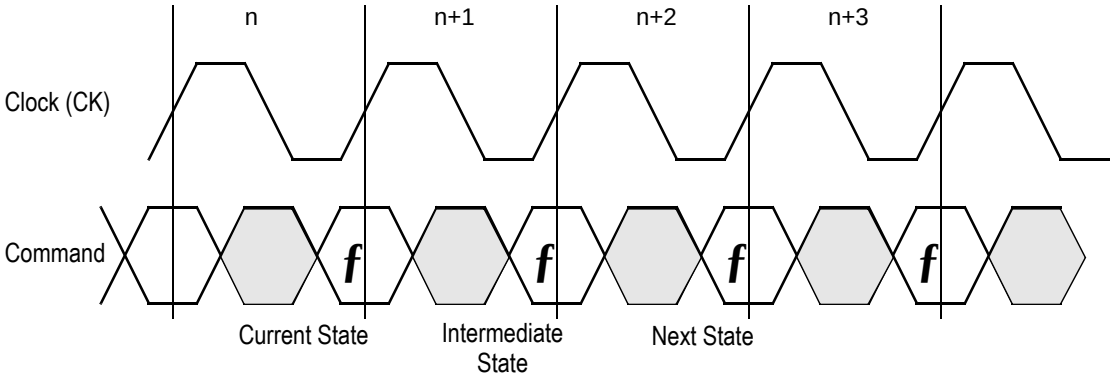
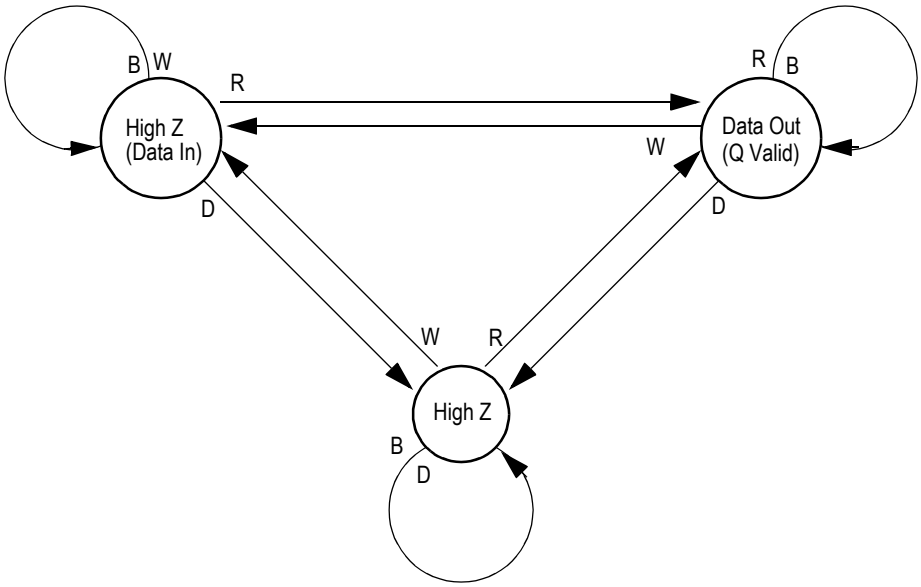


Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram



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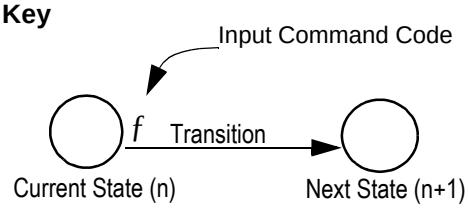

Notes

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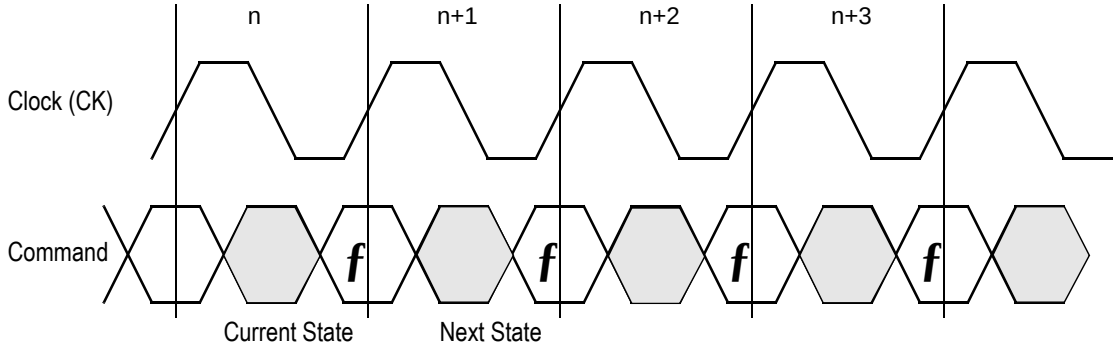


Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{LBO}$). When this pin is Low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

FLXDrive™

The ZQ pin allows selection between NBT RAM nominal drive strength (ZQ low) for multi-drop bus applications and low drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
ByteSafe Data Parity Control	DP	L	Check for Odd Parity
		H or NC	Check for Even Parity
Parity Enable	$\overline{PE}$	L or NC	Activate 9th I/Os (x18/36 Mode)
		H	Deactivate 9th I/Os (x16/32 Mode)
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H	Low Drive (High Impedance)

Note:
There are pull-up devices on the $\overline{LBO}$, ZQ, DP and $\overline{FT}$ pins and a pull down device on the $\overline{PE}$ and ZZ pins, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

Enable / Disable Parity I/O Pins

This SRAM allows the user to configure the device to operate in Parity I/O active (x18 or x36) or in Parity I/O inactive (x16 or x32) mode. Holding the $\overline{PE}$ bump low or letting it float will activate the 9th I/O on each byte of the RAM. Tying $\overline{PE}$ high deactivates the 9th I/O of each byte, although the bit in each byte of the memory array remains active to store and recall parity bits generated and read into the ByteSafe parity circuits.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

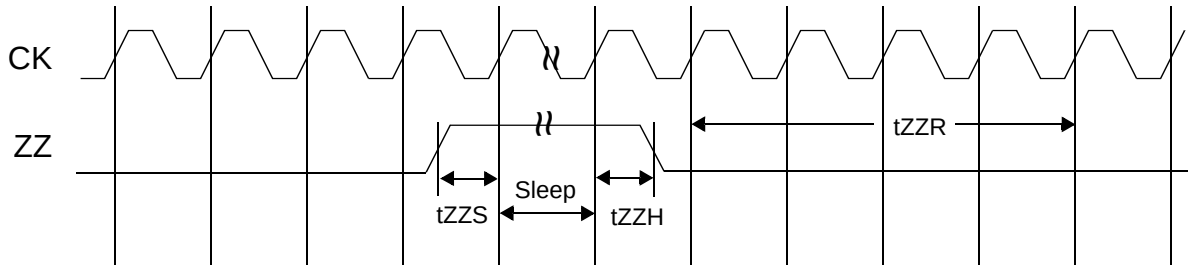
BPR 1999.05.18

Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipeline mode via the $\overline{FT}$ signal found on bump 5R. Not all vendors offer this option, however most mark bump 5R as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

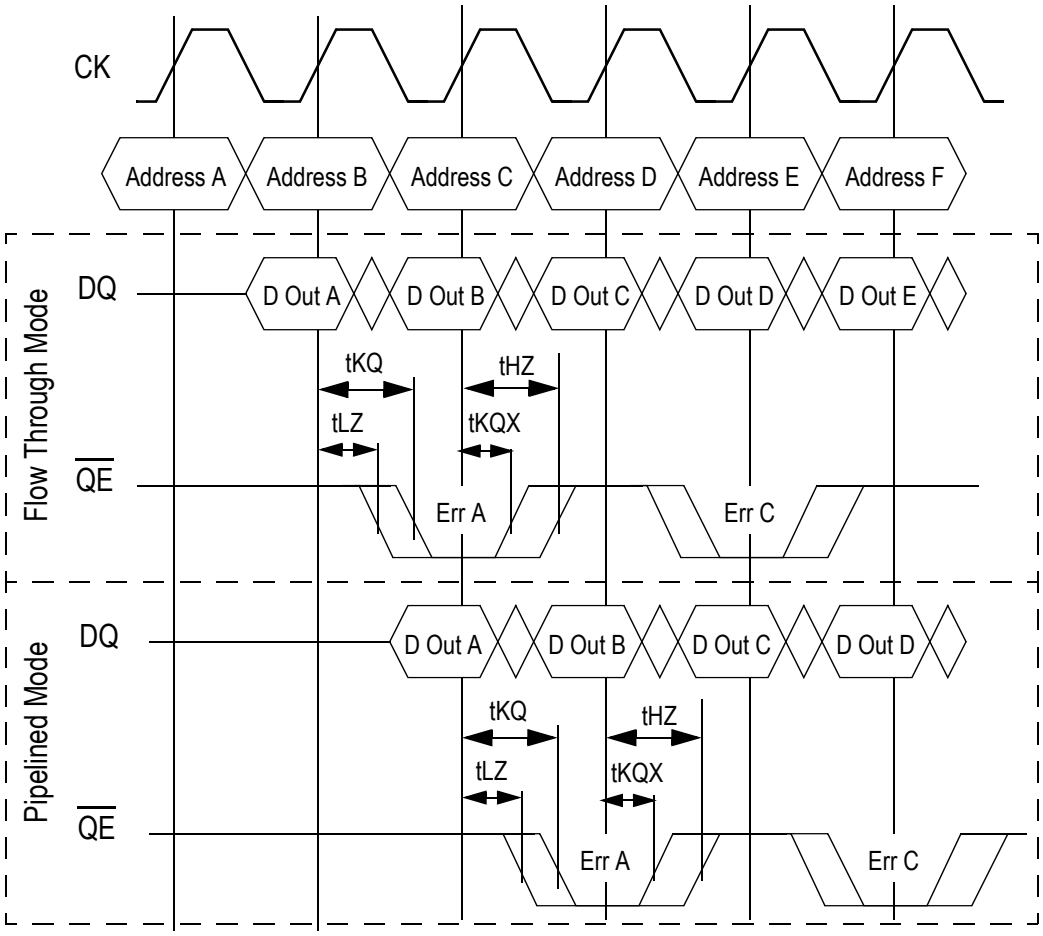
ByteSafe™ Parity Functions

In x32/x16 mode this RAM features a parity encoding and checking function. It is assumed that the RAM is being used in x32/x16 mode because there is no source for parity bits from the system. So, in x32/x16 mode, the device generates parity and stores it along with written data. It is also assumed that there is no facility for parity checking, so the RAM checks read parity and reports an error in the cycle following parity check. In x32/x16 mode the device does not drive the 9th data output, even though the internal ByteSafe parity encoding has been activated. A ByteSafe SRAM, used in x32/x16 mode, allows parity protection of data in applications where parity encoding or checking are not otherwise available. As in any system that checks read parity, reads of un-

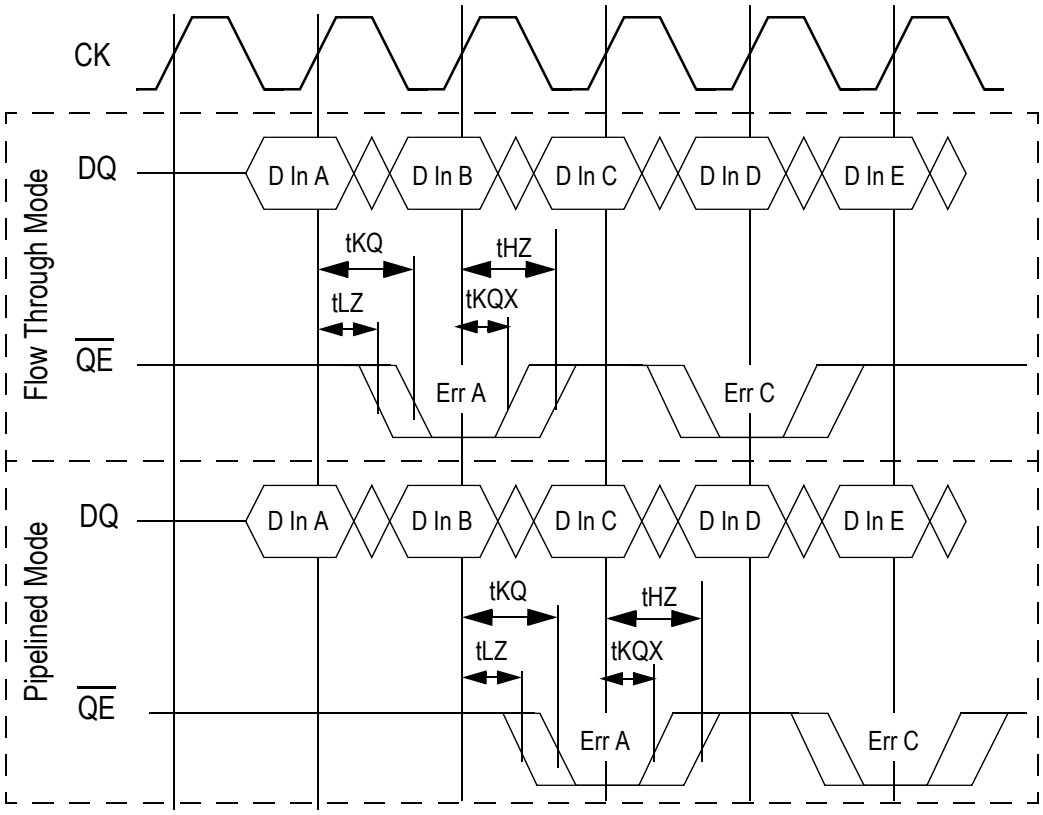
written memory locations may well produce parity errors. Initialization of the memory should be implemented to avoid this issue.

In x18/x36 mode this SRAM includes a write data parity check that checks the validity of data coming into the RAM on write cycles. In Flow Through mode, write data errors are reported in the cycle following the data input cycle. In Pipeline mode, write data errors are reported one clock cycle later. (See **Write Parity Error Output Timing Diagram**.) The Data Parity Mode (DP) pin must be tied high to set the RAM to check for even parity or low to check for odd parity. Read data parity is not checked by the RAM as data. Validity is best established at the data's destination. The Parity Error Output is an open drain output and drives low to indicate a parity error. Multiple Parity Error Output pins may share a common pull-up resistor.

x32 Mode ($\overline{PE}$ = 1) Read Parity Error Output Timing Diagram



x18/x36 Mode ($\overline{PE}$ = 0) Write Parity Error Output Timing Diagram



BPR 1999.05.18

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

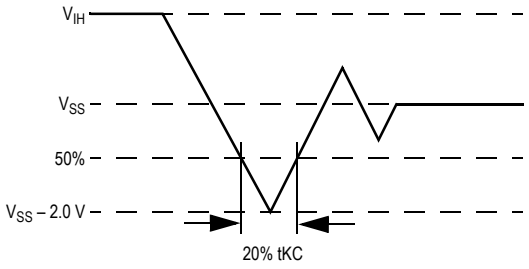
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

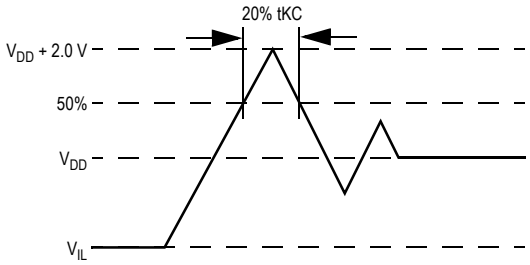
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	3

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ V_{DDQ} ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ V_{DDQ} ≤ 3.135 V (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

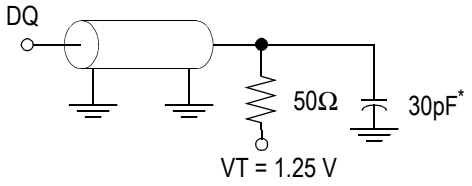
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

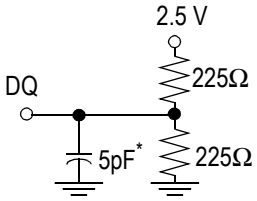
Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

Output Load 2



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ V_{IN} ≤ V_{IL}	–300 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

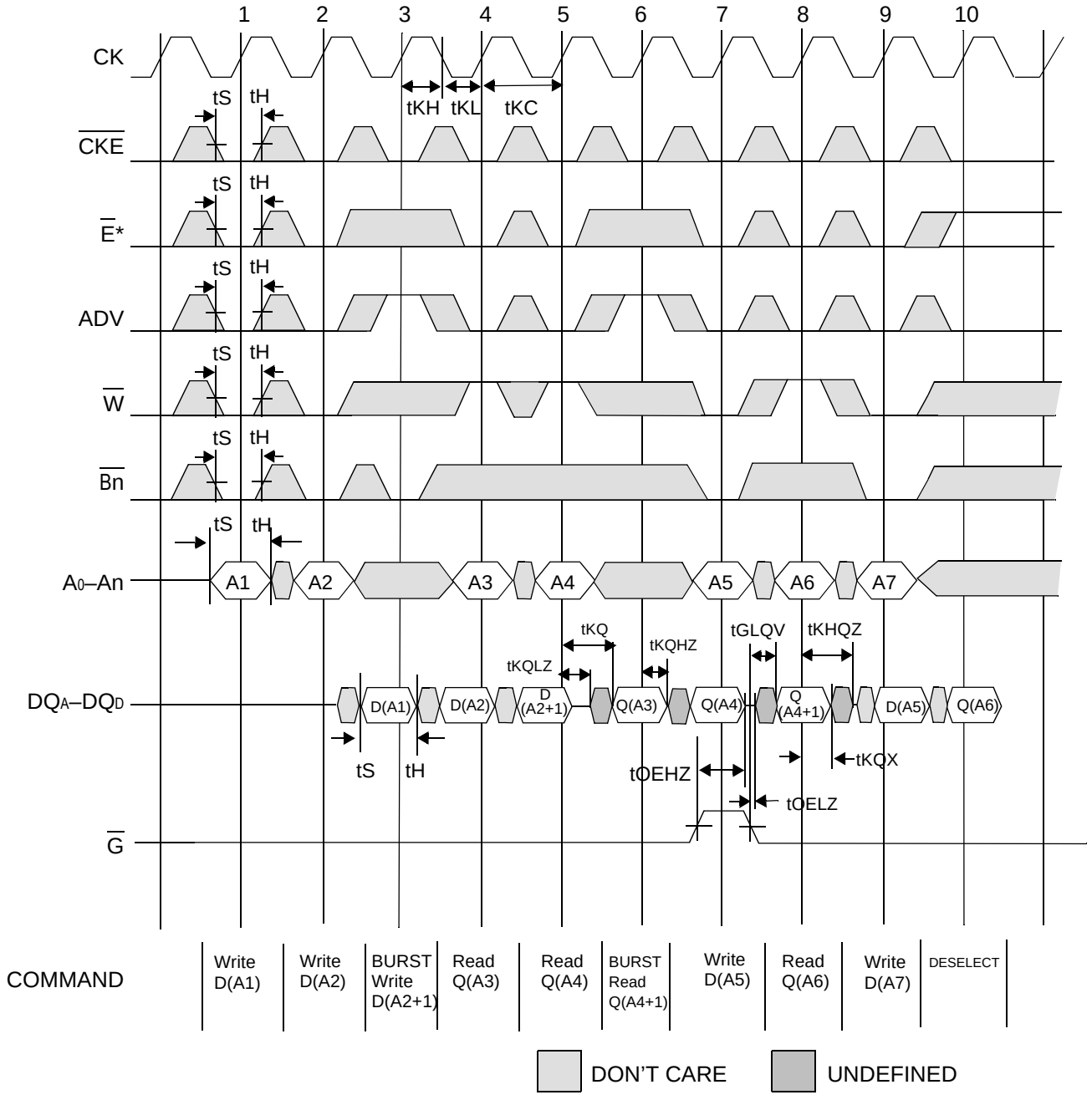
Parameter	Test Conditions	Symbol	-11		-100		-80		-66		Unit
			0 to 70°C	-40 to +85°C	0 to 70°C	-40 to +85°C	0 to 70°C	-40 to +85°C	0 to 70°C	-40 to +85°C	
Operating Current	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL} Output open	I_{DD} Pipeline	210	220	210	220	190	200	170	180	mA
		I_{DD} Flow-through	150	160	150	160	130	140	130	140	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	I_{SB} Pipeline	30	40	30	40	30	40	30	40	mA
		I_{SB} Flow-through	30	40	30	40	30	40	30	40	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	I_{DD} Pipeline	80	90	80	90	70	80	65	75	mA
		I_{DD} Flow-through	65	75	65	75	55	65	55	65	mA

AC Electrical Characteristics

	Parameter	Symbol	-11		-100		-80		-66		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	10	—	10	—	12.5	—	15	—	ns
	Clock to Output Valid	tKQ	—	4.5	—	4.5	—	4.8	—	5	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow-through	Clock Cycle Time	tKC	15.0	—	15.0	—	15.0	—	20	—	ns
	Clock to Output Valid	tKQ	—	11.0	—	12.0	—	14.0	—	18.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.7	—	2	—	2	—	2.3	—	ns
	Clock LOW Time	tKL	2	—	2.2	—	2.2	—	2.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	4.0	1.5	4.5	1.5	4.8	1.5	5	ns
	$\overline{G}$ to Output Valid	tOE	—	4.0	—	4.5	—	4.8	—	5	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	4.0	—	4.5	—	4.8	—	5	ns
	Setup time	tS	1.5	—	2.0	—	—	2.0	—	2.0	ns
	Hold time	tH	0.5	—	0.5	—	—	0.5	—	0.5	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	ns

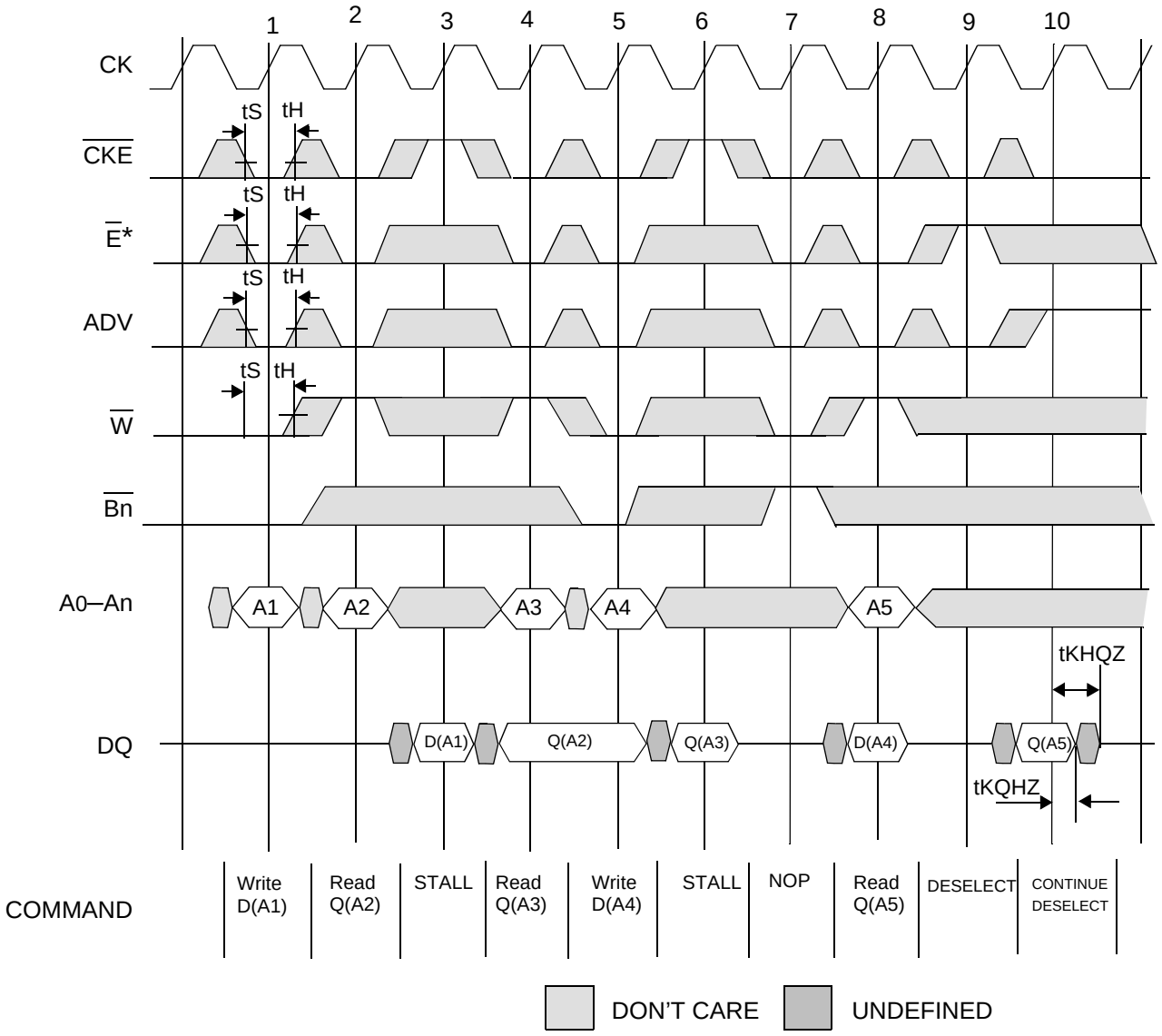
Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Read/Write Cycle Timing



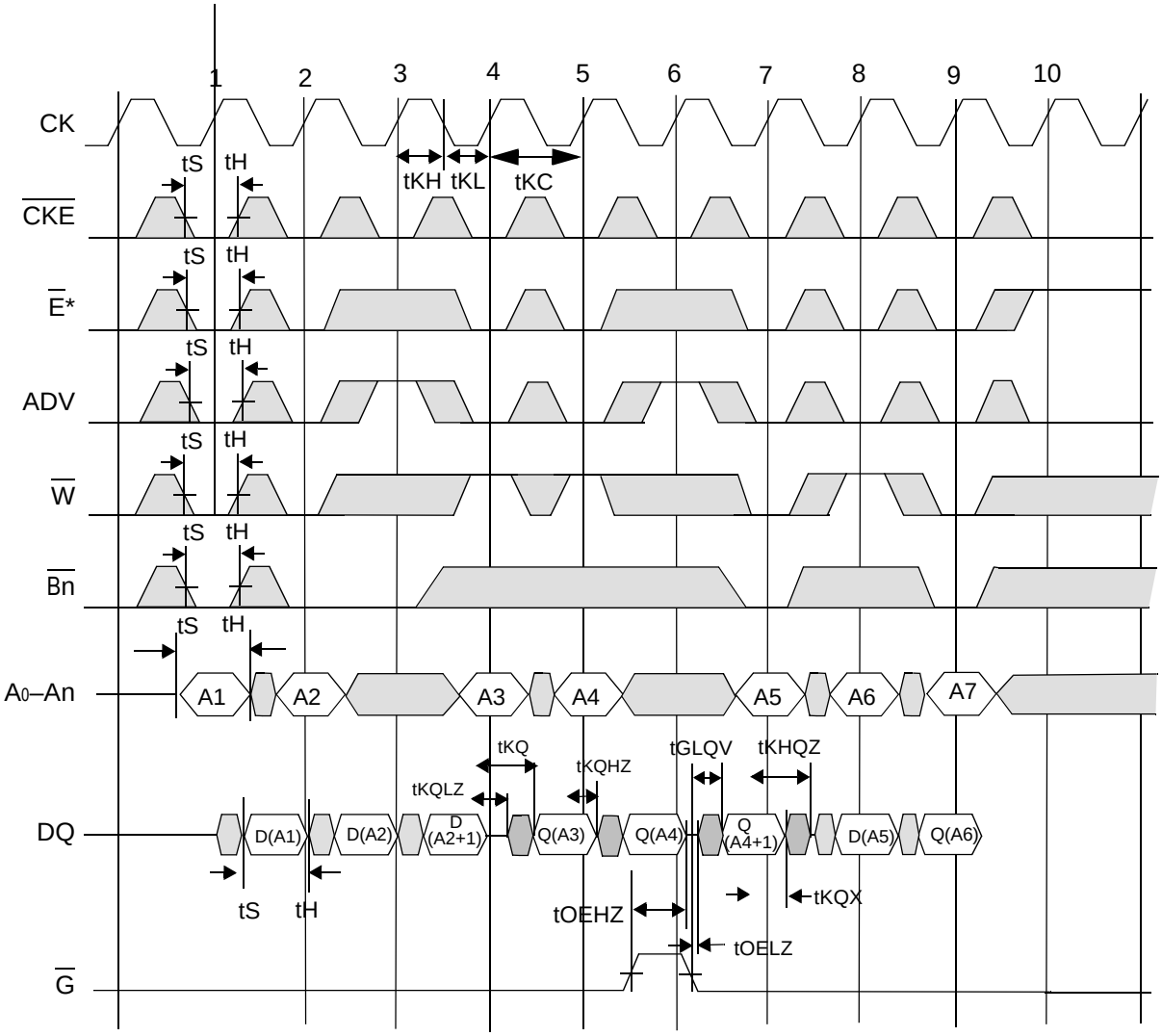
*Note: E = High (False) if E_1 = 1 or E_2 = 0 or E_3 = 1

Pipeline Mode No-Op, Stall and Deselect Timing



*Note: E = High (False) if E_1 = 1 or E_2 = 0 or E_3 = 1

Flow Through Mode Read/Write Cycle Timing

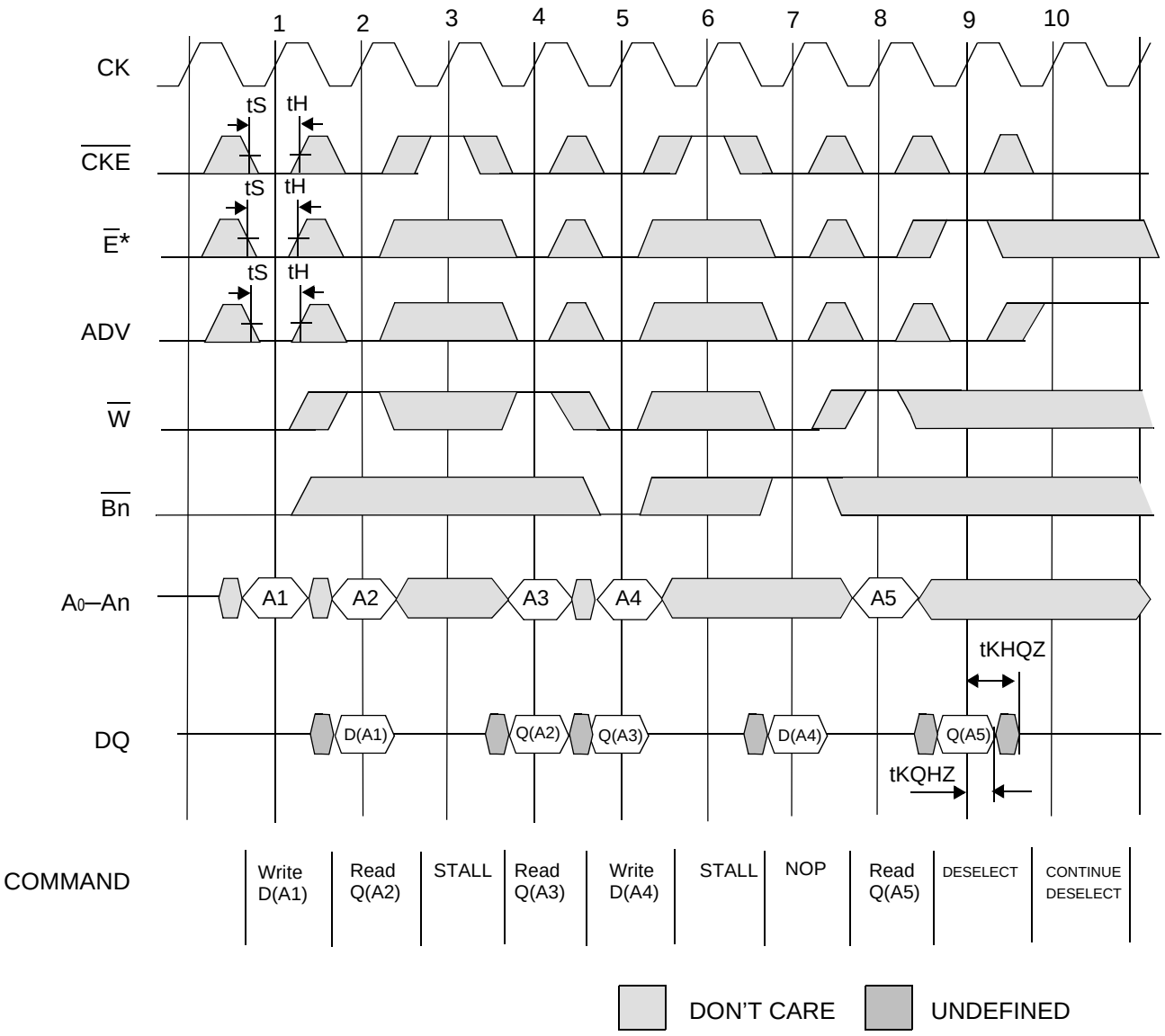


COMMAND	Write D(A1)	Write D(A2)	BURST Write D(A2+1)	Read Q(A3)	Read Q(A4)	BURST Read Q(A4+1)	Write D(A5)	Read Q(A6)	Write D(A7)	DESELECT

DON'T CARE UNDEFINED

*Note: E = High (False) if E_1 = 1 or E_2 = 0 or E_3 = 1

Flow Through Mode No-Op, Stall and Deselect Timing



*Note: E = High (False) if E_1 = 1 or E_2 = 0 or E_3 = 1

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Some functions have been modified or eliminated because they can slow the RAM. Nevertheless, the RAM supports 1149.1-1990 TAP (Test Access Port) Controller architecture, and can be expected to function in a manner that does not conflict with the operation of Standard 1149.1 compliant devices. The JTAG Port interfaces with conventional TTL / CMOS logic level signaling.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

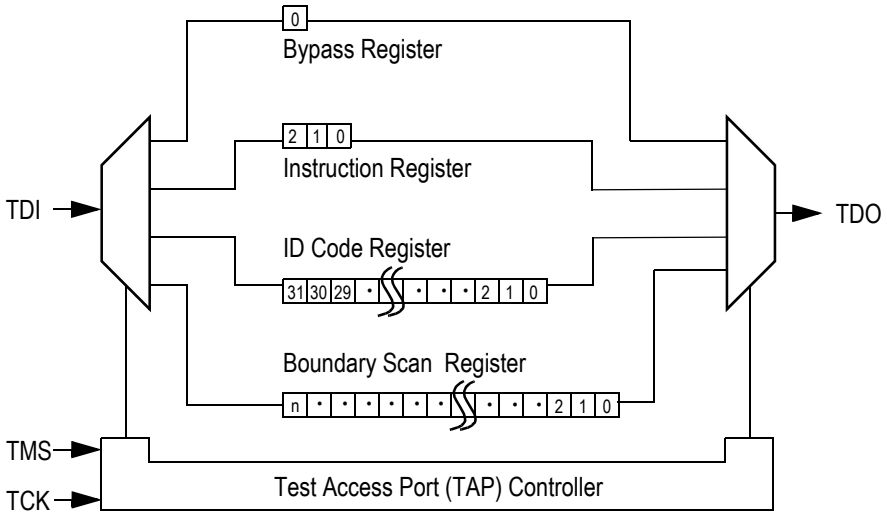
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. Two TAP instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x32	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0	0	1	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1

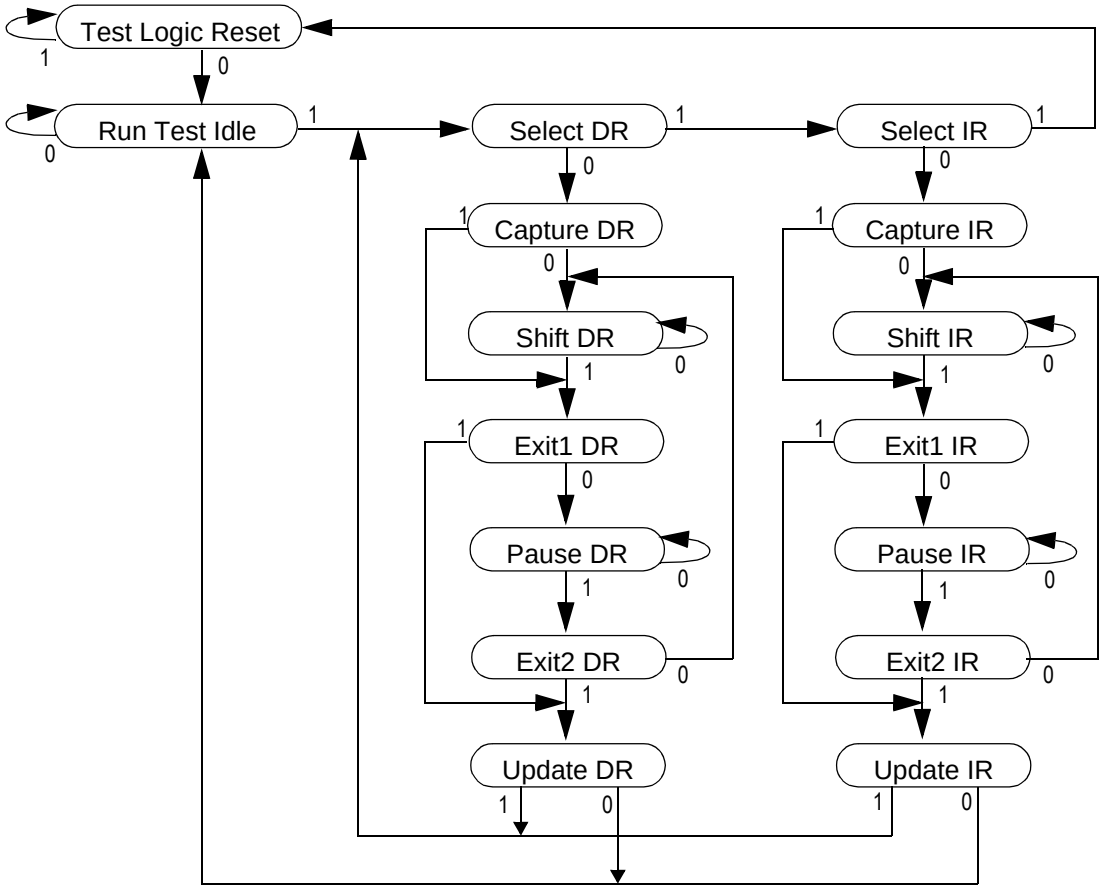
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions, are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but cannot be used to load address, data or control signals into the RAM or to preload the I/O buffers.This device will not perform EXTEST, INTEST or the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE / PRELOAD instruction loaded in the Instruction Register has the same effect as the Pause-DR command. This functionality is not Standard 1149.1-compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore, this device is not 1149.1-compliant. Nevertheless, this RAM's TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the BYPASS instruction described above.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Replicates BYPASS instruction. Places Bypass Register between TDI and TDO. This RAM does not implement 1149.1 EXTEST function. *Not 1149.1 Compliant *	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This RAM does not implement 1149.1 PRELOAD function. *Not 1149.1 Compliant *	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHT}	1.7	V_{DD} +0.3	V	1, 2
Test Port Input Low Voltage	V_{ILT}	–0.3	0.8	V	1, 2
TMS, TCK and TDI Input Leakage Current	I_{INTH}	–300	1	uA	3
TMS, TCK and TDI Input Leakage Current	I_{INTL}	–1	1	uA	4
TDO Output Leakage Current	I_{OLT}	–1	1	uA	5
Test Port Output High Voltage	V_{OHT}	2.4	—	V	6, 7
Test Port Output Low Voltage	V_{OLT}	—	0.4	V	6, 8

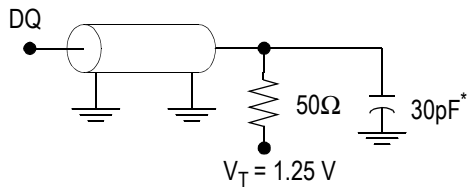
Notes:
1. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tTKC.
3. $V_{DD} \geq V_{IN} \geq V_{IL}$
4. $0\ V \leq V_{IN} \leq V_{IL}$
5. Output Disable, V_{OUT} = 0 to V_{DD}
6. The TDO output driver is served by the V_{DD} supply.
7. I_{OH} = –4 mA
8. I_{OL} = +4 mA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V

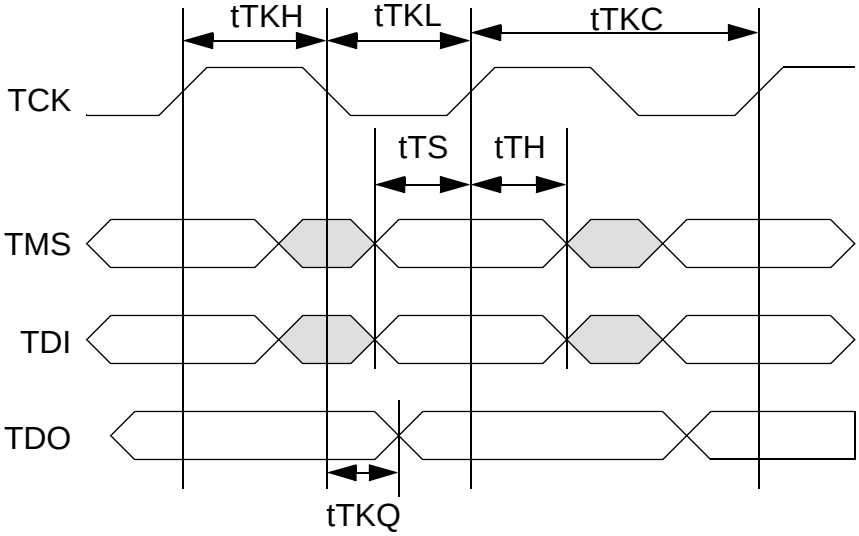
Notes:
1. Include scope and jig capacitance.

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	20	—	ns
TCK Low to TDO Valid	tTKQ	—	10	ns
TCK High Pulse Width	tTKH	10	—	ns
TCK Low Pulse Width	tTKL	10	—	ns
TDI & TMS Set Up Time	tTS	5	—	ns
TDI & TMS Hold Time	tTH	5	—	ns

GS882Z18/36B BGA Boundary Scan Register

Order	x36	x18	Bump x36	Bump x18
1	$\overline{PE}$		7R	
2	PH = 0		n/a	
3	A_{10}		3T	2T
4	A_{11}		4T	3T
5	A_{12}		5T	
6	A_{13}		6R	
7	A_{14}		5C	
8	A_{15}		5B	
9	A_{16}		6C	
10	x36 = DQ_{A9} x32 = NA = 0	NC = 1	6P	
11	DQ_{A8}	NC = 1	7N	
12	DQ_{A4}	NC = 1	6M	
13	DQ_{A3}	NC = 1	7L	
14	DQ_{A7}	NC = 1	6K	
15	DQ_{A6}	DQ_{A1}	7P	
16	DQ_{A5}	DQ_{A2}	6N	
17	DQ_{A2}	DQ_{A3}	6L	
18	DQ_{A1}	DQ_{A4}	7K	
19	$\overline{ZZ}$		7T	
20	$\overline{QE}$		5J	
21	DQ_{B5}	DQ_{A5}	6H	
22	DQ_{B1}	DQ_{A6}	7G	
23	DQ_{B2}	DQ_{A7}	6F	
24	DQ_{B6}	DQ_{A8}	7E	
25	DQ_{B3}	x18 =DQ_{A9} x16 = NA = 0	7H	6D
26	DQ_{B4}	NC = 1	6G	
27	DQ_{B7}	NC = 1	6E	
28	DQ_{B8}	NC = 1	7D	
29	x36 = DQ_{B9} x32 = NA = 0	A_{18}	6D	6T

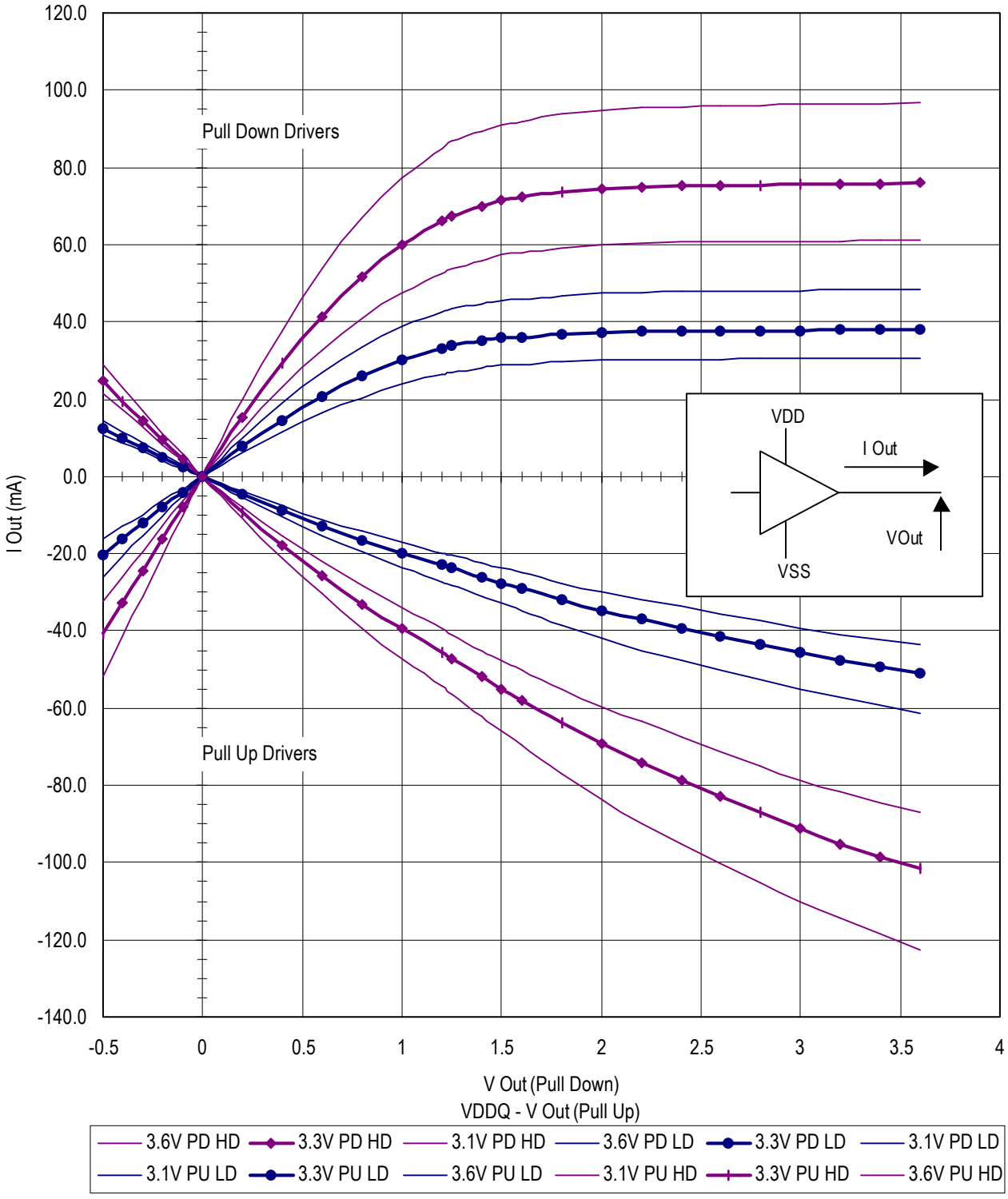
Order	x36	x18	Bump x36	Bump x18
30	A_9		6A	
31	A_8		5A	
32	A_{17}		4G	
33	NC = 0		4A	
34	ADV		4B	
35	$\overline{G}$		4F	
36	$\overline{CKE}$		4M	
37	$\overline{W}$		4H	
38	CK		4K	
39	PH = 0		n/a	
40	PH = 1		n/a	
41	$\overline{CE_3}$		6B	
42	$\overline{B_A}$		5L	
43	$\overline{B_B}$	$\overline{B_B}$	5G	3G
44	$\overline{B_C}$	NC = 1	3G	5G
45	$\overline{B_D}$	NC = 1	3L	
46	CE_2		2B	
47	$\overline{CE_1}$		4E	
48	A_7		3A	
49	A_6		2A	
50	x36 =DQ_{C9} x32 = NA = 0	NC = 1	2D	
51	DQ_{C8}	NC = 1	1E	
52	DQ_{C4}	NC = 1	2F	
53	DQ_{C3}	NC = 1	1G	
54	DQ_{C7}	NC = 1	2H	
55	DQ_{C6}	DQ_{B1}	1D	
56	DQ_{C5}	DQ_{B2}	2E	
57	DQ_{C2}	DQ_{B3}	2G	
58	DQ_{C1}	DQ_{B4}	1H	
59	$\overline{FT}$		5R	

Order	x36	x18	Bump x36	Bump x18
60	DP		3J	
61	PH = 1		n/a	
62	DQ_{D1}	DQ_{B5}	2K	
63	DQ_{D2}	DQ_{B6}	1L	
64	DQ_{D5}	DQ_{B7}	2M	
65	DQ_{D6}	DQ_{B8}	1N	
66	DQ_{D3}	x18 = DQ_{B9} x16 = NA = 0	1K	2P
67	DQ_{D4}	NC = 1	2L	
68	DQ_{D7}	NC = 1	2N	
69	DQ_{D8}	NC = 1	1P	
70	x36 = DQ_{D9} x32 = NA = 0	NC = 1	2P	1K
71	$\overline{LBO}$		3R	
72	A_5		2C	
73	A_4		3B	
74	A_3		3C	
75	A_2		2R	
76	A_1		4N	
77	A_0		4P	
78	ZQ		4D	

BPR 1999.08.11

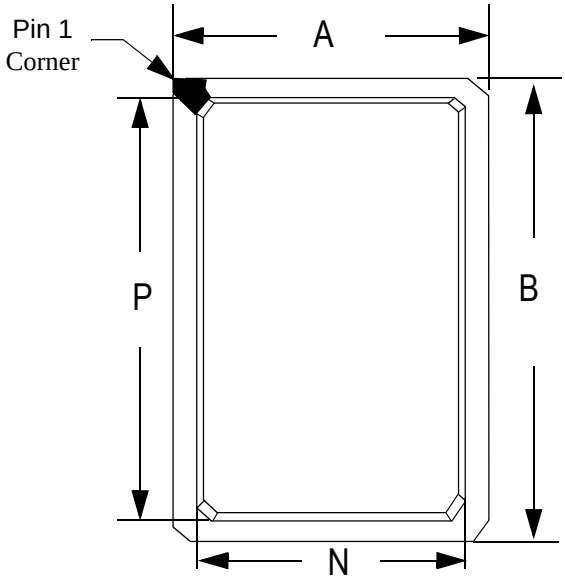
Note:
1. The Boundary Scan Register contains a number of registers that are not connected to any pin. They default to the value shown at reset.
2. Registers are listed in exit order (i.e., Location 1 is the first out of the TDO pin).
3. NC = No Connect, NA = Not Active

FLXDrive Output Driver Characteristics

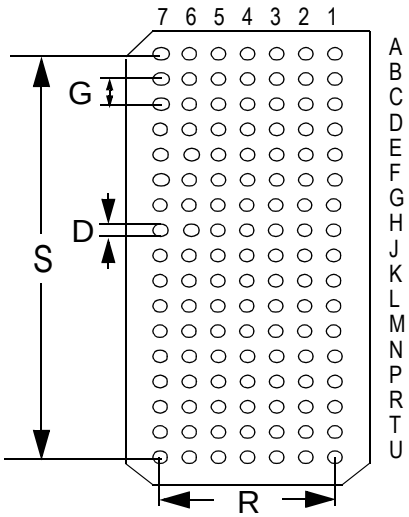


BPR 1999.05.18

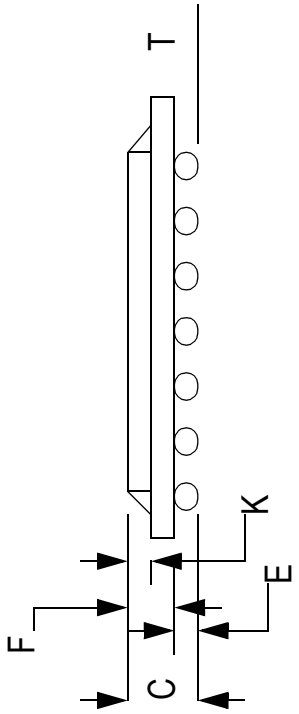
Package Dimensions—119-Bump PBGA



Top View



Bottom View



Side View

Package Dimensions—119-Bump PBGA

Symbol	Description	Min	Nom	Max
A	Width	13.8	14.0	14.2
B	Length	21.8	22.0	22.2
C	Package Height (including ball)	—	—	2.40
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)	—	1.46	1.70
G	Width between Balls	—	1.27	—
K	Package Height above board	0.80	0.90	1.00
N	Cut-out Package Width	—	12.00	—
P	Foot Length	—	19.50	—
R	Width of package between balls	—	7.62	—
S	Length of package between balls	—	20.32	—
T	Variance of Ball Height	—	0.15	—

Unit: mm

BPR 1999.05.18

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
512K x 18	GS882Z18B-11	ByteSafe NBT Pipeline/Flow Through	BGA	100/11	C	
512K x 18	GS882Z18B-100	ByteSafe NBT Pipeline/Flow Through	BGA	100/12	C	
512K x 18	GS882Z18B-80	ByteSafe NBT Pipeline/Flow Through	BGA	80/14	C	
512K x 18	GS882Z18B-66	ByteSafe NBT Pipeline/Flow Through	BGA	66/18	C	
256K x 36	GS882Z36B-11	ByteSafe NBT Pipeline/Flow Through	BGA	100/11	C	
256K x 36	GS882Z36B-100	ByteSafe NBT Pipeline/Flow Through	BGA	100/12	C	
256K x 36	GS882Z36B-80	ByteSafe NBT Pipeline/Flow Through	BGA	80/14	C	
256K x 36	GS882Z36B-66	ByteSafe NBT Pipeline/Flow Through	BGA	66/18	C	
512K x 18	GS882Z18B-11I	ByteSafe NBT Pipeline/Flow Through	BGA	100/11	I	
512K x 18	GS882Z18B-100I	ByteSafe NBT Pipeline/Flow Through	BGA	100/12	I	
512K x 18	GS882Z18B-80I	ByteSafe NBT Pipeline/Flow Through	BGA	80/14	I	
512K x 18	GS882Z18B-66I	ByteSafe NBT Pipeline/Flow Through	BGA	66/18	I	
256K x 36	GS882Z36B-11I	ByteSafe NBT Pipeline/Flow Through	BGA	100/11	I	
256K x 36	GS882Z36B-100I	ByteSafe NBT Pipeline/Flow Through	BGA	100/12	I	
256K x 36	GS882Z36B-80I	ByteSafe NBT Pipeline/Flow Through	BGA	80/14	I	
256K x 36	GS882Z36B-66I	ByteSafe NBT Pipeline/Flow Through	BGA	66/18	I	

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS882Z36B-100IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page /Revisions/Reason
GS882Z818/36BRev1.04h 5/ 1999; 1.05 9/1999	Format/Typos	• Last Page/Fixed "GSGS.." in Ordering Information Note.Document/Changed format of all E's from EN to EN. • Timing Diagrams/Changed format. ex. A0 to A0. • Flow Through Timing Diagrams/Upper case "T" in Flow Through. thru to Through. • Pin outs/Block Diagrams -Updated format to small caps. • Added Rev History.
	Content	• Pin Outs/Numbered all data I/O's. • Boundary Scan/Ordered Data I/O pins correctly. • Speed Bins on Page 1/Last column-changed 12ns to 15ns and 15ns to 12ns.
GS882Z818/36B 1.05 9/ 1999K/ 1.06 10/1999	Format	• Improved Appearance of Timing Diagrams. • Minor formatting changes.
GS882Z818/36B 1.06 9/ 1999K 1.07 1/2000L	Content	• Changed pin 4J to VDD in x 18 Pinout. • Took out overbar on NC in PinoutNew GSI Logo.Placed pin 4A in the No Connect list in the pin description.
Rev.1.10; 882Z18_r1_11	Content/Format	• Removed 166 and 150 MHz speed bins • Used 100 MHz Pipeline numbers for 133 MHz • Changed all 133 MHz references to 11 ns • Updated format to comply with Technical Publications standards
882Z18_r1_11; 882Z18_r1_12	Content	• Updated Capitance table—removed Input row and changed Output row to I/O
882Z18_r1_12; 882Z18_r1_13	Content	• Corrected typo on pinouts
882Z18_r1_13; 882Z18_r1_14	Content	• Removed SCD/DCD reference from Mode Pin Functions table on page 11
882Z18_r1_14; 882Z18_r1_15	Content	• Added parity bit references to x36 pad out • Updated order of data input and output pins in pin description table

