Features

- 16 Channel GPS Correlator
  - 8192 Search Bins with GPS Acquisition Accelerator
  - Accuracy: 2.5m CEP (Stand-Alone, S/A off)
  - Time to First Fix: 34s (Cold Start)
  - Acquisition Sensitivity: –140 dBm
  - Tracking Sensitivity: –150 dBm
- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - EmbeddedICE™ (In-circuit Emulator)
- 128 Kbyte Internal RAM
- 384 Kbyte Internal ROM, Firmware Version V5.0
- Position Technology Provided by u-blox
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 8 Mbytes
  - Up to 4 Chip Selects
  - Software Programmable 8-bit/16-bit External Data Bus
- 6-channel Peripheral Data Controller (PDC)
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 2 External Interrupts
- 32 User-programmable I/O Lines
- 1 USB Device Port
  - Universal Serial Bus (USB) V2.0 Full-speed Device
  - Embedded USB V2.0 Full-speed Transceiver
  - Suspend/Resume Logic
  - Ping-pong Mode for Isochronous and Bulk Endpoints
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Advanced Power Management Controller (APMC)
  - Peripherals Can Be Deactivated Individually
  - Geared Master Clock to Reduce Power Consumption
  - Sleep State with Disabled Master Clock
  - Hibernate State with 32.768 kHz Master Clock
- Real Time Clock (RTC)
- 2.3V to 3.6V or 1.8V Core Supply Voltage
- Includes Power Supervisor
- 1.8V to 3.3V User-definable I/O Voltage for Several GPIOs with 5V Tolerance
- 4 Kbytes Battery Backup Memory
- 9 mm × 9 mm 100-pin BGA Package (LFBGA100)
- RoHS-compliant

GPS Baseband Processor

ATR0621P1 Automotive

Summary

NOTE: This is a summary document. The complete document is available. For more information, please contact your local Atmel sales office.

4975BS–GPS–05/08

1. Description

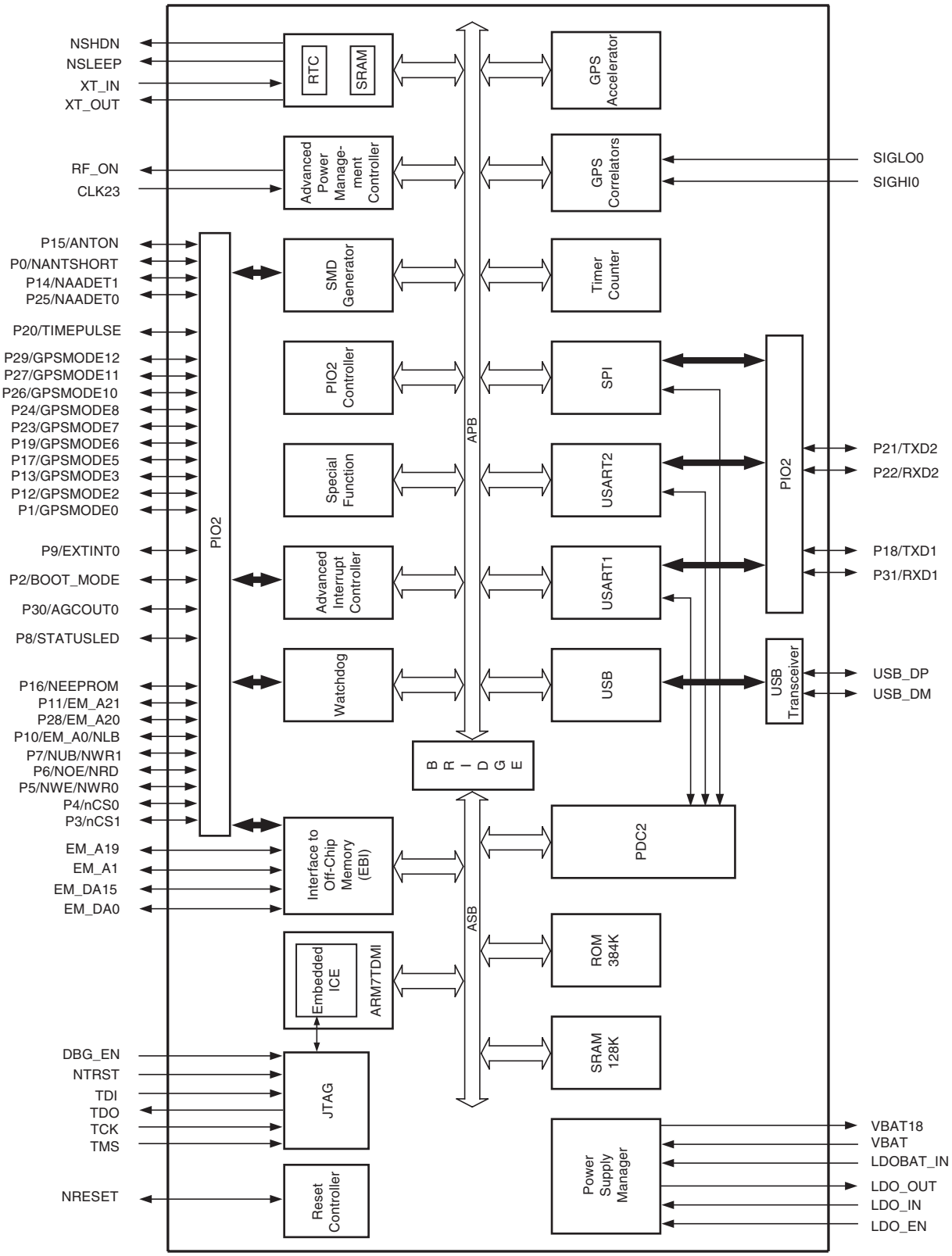
The GPS baseband processor ATR0621P1 includes a 16-channel GPS correlator and is based on the ARM7TDMI processor core.

This processor has a high-performance 32-bit RISC architecture and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The ATR0621P1 has two USART and an USB device port. This port is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The ATR0621P1 has a direct connection to off-chip memory, including Flash, through the External Bus Interface (EBI).

The ATR0621P1 includes full GPS firmware, licensed from u-blox AG, which performs the basic GPS operation, including tracking, acquisition, navigation and position data output. For normal PVT (Position/Velocity/Time) applications, there is no need for off-chip Flash memory or ROM. The firmware supports e.g. the NMEA® protocol (2.1 and 2.3), a binary protocol for PVT data, configuration and debugging, the RTCM protocol for DGPS, SBAS (WAAS, EGNOS and MSAS) and A-GPS (aiding). It is also possible to store the configuration settings in an optional external EEPROM.

The ATR0621P1 is manufactured using the Atmel® high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, 16-channel GPS correlator and a wide range of peripheral functions on a monolithic chip, the ATR0621P1 provides a highly-flexible and cost-effective solution for GPS applications.

Figure 1-1. Block Diagram



2. Architectural Overview

2.1 Description

The ATR0621P1 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The ATR0621P1 peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits, and the third address reads the value stored in the register. A bit can be set or reset by writing a “1” to the corresponding position at the appropriate address. Writing a “0” has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit-manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode on the ATR0621P1 GPS Baseband. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI datasheet.

The ARM standard In-Circuit Emulation debug interface is supported via the JTAG/ICE port of the ATR0621P1.

Features of the ROM firmware are described in software documentation available from u-blox AG, Switzerland.

3. Pin Configuration

3.1 Pinout

Figure 3-1. Pinout LFBGA100 (Top View)

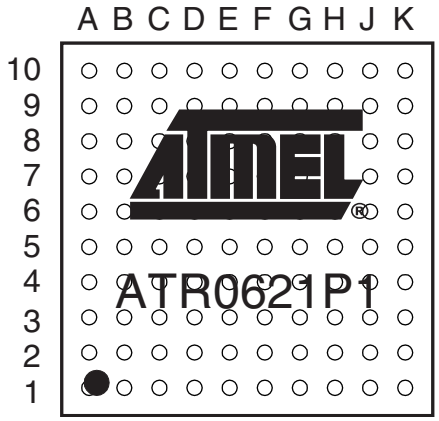


Table 3-1. ATR0621P1 Pinout

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
CLK23	G9	IN						
DBG_EN	H4	IN	PD					
EM_A1	A6	OUT						
EM_A2	A5	OUT						
EM_A3	A4	OUT						
EM_A4	A2	OUT						
EM_A5	A3	OUT						
EM_A6	B5	OUT						
EM_A7	B4	OUT						
EM_A8	B2	OUT						
EM_A9	D4	OUT						
EM_A10	C2	OUT						
EM_A11	D6	OUT						
EM_A12	D7	OUT						
EM_A13	C3	OUT						
EM_A14	C1	OUT						
EM_A15	D5	OUT						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P1 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
EM_A16	C6	OUT						
EM_A17	F8	OUT						
EM_A18	B3	OUT						
EM_A19	C5	OUT						
EM_DA0	B6	I/O	PD					
EM_DA1	B10	I/O	PD					
EM_DA2	C7	I/O	PD					
EM_DA3	C10	I/O	PD					
EM_DA4	D10	I/O	PD					
EM_DA5	E7	I/O	PD					
EM_DA6	E9	I/O	PD					
EM_DA7	B7	I/O	PD					
EM_DA8	B8	I/O	PD					
EM_DA9	A9	I/O	PD					
EM_DA10	C8	I/O	PD					
EM_DA11	B9	I/O	PD					
EM_DA12	D8	I/O	PD					
EM_DA13	C9	I/O	PD					
EM_DA14	D9	I/O	PD					
EM_DA15	E8	I/O	PD					
GND	A1	IN						
GND	A10	IN						
GND	K1	IN						
GND	K10	IN						
LDOBAT_IN	K8	IN						
LDO_EN	H7	IN						
LDO_IN	K7	IN						
LDO_OUT	H6	OUT						
NRESET	C4	I/O	Open Drain PU					
NSHDN	G7	OUT						
NSLEEP	J6	OUT						
NTRST	K2	IN	PD					
P0	K9	I/O	PD	NANTSHORT				
P1	G3	I/O	Configurable (PD)	GPSMODE0		AGCOUT1		

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P1 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
P2	G4	I/O	Configurable (PD)	BOOT_MODE		“0”		
P3	H5	I/O	OH	NCS1		NCS1		“0”
P4	A7	I/O	OH	NCS0		NCS0		“0”
P5	B1	I/O	OH	NWE/NWR0		NWE/NWR0		“0”
P6	A8	I/O	OH	NOE/NRD		NOE/NRD		“0”
P7	D2	I/O	OH	NUB/NWR1		NUB/NWR1		“0”
P8	G2	I/O	Configurable (PD)	STATUSLED		“0”		
P9	J8	I/O	PU to VBAT18	EXTINT0	EXTINT0			
P10	E4	I/O	OH	EM_A0/NLB		EM_A0/NLB		“0”
P11	H10	I/O	OH	EM_A21		NCS2		EM_A21
P12	F3	I/O	Configurable (PU)	GPSMODE2		NPCS2		
P13	G10	I/O	PU to VBAT18	GPSMODE3	EXTINT1			
P14	J5	I/O	Configurable (PD)	NAADET1		“0”		
P15	K5	I/O	PD	ANTON				
P16	E1	I/O	Configurable (PU)	NEEPROM	SIGHI1			NWD_OVF
P17	J4	I/O	Configurable (PD)	GPSMODE5	SCK1	SCK1		
P18	K4	I/O	Configurable (PU)	TXD1		TXD1		“0”
P19	F1	I/O	Configurable (PU)	GPSMODE6	SIGLO1			“0”
P20	H2	I/O	Configurable (PD)	TIMEPULSE	SCK2	SCK2		TIMEPULSE
P21	F2	I/O	Configurable (PU)	TXD2		TXD2		“0”
P22	H8	I/O	PU to VBAT18	RXD2	RXD2			
P23	H3	I/O	Configurable (PU)	GPSMODE7	SCK	SCK		MCLK_OUT
P24	H1	I/O	Configurable (PU)	GPSMODE8	MOSI	MOSI		“0”
P25	D1	I/O	Configurable (PD)	NAADET0	MISO	MISO		“0”
P26	G8	I/O	Configurable (PU)	GPSMODE10	NSS	NPCS0		“0”
P27	E2	I/O	Configurable (PU)	GPSMODE11		NPCS1		
P28	G1	I/O	OH	EM_A20		NCS3		EM_A20
P29	E3	I/O	Configurable (PU)	GPSMODE12		NPCS3		
P30	G5	I/O	PD	AGCOUT0		AGCOUT0		“0”
P31	H9	I/O	PU to VBAT18	RXD1	RXD1			
RF_ON	K6	OUT	PD					
SIGHI0	F9	IN						
SIGLO0	E10	IN						
TCK	J3	IN	PU					

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P1 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
TDI	J2	IN	PU					
TDO	K3	OUT						
TMS	J1	IN	PU					
USB_DM	F10	I/O						
USB_DP	D3	I/O						
VBAT	J7	IN						
VBAT18[2]	G6	OUT						
VDD18	E6	IN						
VDD18	F7	IN						
VDD18	F6	IN						
VDDIO[3]	E5	IN						
VDD_USB[4]	F5	IN						
XT_IN	J9	IN						
XT_OUT	J10	OUT						
NC[5]	F4	-						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

3.2 Signal Description

Table 3-2. ATR0621P1 Signal Description

Module	Name	Function	Type	Active Level	Comment
EBI	EM_A0 to EM_A21	External memory address bus	Output	–	All valid after reset
	EM_DA0 to EM_DA15	External memory data bus	I/O	–	Internal pull-down resistor
	NCS0 to NCS1	Chip select	Output	Low	Output high in RESET state
	NCS2 to NCS3	Chip select	Output	Low	Output high in RESET state
	NWR0	Lower byte write signal	Output	Low	Output high in RESET state
	NWR1	Upper byte write signal	Output	Low	Output high in RESET state
	NRD	Read signal	Output	Low	Output high in RESET state
	NWE	Write enable	Output	Low	Output high in RESET state
	NOE	Output enable	Output	Low	Output high in RESET state
	NUB	Upper byte select (16-bit SRAM)	Output	Low	Output high in RESET state
	NLB	Lower byte select (16-bit SRAM)	Output	Low	Output high in RESET state
	BOOT_MODE	Boot mode input	Input	–	PIO-controlled after reset, internal pull-down resistor
USART	TXD1-2	Transmit data output	Output	–	PIO-controlled after reset
	RXD1-2	Receive data input	Input	–	PIO-controlled after reset
	SCK1-2	External synchronous serial clock	I/O	–	PIO-controlled after reset
USB	USB_DP	USB data (D+)	I/O	–	
	USB_DM	USB data (D-)	I/O	–	
APMC	RF_ON		Output	–	Interface to ATR0601
AIC	EXTINT0-1	External interrupt request	Input	High/ Low/ Edge	PIO-controlled after reset
AGC	AGCOUT0-1	Automatic gain control	Output	–	Interface to ATR0601 PIO-controlled after reset
RTC	NSLEEP	Sleep output	Output	Low	Interface to ATR0601
	NSHDN	Shutdown output	Output	Low	Connect to pin LDO_EN
	XT_IN	Oscillator input	Input	–	RTC oscillator
	XT_OUT	Oscillator output	Output	–	RTC oscillator
SPI	SCK	SPI clock	I/O	–	PIO-controlled after reset
	MOSI	Master out slave in	I/O	–	PIO-controlled after reset
	MISO	Master in slave out	I/O	–	PIO-controlled after reset
	NSS/NPCS0	Slave select	I/O	Low	PIO-controlled after reset
	NPCS1-3	Slave select	Output	Low	PIO-controlled after reset
WD	NWD_OVF	Watchdog timer overflow	Output	–	PIO-controlled after reset
PIO	P0-31	Programmable I/O port	I/O	–	Input after reset (except P3 to P7, P10, P11, P28)

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

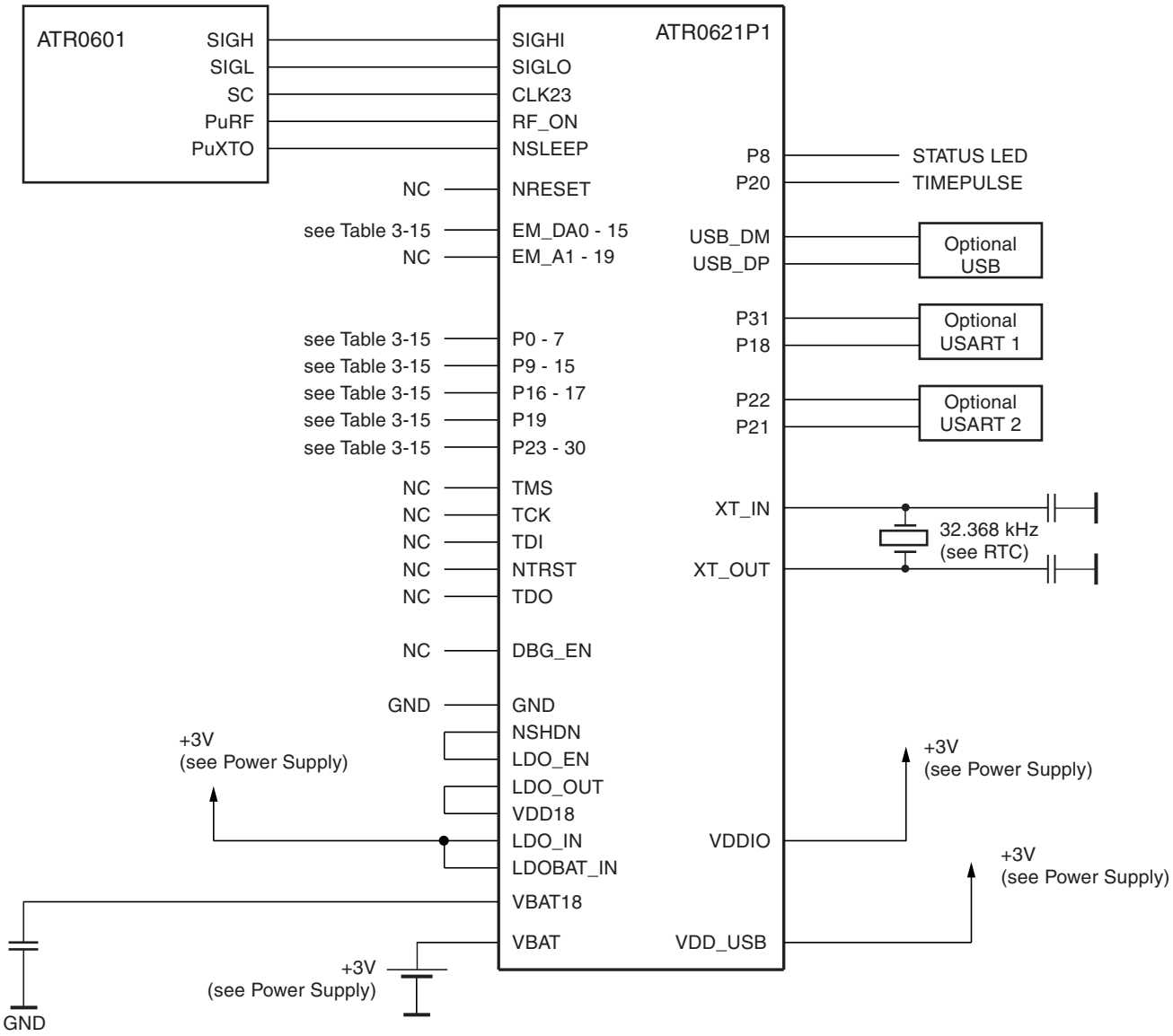
Table 3-2. ATR0621P1 Signal Description (Continued)

Module	Name	Function	Type	Active Level	Comment
GPS	SIGHI0	Digital IF	Input	–	Interface to ATR0601
	SIGLO0	Digital IF	Input	–	Interface to ATR0601
	SIGHI1	Digital IF	Input	–	PIO-controlled after reset
	SIGLO1	Digital IF	Input	–	PIO-controlled after reset
	TIMEPULSE	GPS synchronized time pulse	Output	–	PIO-controlled after reset
CONFIG	GPSMODE0-12	GPS mode	Input	–	PIO-controlled after reset
	STATUSLED	Status LED	Output	–	PIO-controlled after reset
	NEEPROM	Enable EEPROM support	Input	Low	PIO-controlled after reset
	ANTON	Active antenna power on output	Output	–	PIO-controlled after reset
	NANTSHORT	Active antenna short circuit detection Input	Input	Low	PIO-controlled after reset
	NAADET0-1	Active antenna detection input	Input	Low	PIO-controlled after reset
JTAG/ICE	TMS	Test mode select	Input	–	Internal pull-up resistor
	TDI	Test data in	Input	–	Internal pull-up resistor
	TDO	Test data out	Output	–	Output high in RESET state
	TCK	Test clock	Input	–	Internal pull-up resistor
	NTRST	Test reset input	Input	Low	Internal pull-down resistor
	DBG_EN	Debug enable	Input	High	Internal pull-down resistor
CLOCK	CLK23	Clock input	Input	–	Interface to ATR0601, Schmitt trigger input
	MCLK_OUT	Master clock output	Output	–	PIO-controlled after reset
RESET	NRESET	Reset input	I/O	Low	Open drain with internal pull-up resistor
POWER	VDD18		Power	–	Core voltage 1.8V
	VDDIO		Power	–	Variable I/O voltage 1.65V to 3.6V
	VDD_USB		Power	–	USB voltage 0 to 2.0V or 3.0Vto 3.6V[1]
	GND		Power	–	Ground
LDOBAT	LDOBAT_IN		Power	–	2.3V to 3.6V
	VBAT		Power	–	1.5V to 3.6V
	VBAT18		Out	–	1.8V backup voltage
LDO18	LDO_IN	LDO in	Power	–	2.3V to 3.6V
	LDO_OUT	LDO out	Power	–	1.8V core voltage, maximum 80 mA
	LDO_EN	LDO enable	Input	–	

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

3.3 External Connections for a Working GPS System

Figure 3-2. Example of an External Connection



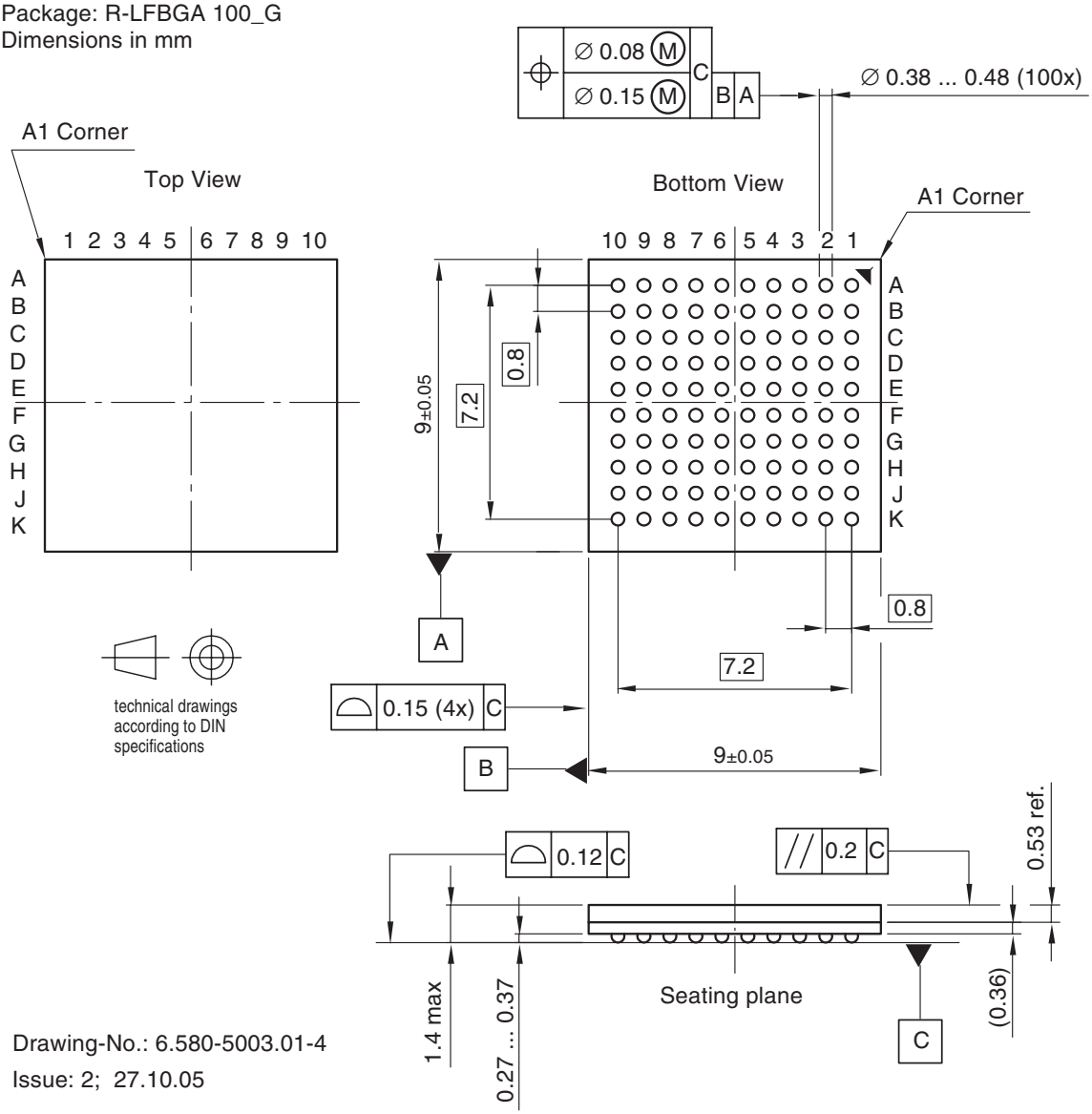
NC: Not connected

4. Ordering Information

Extended Type Number	Package	MPQ	Remarks
ATR0621P1-7FQY	LFBGA100	2000	9 mm × 9 mm, 0.80 mm pitch, ROM5, RoHS-compliant, automotive type
ATR0621P1-7FHW	LFBGA100	2000	9 mm × 9 mm, 0.80 mm pitch, ROM5, RoHS-compliant, green, automotive type
ATR0622-EK1	-	1	Evaluation kit/road test kit
ATR0622-DK1	-	1	Development kit including example design information

5. Package LFBGA100

Package: R-LFBGA 100_G
Dimensions in mm



Drawing-No.: 6.580-5003.01-4
Issue: 2; 27.10.05

Moisture sensitivity level (MSL) = 3

6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, and not to this document.

Revision No.	History
4975BS-GPS-05/08	• Table 3-1 “ATR0621P1 Pinout” on page 5: Pin type of pin CLK23 changed.

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