DATA SHEET

SAA5249
Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX)

Preliminary specification
Supersedes data of December 1993
File under Integrated Circuits, IC02

1996 Nov 07

Philips Semiconductors

PHILIPS

Integrated VIP and Teletext with Background Memory Controller

SAA5249

FEATURES

- Complete teletext decoder featuring a background memory controller in a single 48-pin DIP package. Capable of storing of up to 512 teletext pages in an external DRAM, giving instant access to the teletext data
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and the language option is readable via I²C-bus.
- 100% hardware compatible with the SAA5247 plug-in replacement and with the possibility of extra market in those countries with packet 26 transmissions. Still pin-aligned to SAA5254 and SAA5244A.
- 100% software compatible with the SAA5247, and SAA5244A, except if the special OSD symbols were used. Also 100% software compatible to SAA5254. In all events there is a change to the ROM ID number.
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5281 and the SAA5254, making one hardware solution for the whole range
- Low software overhead for the microprocessor
- RGB interface to standard colour decoder ICs, push-pull output drive.

GENERAL DESCRIPTION

The Integrated VIP and Teletext (IVT1.1BMCX) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. With its built-in background memory controller the device can store incoming teletext packets in the external 1M4 DRAM. With this large packet store which can be rapidly scanned, we can achieve near instantaneous access to all the pages transmitted by the broadcaster.

This version of the decoder also contains some extra hardware to process extension packet 26 automatically, extending the markets to which the TV chassis can be shipped and offering many more language options for the set maker.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5249P/E	DIP48	plastic dual in-line package; 48 leads (600 mil)	SOT240-1
SAA5249GP/E	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

BLOCK DIAGRAM

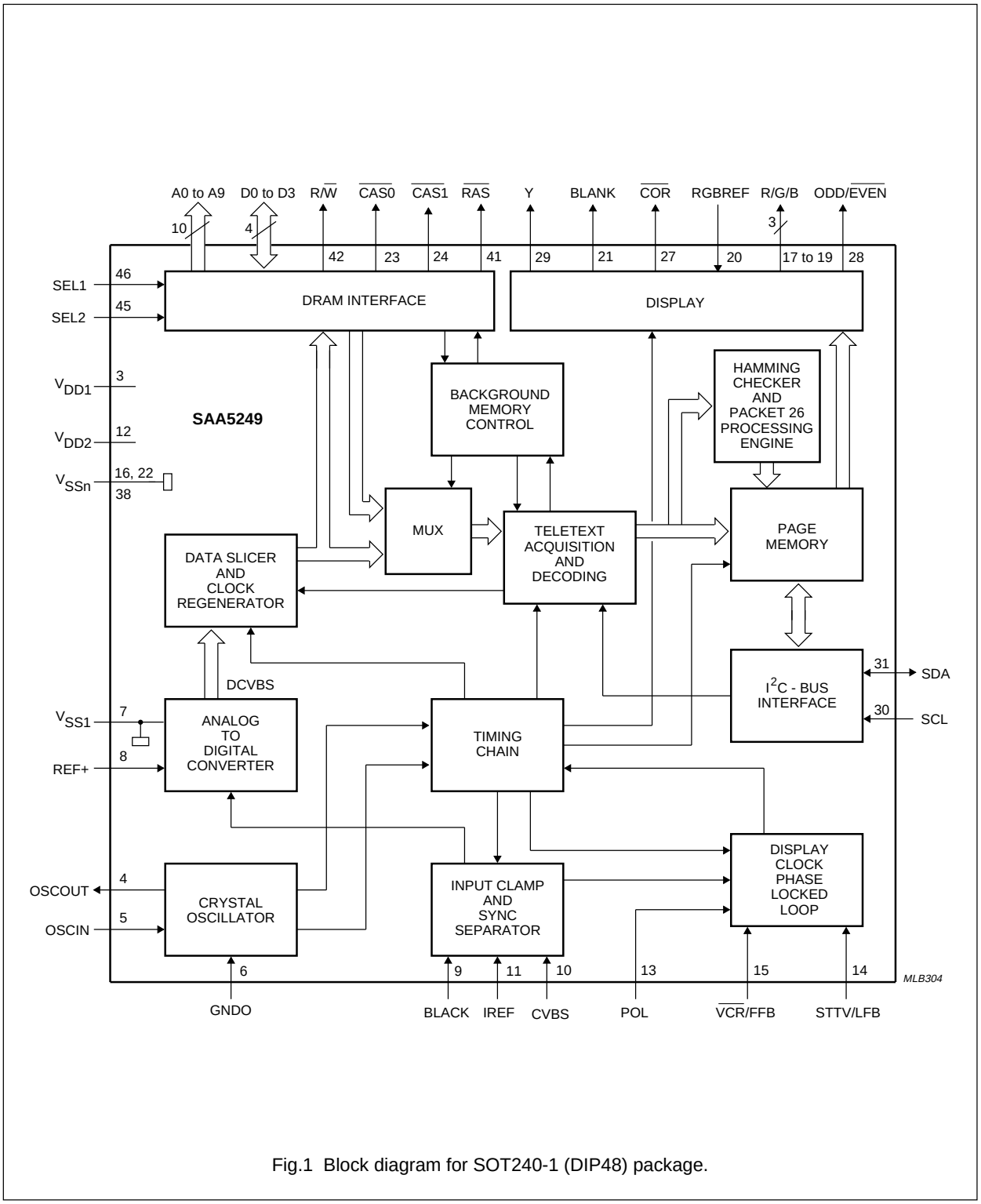


Fig.1 Block diagram for SOT240-1 (DIP48) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT319-1[1]	
n.c.	1	1	not connected
n.c.	2	2	not connected
V_{DD1}	3	25	+5 V supply
OSCOUT	4	27	27 MHz crystal oscillator output
OSCIN	5	28	27 MHz crystal oscillator input
GNDO	6	29	0 V crystal oscillator ground
V_{SS1}	7	12	0 V ground
REF+	8	32	positive reference voltage; this pin should be connected to ground via a 100 nF capacitor
BLACK	9	35	video black level storage pin; this pin should be connected to ground via a 100 nF capacitor
CVBS	10	36	composite video input pin; a positive-going 1 V (p-p) input is required, connected via a 100 nF capacitor
IREF	11	37	reference current input pin; connected to ground via a 27 kΩ resistor
V_{DD2}	12	38	+5 V supply
POL	13	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	14	40	sync to TV output pin/line flyback input pin; function controlled by an internal register bit (scan sync mode)
$\overline{\text{VCR}}$/FFB	15	42	PLL time constant switch/field input pin; function controlled by an internal register bit (scan sync mode)
V_{SS2}	16	30	0 V ground
REF–	–	31	negative reference voltage; this pin should be connected to REF+ via a 100 nF capacitor
R	17	49	dot rate character output of the RED colour information
G	18	50	dot rate character output of the GREEN colour information
B	19	51	dot rate character output of the BLUE colour information
RGBREF	20	52	input DC voltage to define the output high level on the RGB pins
BLANK	21	53	dot rate fast blanking output
V_{SS3}	22	54, 55	0 V ground; internally connected for SOT319
$\overline{\text{CAS0}}$	23	56	column address select to external DRAM for BMCX function
$\overline{\text{CAS1}}$	24	57	column address select to external DRAM for BMCX function for second DRAM where two 256 k × 4 devices are used
A4	25	58	address output to external DRAM for BMCX function
A3	26	59	address output to external DRAM for BMCX function
$\overline{\text{COR}}$	27	60	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output
ODD/$\overline{\text{EVEN}}$	28	61	25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT319-1[1]	
Y	29	62	dot rate character output of teletext foreground colour information; open drain output
SCL	30	63	serial clock input for I^2C-bus; it can still be driven HIGH during power-down of the device
SDA	31	64	serial data port for the I^2C-bus; open drain output. It can still be driven HIGH during power-down of the device
A5	32	4	address output to external DRAM for BMCX function
A2	33	5	address output to external DRAM for BMCX function
A6	34	6	address output to external DRAM for BMCX function
A1	35	8	address output to external DRAM for BMCX function
A7	36	9	address output to external DRAM for BMCX function
A0	37	11	address output to external DRAM for BMCX function
V_{SS4}	38	43	0 V ground
A8	39	13	address output to external DRAM for BMCX function
A9	40	14	address output to external DRAM for BMCX function
$\overline{RAS}$	41	15	row address select to external DRAM
R/$\overline{W}$	42	18	read/$\overline{write}$ for external DRAM
D2	43	19	data input/output for external DRAM
D0	44	20	data input/output for external DRAM
SEL2	45	21	RAM select input to choose external DRAM size
SEL1	46	22	RAM select input to choose external DRAM size
D3	47	23	data input/output for external DRAM
D1	48	24	data input/output for external DRAM

Note

1. The remaining pins for SOT319 are not connected.

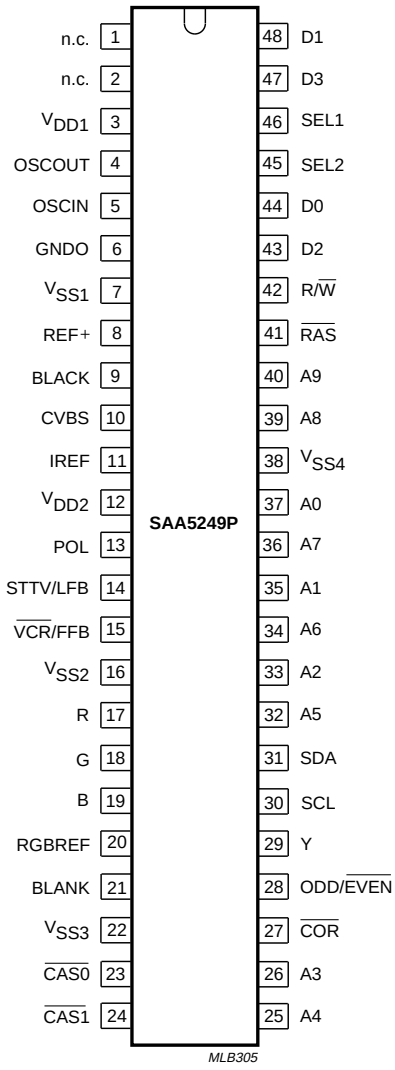


Fig.2 Pin configuration; SOT240-1 (DIP48).

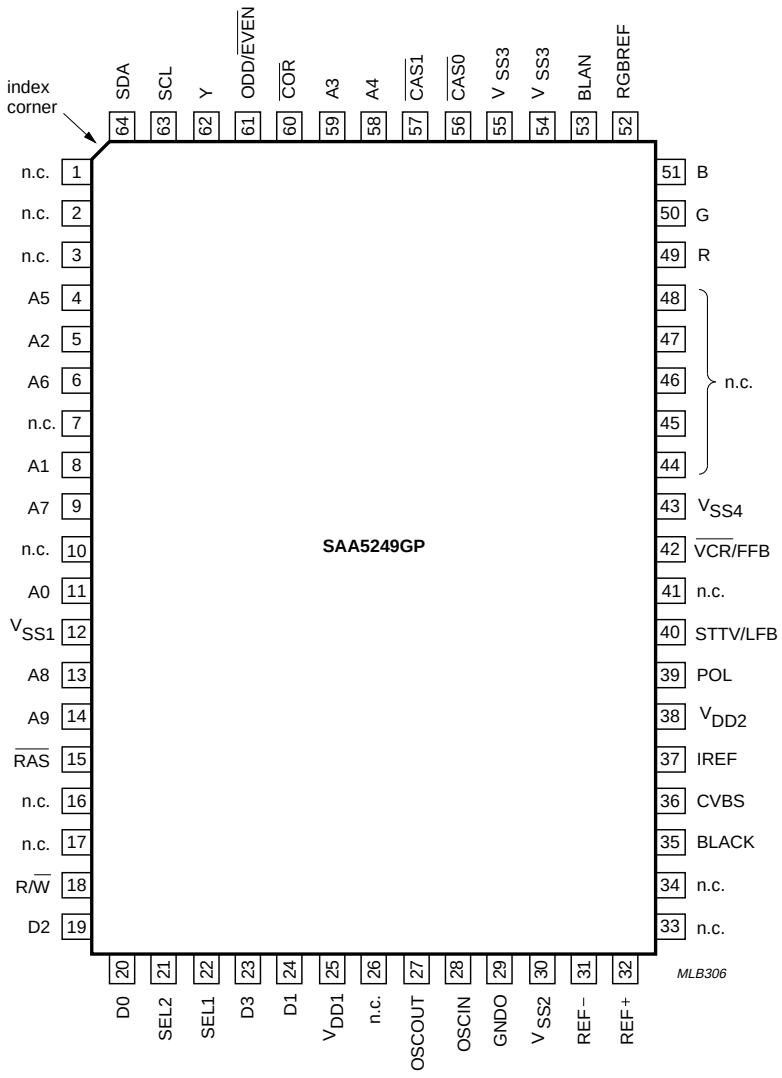


Fig.3 Pin configuration; SOT319-1 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	–0.3	+6.5	V
V_I	input voltage (any input)	–0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	–0.3	V_{DD} + 0.5	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature	–20	+70	°C

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *“Consumer Integrated Circuits SNW-FQ-611-Part E”*. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <100 ppm
Electrical	cumulative target: <100 ppm

Group B

Table 2 Processability tests (by package family)

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family)

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V, 100 pF, 1.5 kΩ	<15% LTPD
	latch-up 100 mA, 1.5 × V_{DD} (absolute maximum)	<15% LTPD

Note to Tables 1 to 4

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
$I_{DD(tot)}$	total supply current		–	90	120	mA
Inputs						
CVBS						
V_{sync}	sync amplitude		0.1	0.3	0.6	V
$t_{d(sync)}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	+150	ns
$\Delta t_{d(sync)}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{source}	source impedance		–	–	250	Ω
C_i	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
I_i	input current	note 1	–1	–	+1	mA
$t_{d(LFB)}$	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
I_i	input current	note 1	–1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF note 2						
V_{IL}	LOW level input voltage		–0.3	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SEL1 AND SEL2						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
SCL						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_i	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	
G_m	mutual conductance	f_i = 100 kHz	1.5	–	–	mA/V
C_i	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
D0 TO D3						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 to 0.6 V	–	–	20	ns
C_L	load capacitance		–	–	50	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{TCS}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A9 ADDRESS OUTPUT TO MEMORY A0 TO A9						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 to 0.6 V	–	–	20	ns
R/$\overline{W}$, $\overline{CASO}$ AND $\overline{CAS1}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 to 0.6 V	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD} – 2 V	RGBREF –0.25	RGBREF	RGBREF +0.25	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLANK						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN-DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} – 0.5 V and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
t_{skew}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLANK		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
DRAM INTERFACE						
t_{RC}	read or write cycle time		344	380	415	ns
t_{RP}	$\overline{RAS}$ precharge time		125	140	155	ns
t_{RAS}	$\overline{RAS}$ pulse width		194	210	230	ns
t_{CAS}	$\overline{CAS}$ pulse width		113	133	153	ns
t_{ASR}	row address set-up time		30	60	80	ns
t_{RAH}	row address hold time		50	60	92	ns
t_{ASC}	column address set-up time		50	60	75	ns
t_{CAH}	column address hold time		50	60	70	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		130	148	160	ns
t_{RAD}	$\overline{RAS}$ to column address delay time		60	74	105	ns
t_{RSH}	$\overline{RAS}$ hold time		15	60	70	ns
t_{CSH}	$\overline{CAS}$ hold time		260	286	300	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		60	70	80	ns
t_{DZO}	$\overline{CAS}$ set-up time from data input		200	225	280	ns
t_r, t_f	rise and fall times		10	15	20	ns
t_{WCS}	write set-up time		193	212	235	ns
t_{WCH}	write command hold time		116	137	150	ns
t_{DS}	data input set-up time		193	212	235	ns
t_{DH}	data input hold time		42	62	80	ns
t_{RAC}	access time from $\overline{RAS}$		165	183	220	ns
t_{CAC}	access time from $\overline{CAS}$		0	35	40	ns
t_{AA}	access time from address		95	108	120	ns
t_{RCS}	read command set-up time		193	212	235	ns
t_{RCH}	read command hold time to $\overline{CAS}$		0	10	20	ns
t_{RRH}	read command hold time to $\overline{RAS}$		55	65	100	ns
t_{RAL}	column address to $\overline{RAS}$ lead time		90	133	150	ns
t_{OFF1}	output buffer turn-off time		20	30	40	ns
t_{CDD}	$\overline{CAS}$ to data input delay time		25	35	45	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ±1 mA.
2. RGBREF is the positive supply pin for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

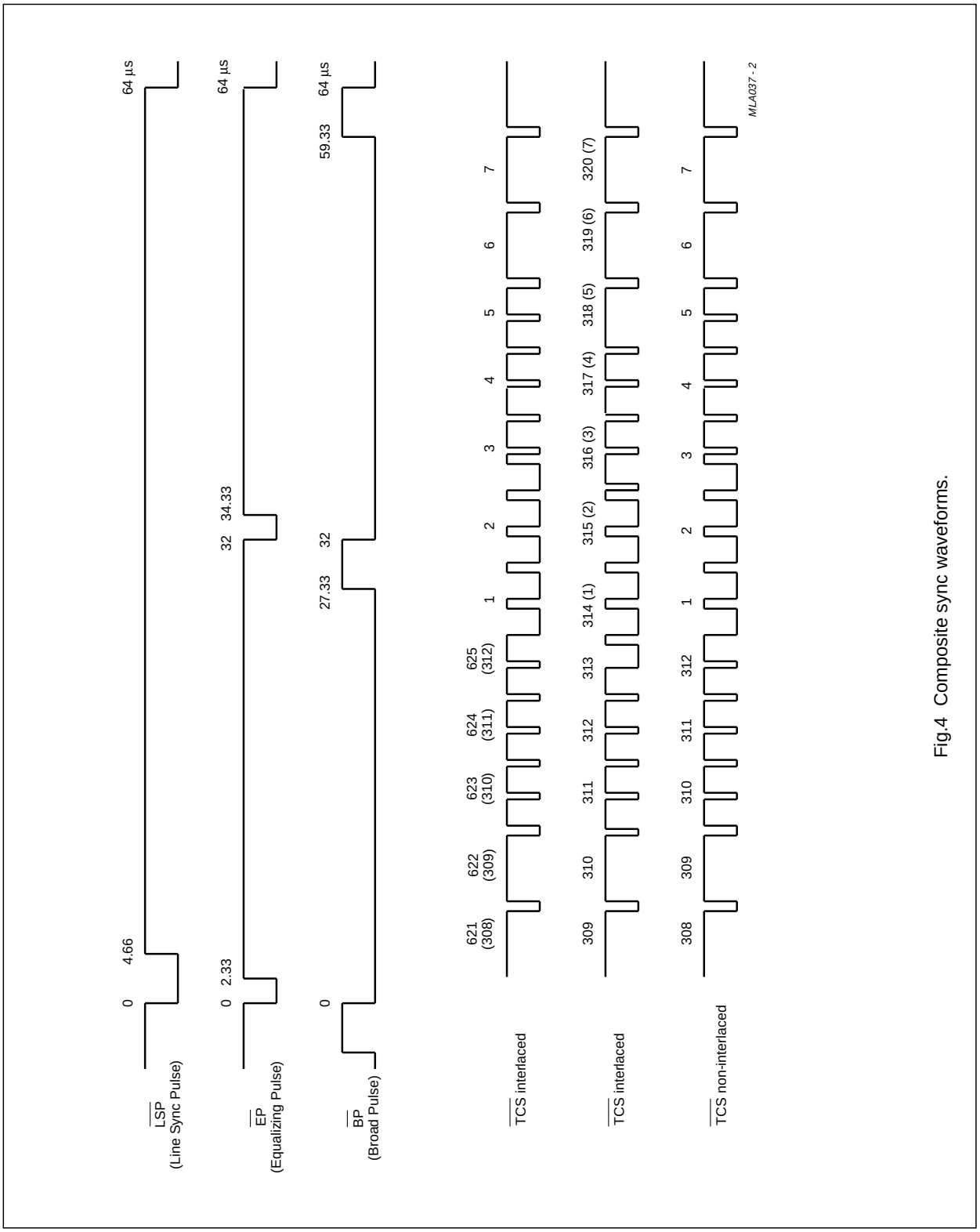
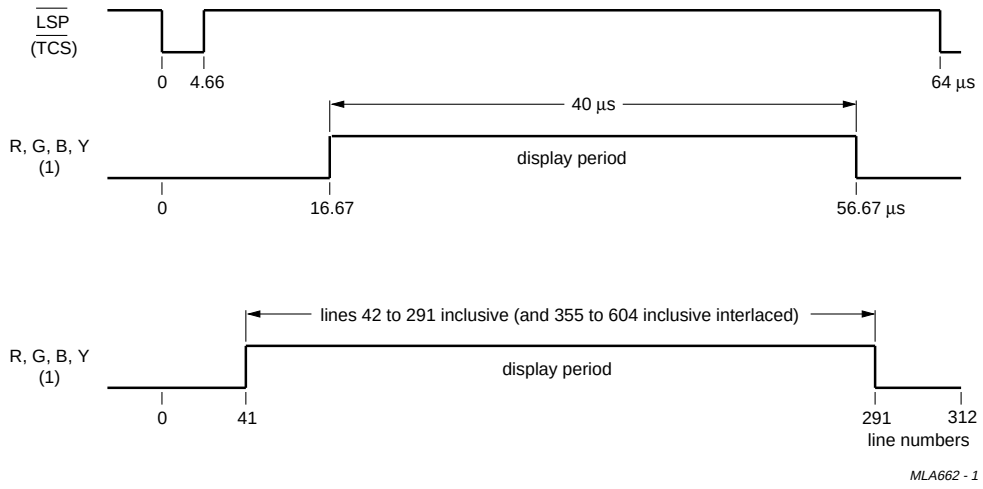


Fig.4 Composite sync waveforms.



(1) Also BLANK in character and box blanking.

Fig.5 Display output timing (a) line rate (b) field rate.

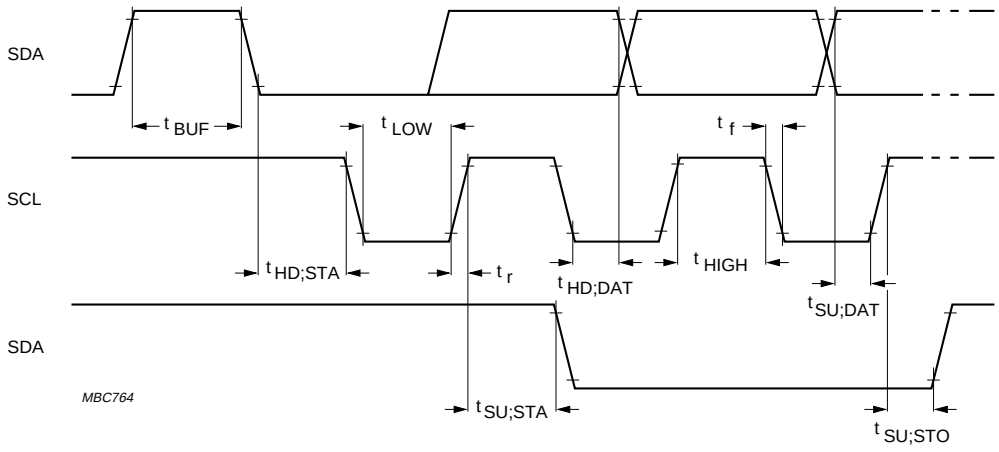


Fig.6 I²C-bus timing.

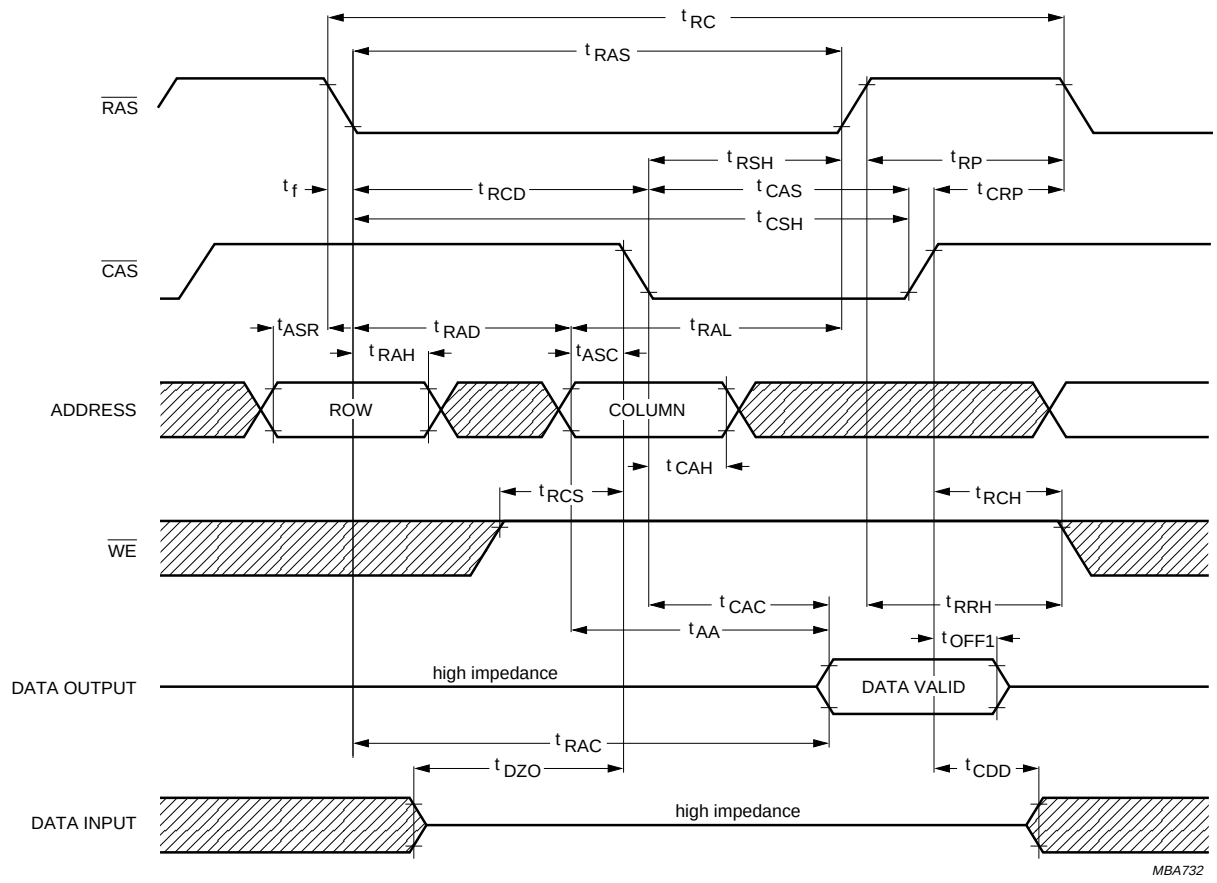


Fig.7 DRAM interface timing; read cycle.

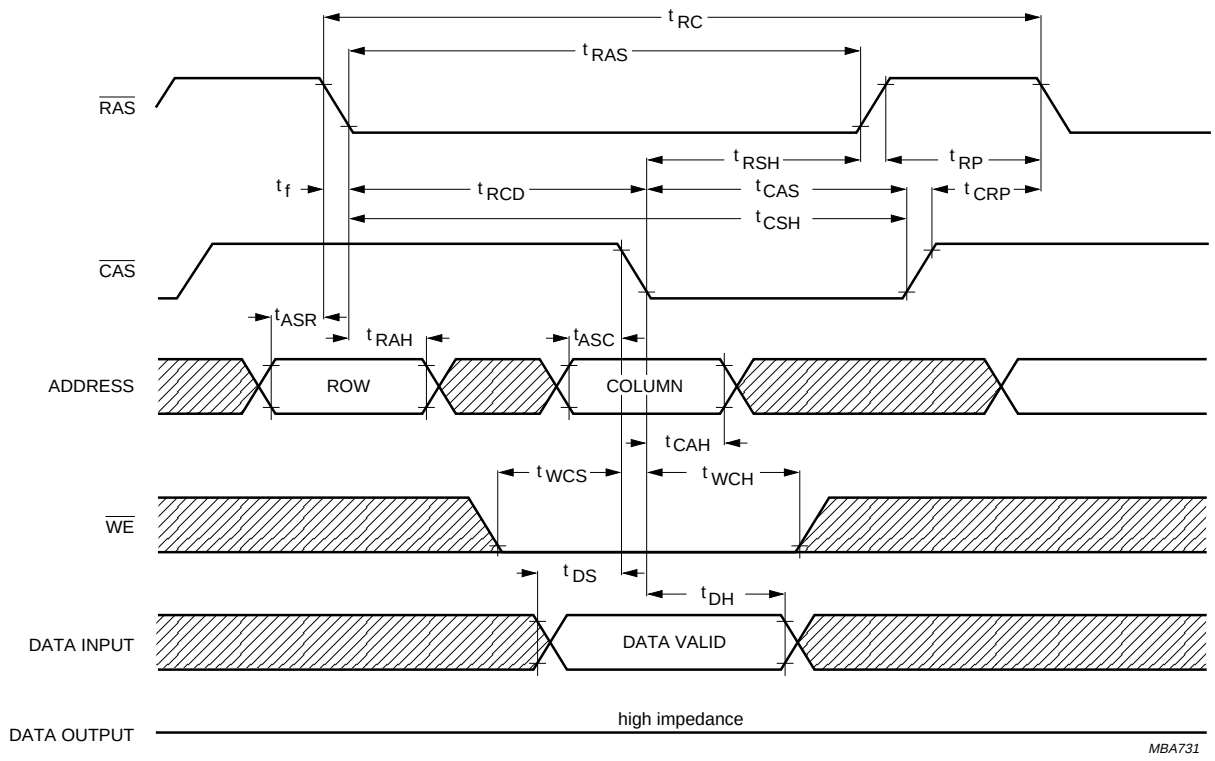


Fig.8 DRAM interface timing; write cycle.

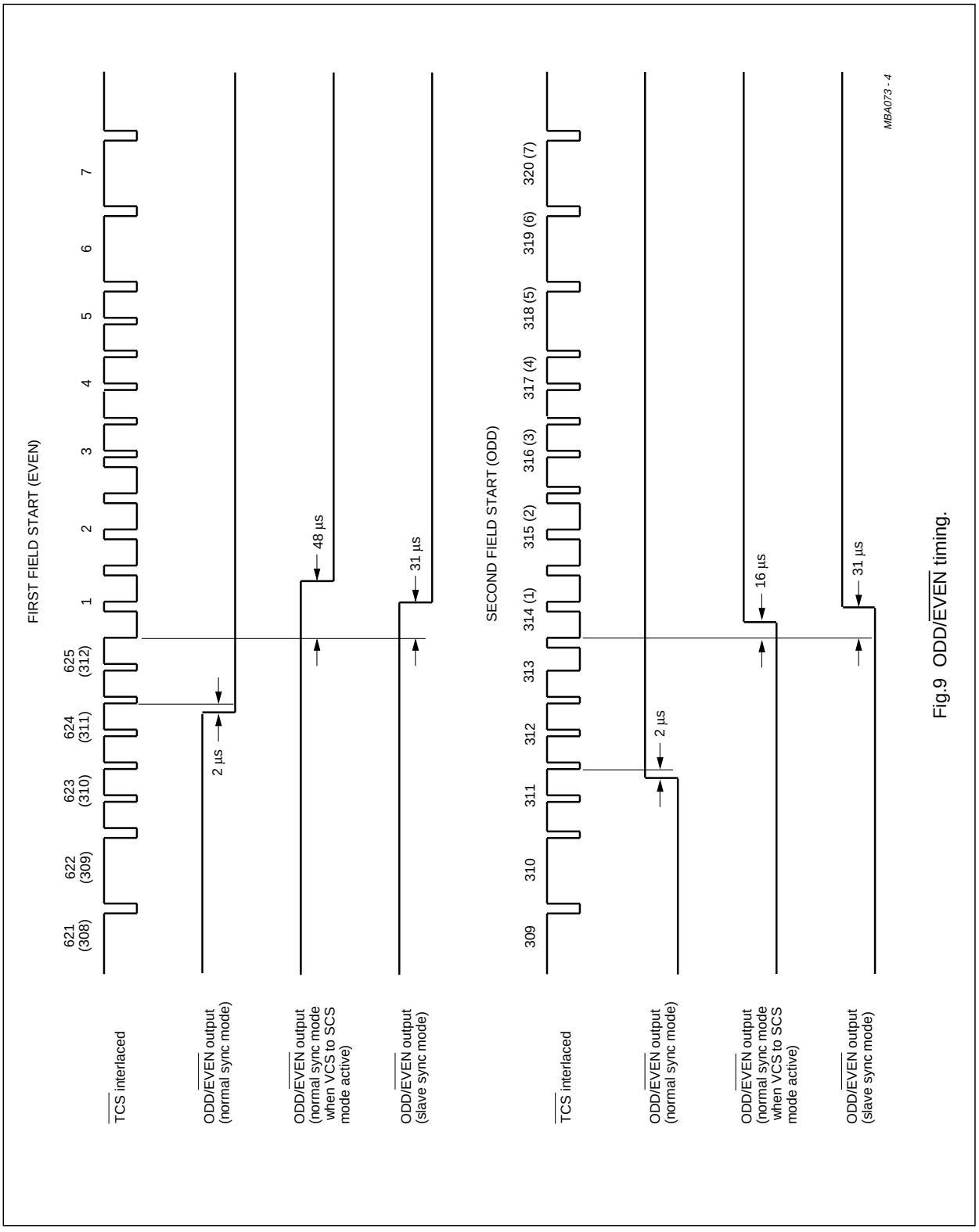


Fig.9 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION

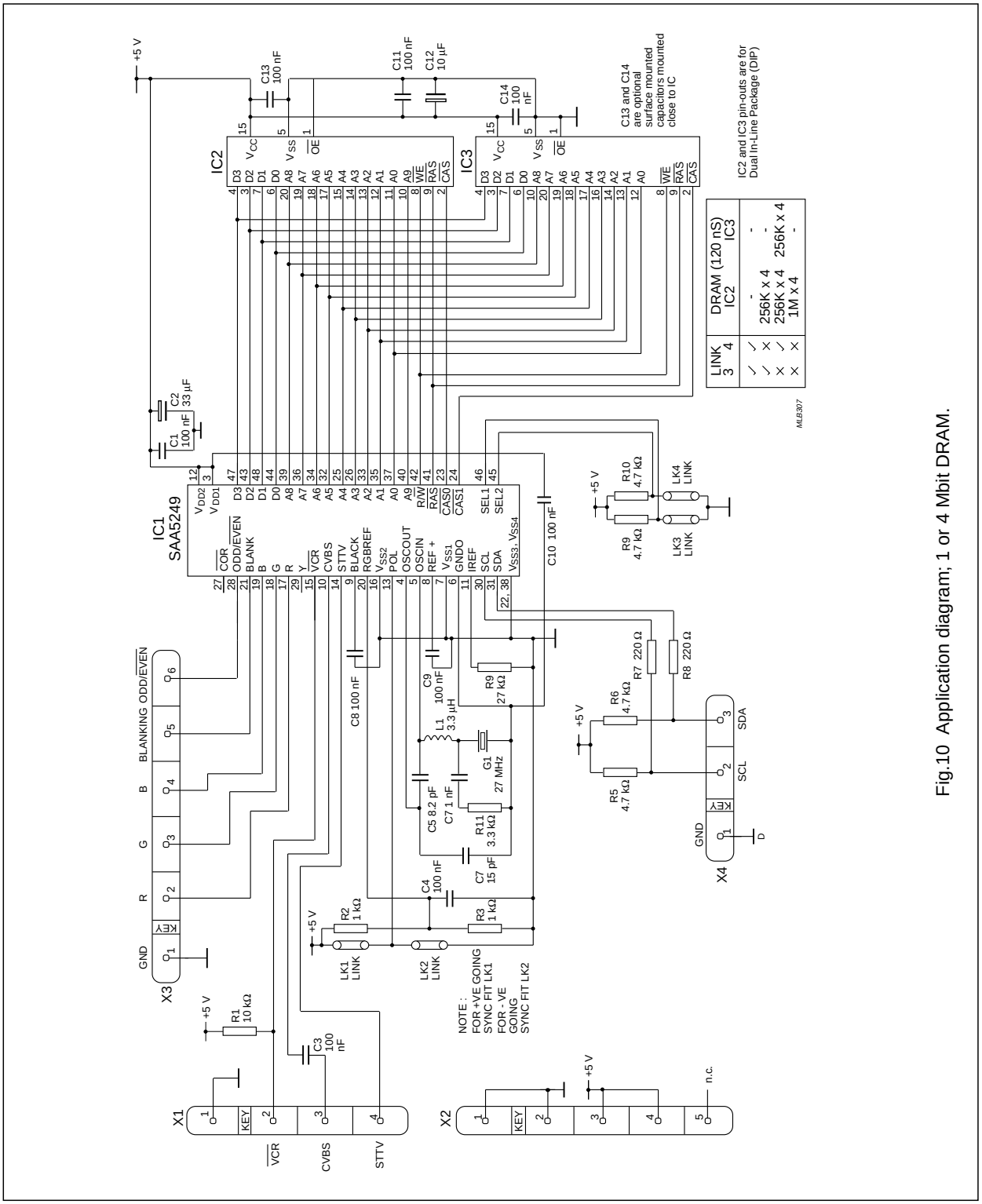


Fig.10 Application diagram; 1 or 4 Mbit DRAM.

IVT1.1BMCX page memory organization

The organization of the page memory is illustrated by Fig.11. The IVT1.1BMCX provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

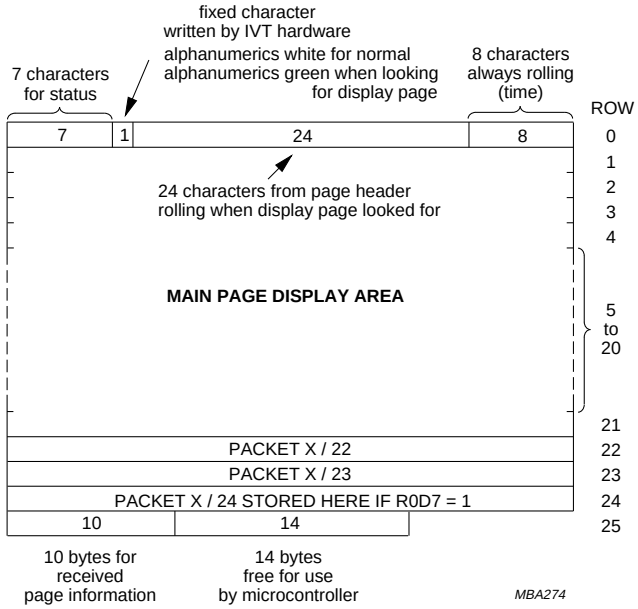


Fig.11 Basic page memory organization.

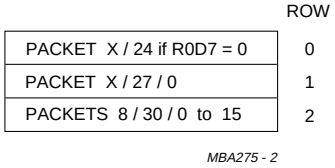


Fig.12 Organization of the extension memory.

REMARK TO Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT1.1BMCX to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 5. The remaining 14-bytes are free for use by the microcomputer.

Table 5 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 6 Page number and sub-code for Table 5

Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4 to C14	transmitted control bits

Register maps

IVT1.1BMCX mode registers R0 to R11 are shown in Table 7. R0 to R10 are write only; R11 is read/write. Register map (R3), for page requests, is shown in detail in Table 9.

Table 7 Register map (notes 1 to 5)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	DISPLAY SRATUS ROW ONLY	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7 + P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	DISABLE PKT 26	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	CLEAR B.M.	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	–	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes

1. The dash (–) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to space (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is alpha white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C-bus slave address is 0010001.

Table 8 Register description

R0 ADVANCED CONTROL - auto increments to register 1	
$\overline{R11}$/R11B SELECT	selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISPLAY STATUS ROW	when SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German TOP system
DISABLE HDR ROLL	disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	when set forces ODD/$\overline{EVEN}$ LOW if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	will force the PLL to free run in all conditions
X24 POS	automatic display of FASTEXT prompt row when logic 1
R1 MODE - auto increments to register 2	
T0, T1	interlace/non-interlace 312/313 line control (see Table 10)
TCS ON	text composite sync or direct sync select (see Table 10 for FFB mode selection)
$\overline{DEW}$/FULL FIELD	field-flyback or full-channel mode
DISABLE PKT 26	disable automatic processing of packet 26
ACQ $\overline{ON}$/OFF	acquisition circuits turned off when logic 1
$\overline{7 + P}$/8-BIT	7-bits with parity checking or 8-bit mode
VCS TO SCS	when logic 1 enables display of messages with 60 Hz input signal
R2 PAGE REQUEST ADDRESS - auto increments to register 3	
COL SCO - SC2	point to start column for page request data (see Table 9)
TB	must be logic 0 for normal operation
R3 PAGE REQUEST DATA - does not auto increment (see Table 9)	
CLEAR B.M.	when set to logic 1. Useful when transmission channel changes
R5 NORMAL DISPLAY CONTROL - auto increments to register 6	
R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to register 7; (note 1)	
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

R7 DISPLAY MODE - does not auto increment	
BOX ON 0	boxing function allowed on Row 0
BOX ON 1-23	boxing function allowed on Rows 1 to 23
BOX ON 24	boxing function allowed on Row 24
DOUBLE HEIGHT	to display double height text
BOTTOM HALF	to select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	to reveal concealed text
CURSOR ON	to display cursor
STATUS TOP	row 25 displayed above or below the main text
R9 CURSOR ROW - auto increments to register 10	
R0 to R4	active row for data written to or read from memory via the I^2C-bus
A0	selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	when set to 1, clears the display memory; this bit is automatically reset
R10 CURSOR COLUMN - auto increments to register 11 or 11B	
C0 to C5	active column for data written to or read from memory via the I^2C-bus
R11 CURSOR DATA - does not auto increment	
D0 to D7	data read from/written to memory via I^2C-bus, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed
R11B DEVICE STATUS - does not auto increment	
VCS SIGNAL QUALITY	indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	if a good teletext signal is being received when logic 1
ROM VER R0 to R4	indicated language/ROM variant. For Western European = 11 000
$\overline{625}$/525 SYNC	if the input video is a 525 line signal when logic 1

Note

1. These functions have IN and OUT referring to inside and outside the boxing function respectively.

Table 9 Register map for page requests (R3); notes 1 to 5

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE page tens	PT3	PT2	PT1	PT0
2	DO CARE page units	PU3	PU2	PU1	PU0
3	DO CARE hours tens	X	X	HT1	HT0
4	DO CARE hours units	HU3	HU2	HU1	HU0
5	DO CARE minutes tens	X	MT2	MT1	MT0
6	DO CARE minutes units	MU3	MU2	MU1	MU0

Notes

1. Abbreviations are as for Table 5 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, normal or timed page selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.
5. X = don't care.

Table 10 Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option; notes 1 and 2

TCS ON FFB MODE	T1	T0	RESULT
X	0	0	interlaced 312.5/312.5 lines
X	0	1	non-interlaced 312/313 lines (note 1)
X	1	0	non-interlaced 312/313 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.
2. X = Don't care.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

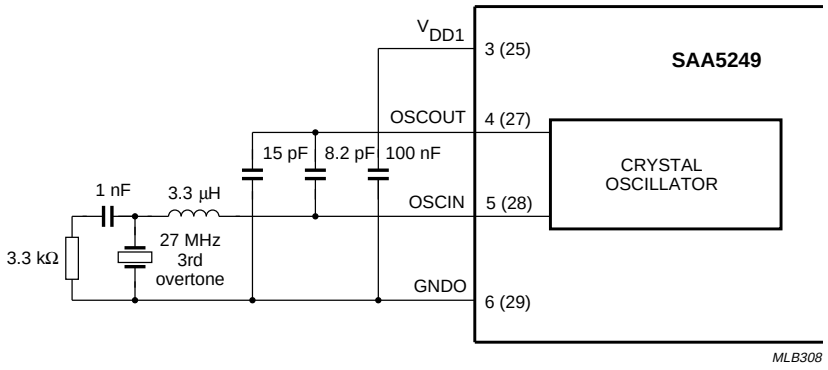


Fig.13 Crystal oscillator application diagram for SOT240-1; pins in parenthesis are for SOT319-1.

Table 11 Crystal characteristics (see Fig.13)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
R_r	resonance resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
X_a	ageing	–	–	±5	10^{-6}/year
X_j	adjustment tolerance	–	–	±25	10^{-6}
X_d	drift	–	–	±25	10^{-6}

CHARACTER SETS

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in the Tables 16, 17 and 18 with reference to their table position in the basic character matrix illustrated in Table 15. The IVT1.1BMCX automatically decodes transmission bits C12 to C14. Tables 12, 13 and 14 illustrate the character matrixes.

Character bytes are listed as transmitted from b1 to b7.

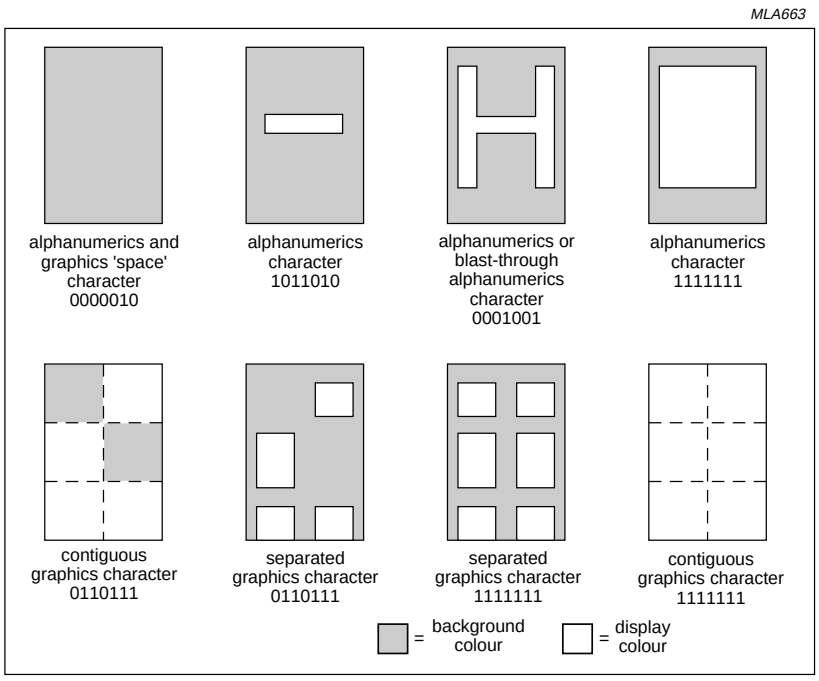


Fig.14 Character format.

Table 12 SAA5249P/E character data input decoding, West European languages; notes 1 to 9
For character version number (11000) see Register 11B.

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	0	1	1	1	1	1	1	1
b_7	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	1	1	1
b_6	0	0	1	1	1	0	0	0	1	1	1	1	0	0	1	0	1	1
b_5	0	1	0	1	1	0	1	1	0	0	1	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha - numerics black	graphics black															
0 0 0 1	1	alpha - numerics red	graphics red															
0 0 1 0	2	alpha - numerics green	graphics green															
0 0 1 1	3	alpha - numerics yellow	graphics yellow															
0 1 0 0	4	alpha - numerics blue	graphics blue															
0 1 0 1	5	alpha - numerics magenta	graphics magenta															
0 1 1 0	6	alpha - numerics cyan	graphics cyan															
0 1 1 1	7	alpha - numerics white (2)	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady (2)	contiguous graphics (2)															
1 0 1 0	10	end box (2)	separated graphics															
1 0 1 1	11	start box	ESC (1)															
1 1 0 0	12	normal height (2)	black back - ground (2)															
1 1 0 1	13	double height	new back - ground															
1 1 1 0	14	SO (1)	hold graphics															
1 1 1 1	15	SI (1)	release graphics (2)															

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Table 13 SAA5249P/H character data input decoding, West European languages; notes 1 to 9

For character version number (11001) see Register 11B.

BITS b_4 b_3 b_2 b_1	row	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
b_8		0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7		0	0	1	1	1	1	1	1	1		1		0	0	1	1	1	1
b_6		0	0	0	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5		0	1	0	0	0	0	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white (2)	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady (2)	contiguous graphics (2)																
1 0 1 0	10	end box (2)	separated graphics																
1 0 1 1	11	start box	ESC (1)																
1 1 0 0	12	normal height (2)	black back - ground (2)																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO (1)	hold graphics																
1 1 1 1	15	SI (1)	release graphics (2)																

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Table 14 SAA5249P/T character data input decoding, West European and Turkish languages; notes 1 to 9
For character version number (11010) see Register 11B.

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	0	1	1	1	1	1	1	1
b_7	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	1	1	1
b_5	0	1	0	1	1	1	0	1	0	1	1	1	0	0	0	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column / row	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white (2)	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady (2)	contiguous graphics (2)																
1 0 1 0	10	end box (2)	separated graphics																
1 0 1 1	11	start box	ESC (1)																
1 1 0 0	12	normal height (2)	black back - ground (2)																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO (1)	hold graphics																
1 1 1 1	15	SI (1)	release graphics (2)																

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Table 15 SAA5249P/R character data input decoding, Baltic and Cyrillic languages; notes 1 to 9

For character version number (11101) see Register 11B.

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	1	1	1	1
b_7				0	0	0	1	1	1	1	1	1	1	1	0	0	0	1	1
b_6				0	0	1	0	1	1	0	1	1	1	1	0	0	1	0	1
b_5				0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
b_4	b_3	b_2	b_1	column / row	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	1	1	alpha - numerics red	graphics red																
0	0	1	0	2	alpha - numerics green	graphics green																
0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	1	0	0	4	alpha - numerics blue	graphics blue																
0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	1	1	1	7	alpha - numerics white (2)	graphics white																
1	0	0	0	8	flash	conceal display																
1	0	0	1	9	steady (2)	contiguous graphics (2)																
1	0	1	0	10	end box (2)	separated graphics																
1	0	1	1	11	start box	TWIST																
1	1	0	0	12	normal height (2)	black back - ground (2)																
1	1	0	1	13	double height	new back - ground																
1	1	1	0	14	SO (1)	hold graphics																
1	1	1	1	15	SI (1)	release graphics (2)																

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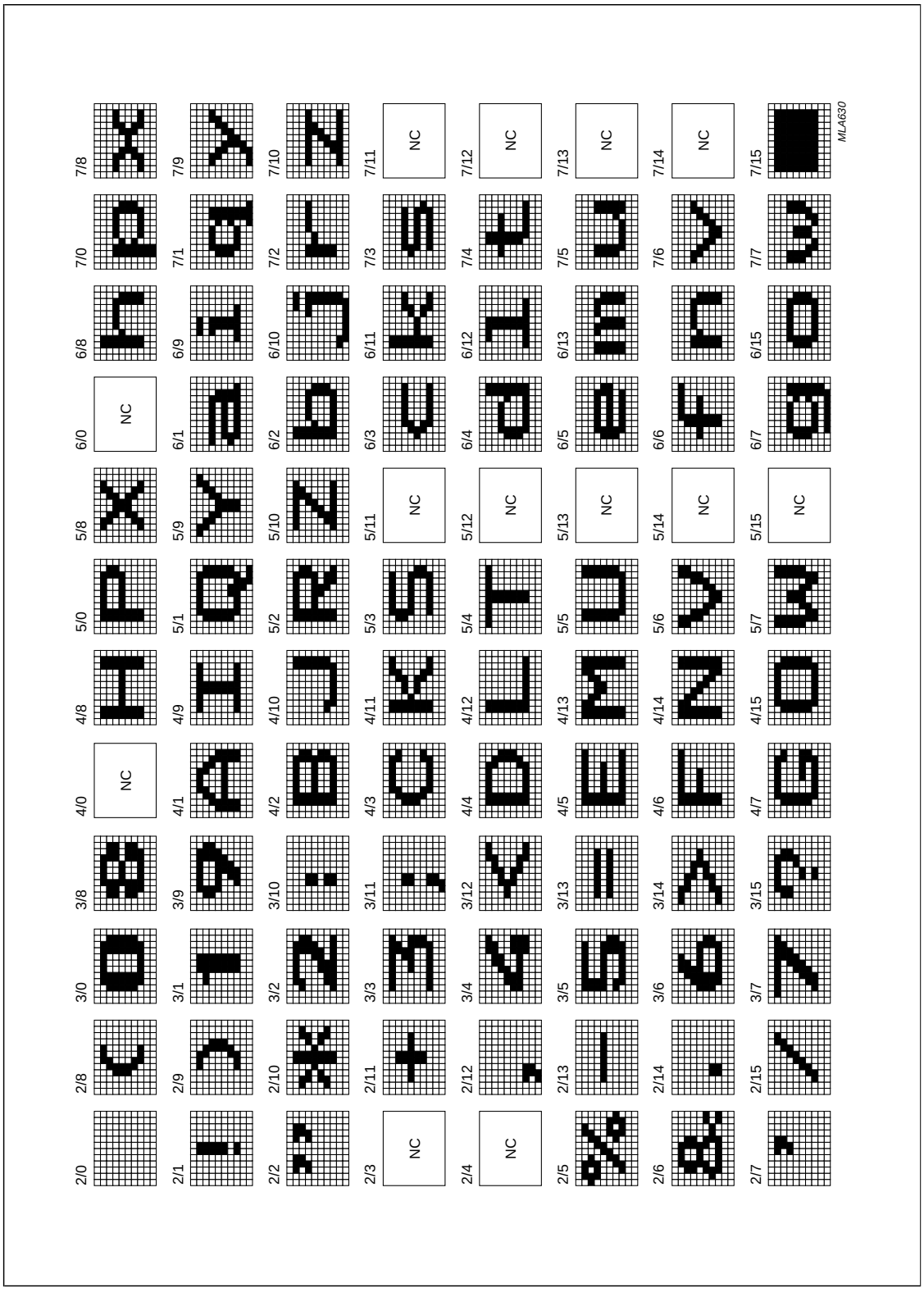
Notes to Tables 12, 13, 14 and 15

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.
3. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
4. Characters may be referred to by column and row (for example 2/5 refers to %).
5. Black represents displayed colour. White represents background.
6. The SAA5249 national option characters are illustrated in Tables 16, 17,18 and 19.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only).
8. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Tables 16, 17, 18 and 19.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 16 SAA5249 basic character matrix; note 1



Note

1. Where: NC = national option character position.

Table 17 SAA5249P/E national option character set; note 1

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

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Note

1. PHCB are the Page Header Control Bits. Other combinations default to English.

Table 18 SAA5249P/H national option character set; note 1

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ż	ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

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Note

1. PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 15.

Table 19 SAA5249P/R national option character set; note 1

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0													

	2	3	4	5	6	7
0		0	Ю	П	ю	п
1	!	1	А	Я	а	я
2	"	2	Б	Р	б	р
3	#	3	Ц	С	ц	с
4	$	4	Д	Т	д	т
5	%	5	Е	У	е	у
6	ы	6	Ф	Ж	ф	ж
7	'	7	Г	В	г	в
8	(	8	Х	Ь	х	ь
9	)	9	И	Ъ	и	ъ
10	*	:	Й	З	й	з
11	+	;	К	Ш	к	ш
12	,	<	Л	Э	л	э
13	−	=	М	Щ	м	щ
14	.	>	Н	Ч	н	ч
15	/	?	О	Ы	о	■

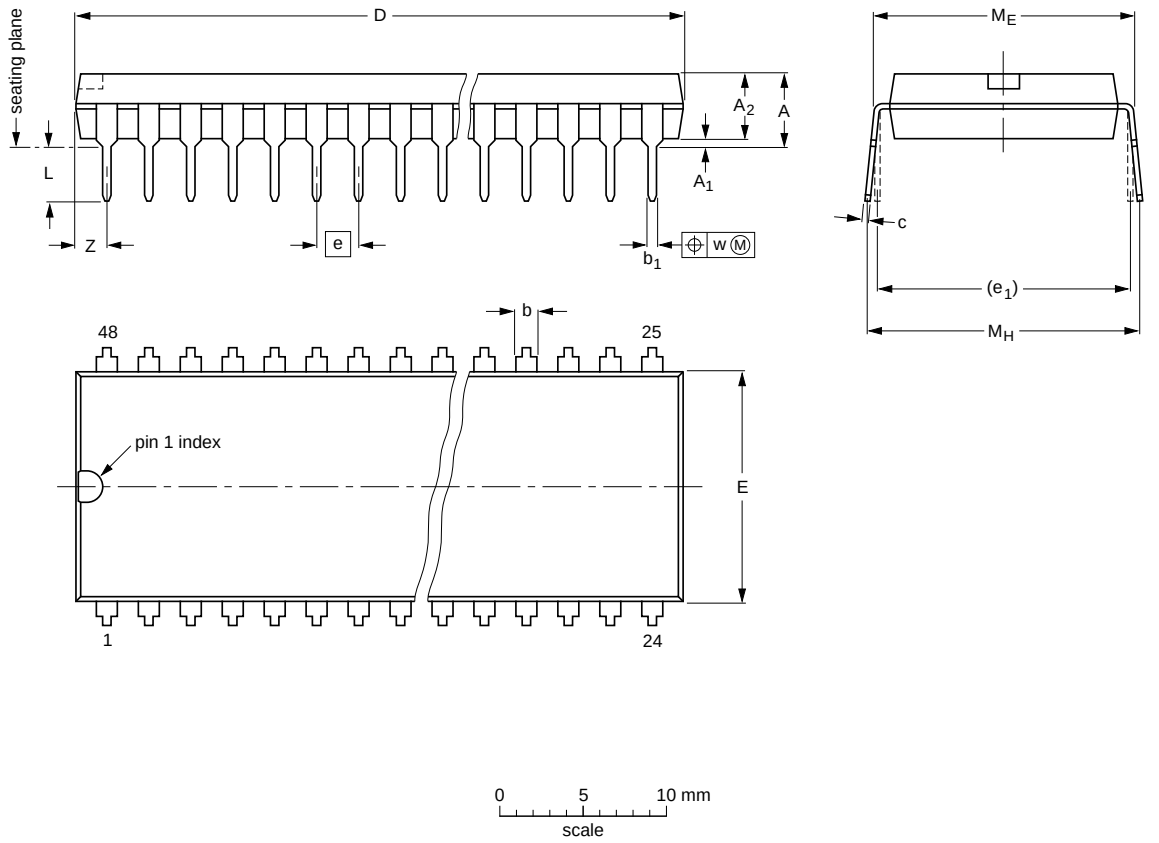
MEA597

Note

1. PHCB are the Page Header Control Bits. Other combinations default to Estonian.

PACKAGE OUTLINES

DIP48: plastic dual in-line package; 48 leads (600 mil) **SOT240-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

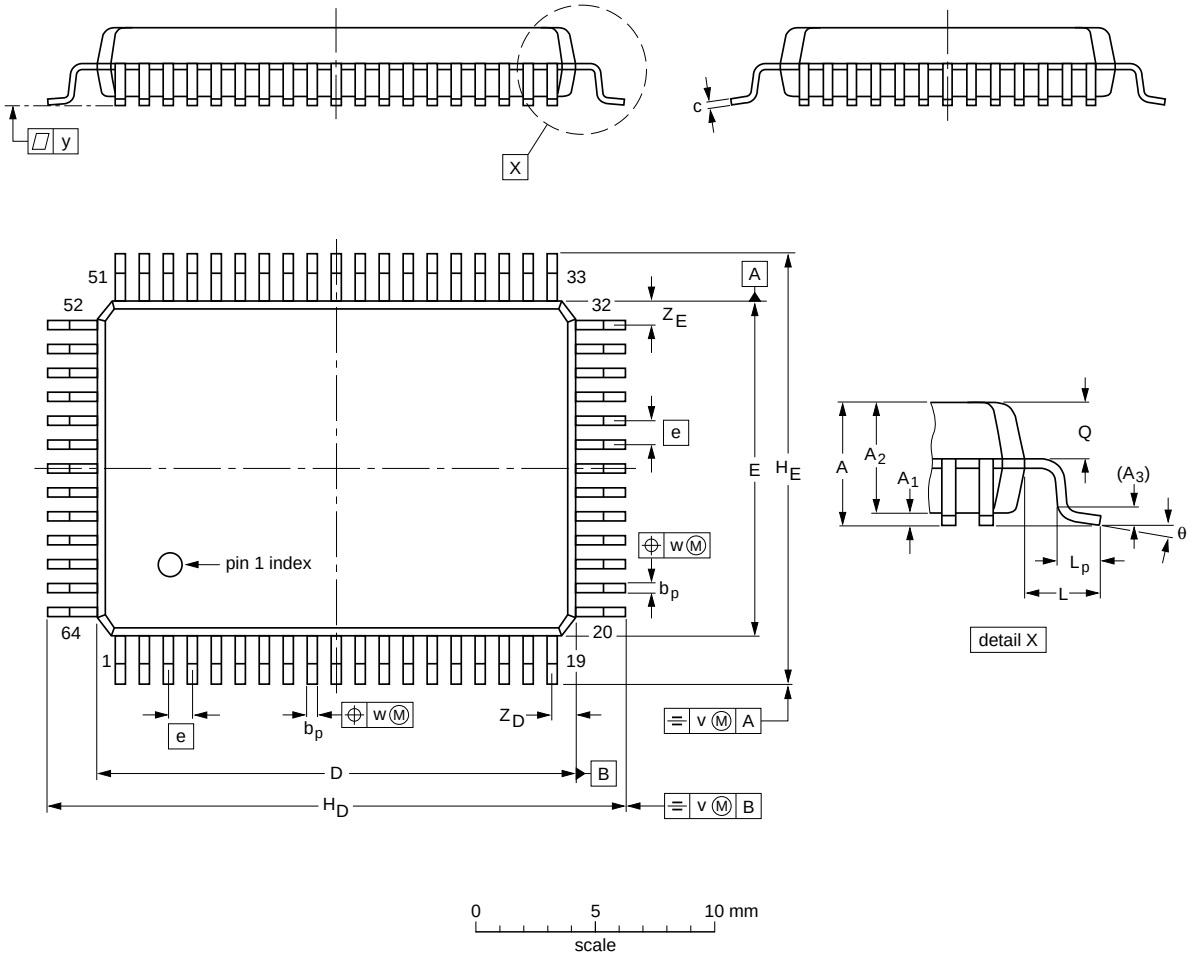
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

QFP64: plastic quad flat package;
64 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT319-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.50 0.35	0.25 0.13	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.43 1.23	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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