

3.3 V 64M x 64/72-Bit, 512MByte SDRAM Modules 168-pin Unbuffered DIMM Modules

- 168-pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications using 256Mbit technology.
- PC100-222, PC133-333 & PC133-222 versions
- Two bank 64M × 64 and 64M × 72 organization
- Optimized for byte-write non-parity and ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Programmed Latencies:

Product Speed		CL	t_{RCD}	t_{RP}
-7	PC133	2	2	2
-7.5	PC133	3	3	3
-8	PC100	2	2	2

- Single + 3.3 V (± 0.3 V) power supply
- Programmable \overline{CAS} Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs and outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- Uses Infineon 256 Mbit SDRAM components in 32M × 8 organization and TSOPII-54 packages
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- Gold contact pad, card size: 133.35 mm × 31.75 mm × 4.00 mm (JEDEC MO-161-BA)

- SDRAM Performance:

		-7	-7.5	-8	Unit
		PC133	PC133	PC100	
f_{CK}	Clock Frequency (max.)	133	133	100	MHz
t_{AC}	Clock Access time	5.4	5.4	6	ns

Description

The HYS 64V64220GU and HYS 72V64220GU are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 64M × 64 and 64M × 72 in two banks high speed memory arrays designed with 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use “-7” speed sorted 256 Mbit Synchronous DRAMs (SDRAMs) to meet the PC133-222 requirements, “-7.5” for PC133-333 and “-8” components for PC100-222 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's module specification. The DIMMs have a serial presence detect, implemented with a serial E²PROM using the 2-pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25“ (31.75 mm) height.

Ordering Information

Type	Code	Package	Descriptions	Module Height
HYS 64V64220GU-7-D	PC133-222-520	L-DIM-168-30	PC133 64M × 64 2 bank SDRAM module	1.25"
HYS 72V64220GU-7-D	PC133-222-520	L-DIM-168-30	PC133 64M × 72 2 bank SDRAM module	1.25"
HYS 64V64220GU-7.5-C2 HYS 64V64220GU-7.5-D	PC133-333-520	L-DIM-168-30	PC133 64M × 64 2 bank SDRAM module	1.25"
HYS 72V64220GU-7.5-C2 HYS 72V64220GU-7.5-D	PC133-333-520	L-DIM-168-30	PC133 64M × 72 2 bank SDRAM module	1.25"
HYS 64V64220GU-8-C2	PC100-222-620	L-DIM-168-30	PC100 64M × 64 2 bank SDRAM module	1.25"
HYS 72V64220GU-8-C2	PC100-222-620	L-DIM-168-30	PC100 64M × 72 2 bank SDRAM module	1.25"

Note: All part numbers end with a place code, designating the die revision. Consult factory for current revision. Example: HYS 64V64220GU-8-C2, indicating Rev.C2 dies are used for SDRAM components.

zeros in parentheses are for the x72 ECC versions; example: Pn 106 = (C85)

Pin Definitions and Functions

A0 - A12	Address Inputs	CLK0 - CLK3	Clock Input
BA0, BA1	Bank Selects	DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output	$\overline{CS0} - \overline{CS3}$	Chip Select
CB0 - CB7	Check Bits (x72 organization only)	V_{DD}	Power (+ 3.3 V)
\overline{RAS}	Row Address Strobe	V_{SS}	Ground
\overline{CAS}	Column Address Strobe	SCL	Clock for Presence Detect
\overline{WE}	Read/Write Input	SDA	Serial Data Out for Presence Detect
CKE0, CKE1	Clock Enable	N.C./DU	No Connection

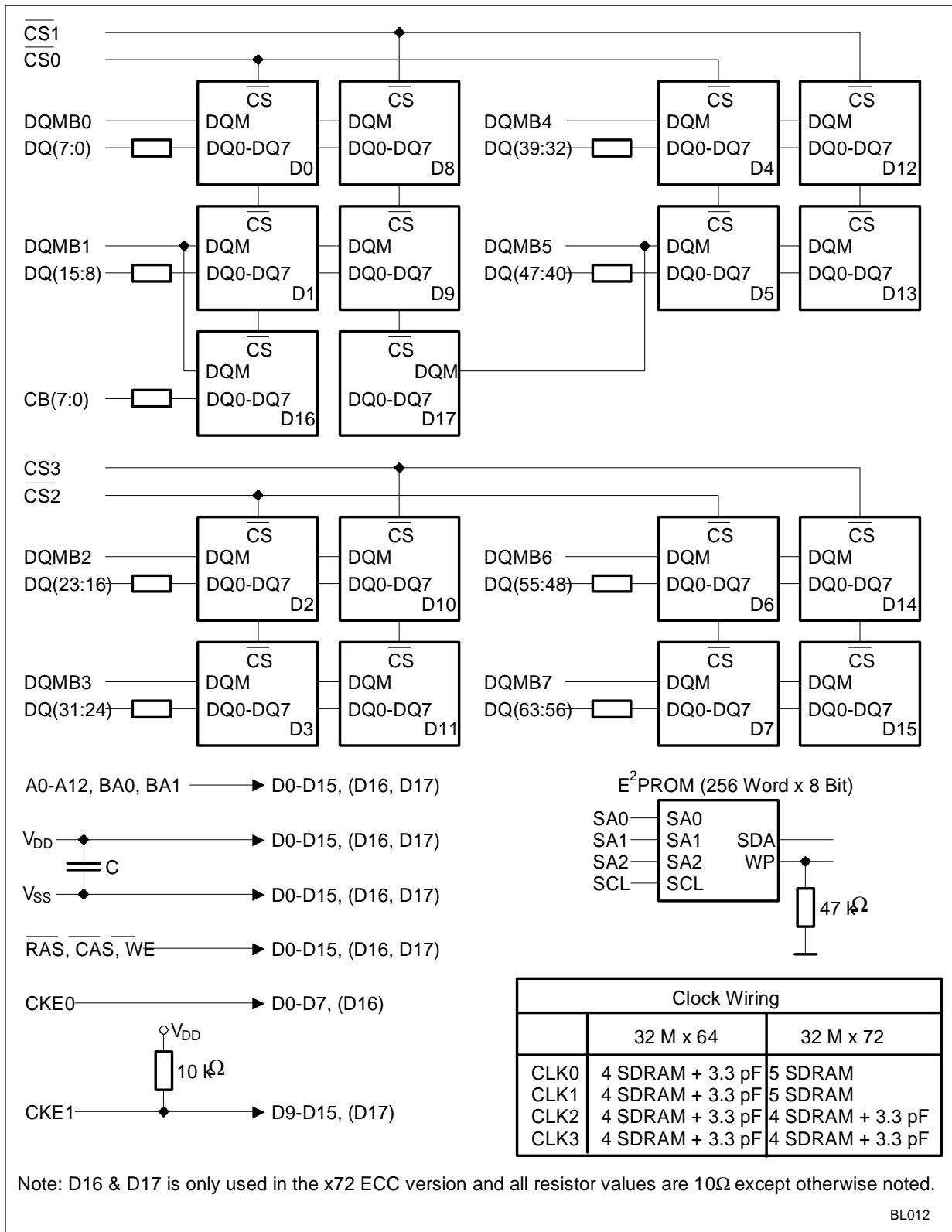
Address Format

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
64M × 64/72	HYS64/72V64220GU	13	10	2	8k	64 ms	7.8 μs

Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V _{DD}	48	DU	90	V _{DD}	132	N.C.
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	N.C. (CB2)	94	DQ39	136	CB6
11	DQ8	53	N.C. (CB3)	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	N.C. (CB0)	63	CKE1	105	N.C. (CB4)	147	N.C.
22	N.C. (CB1)	64	V _{SS}	106	N.C. (CB5)	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	CS1	156	DQ59
31	DU	73	V _{DD}	115	RAS	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V _{DD}	126	A12	168	V _{DD}

Note: Pin names in parentheses are for the x72 ECC versions



Block Diagram: 64M x 64/72 Two Bank SDRAM DIMM Modules

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	- 1.0	4.6	V
Power supply voltage on V_{DD}	V_{DD}	- 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation per SDRAM component	P_D	-	1	W
Data out current (short circuit)	I_{OS}	-	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
 Functional operation should be restricted to recommended operation conditions.
 Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	- 0.5	0.8	V
Output High Voltage ($I_{OUT} = - 4.0$ mA)	V_{OH}	2.4	-	V
Output Low Voltage ($I_{OUT} = 4.0$ mA)	V_{OL}	-	0.4	V
Input Leakage Current, any input (0 V < $V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	- 40	40	μ A
Output Leakage Current (DQ is disabled, 0 V < $V_{OUT} < V_{DD}$)	$I_{O(L)}$	- 40	40	μ A

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		max. 64M \times 64	max. 64M \times 72	
Input Capacitance (A0 to A11, BA0, BA1, \overline{RAS} , \overline{CAS} , \overline{WE})	C_{I1}	105	144	pF
Input Capacitance ($\overline{CS0} - \overline{CS3}$)	C_{I2}	32	40	pF
Input Capacitance (CLK0 - CLK3)	C_{ICL}	40	43	pF
Input Capacitance (CKE0, CKE1)	C_{I3}	65	72	pF
Input Capacitance (DQMB0 - DQMB7)	C_{I4}	20	25	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	17	17	pF
Input Capacitance (SCL, SA0-2)	C_{SC}	8	8	pF
Input/Output Capacitance	C_{SD}	8	8	pF

Operating Currents per SDRAM Component
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

Parameter	Test Condition	Symbol	-7/ -7.5	-8	Unit	Note
			max.			
Operating current $t_{RC} = t_{RC(MIN.)}$; $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	230	170	mA	1, 2
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, $CKE \leq V_{IL(MAX.)}$	$t_{CK} = \text{min.}$	I_{CC2P}	2	2	mA	1, 2
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, $CKE \geq V_{IH(MIN.)}$	$t_{CK} = \text{min.}$	I_{CC2N}	40	30	mA	1, 2
No operating current $t_{CK} = \text{min.}$, $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	$CKE \geq V_{IH(MIN.)}$	I_{CC3N}	50	45	mA	1, 2
	$CKE \leq V_{IL(MAX.)}$	I_{CC3P}	10	10	mA	1, 2
Burst operating current $t_{CK} = \text{min.}$, Read command cycling	–	I_{CC4}	150	100	mA	1,2,3
Auto refresh current $t_{CK} = \text{min.}$, Auto Refresh command cycling	–	I_{CC5}	240	220	mA	1, 2
Self refresh current Self Refresh Mode, $CKE = 0.2 \text{ V}$		I_{CC6}	3	3	mA	1

Notes

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 133 MHz operation frequency for -7 & -7.5 and at 100 MHz for -8 modules.
Input signals are changed once during t_{CK} , excepts for I_{CC6} and for stand-by currents when $t_{CK} = \text{infinity}$.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 are assumed and the data out current is excluded.

AC Characteristics ^{1), 2)}
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 1 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-7		-7.5		-8			
		PC133-222		PC133-333		PC100-222			
		min.	max.	min.	max.	min.	max.		

Clock

Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	t_{CK}	7.5	–	7.5	–	10	–	ns	–
		7.5	–	10	–	10	–	ns	
System Frequency $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	f_{CK}	–	133	–	133	–	100	MHz	–
		–	133	–	100	–	100	MHz	
Clock Access Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	t_{AC}	–	5.4	–	5.4	–	6	ns	3), 4)
		–	5.4	–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	2.5	–	3	–	ns	4)
Clock Low Pulse Width	t_{CL}	2.5	–	2.5	–	3	–	ns	4)

Setup and Hold Times

Input Setup Time	t_{CS}	1.5	–	1.5	–	2	–	ns	5)
Input Hold Time	t_{CH}	0.8	–	0.8	–	1	–	ns	5)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	–	1	CLK	6)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	1	–	CLK	7)
Mode Register Setup Time	t_{RSC}	2	–	2	–	2	–	CLK	
Transition Time (rise and fall)	t_{T}	1	–	1	–	1	–	ns	–

Common Parameters

RAS to $\overline{\text{CAS}}$ Delay	t_{RCD}	15	–	20	–	20	–	ns	–
Precharge Time	t_{RP}	15	–	20	–	20	–	ns	–
Active Command Period	t_{RAS}	42	–	45	100k	50	100k	ns	–
Cycle Time	t_{RC}	60	–	67.5	–	70	–	ns	–
Bank to Bank Delay Time	t_{RRD}	14	–	15	–	16	–	ns	–
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (same bank)	t_{CCD}	1	–	1	–	1	–	CLK	–

AC Characteristics (cont'd) ^{1), 2)}
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 1 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.	min.	max.		

Refresh Cycle

Refresh Period (8192 cycles)	t_{REF}	64	–	–	64	–	64	ms	⁶⁾
Self Refresh Exit Time	t_{SREX}	–	1	1	–	1	–	CLK	⁸⁾

Read Cycle

Data Out Hold Time	t_{OH}	3	–	3	–	3	–	ns	²⁾
Data Out to Low Impedance	t_{LZ}	0	–	0	–	0	–	ns	–
Data Out to High Impedance	t_{HZ}	3	7	3	7	3	8	ns	⁹⁾
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	–

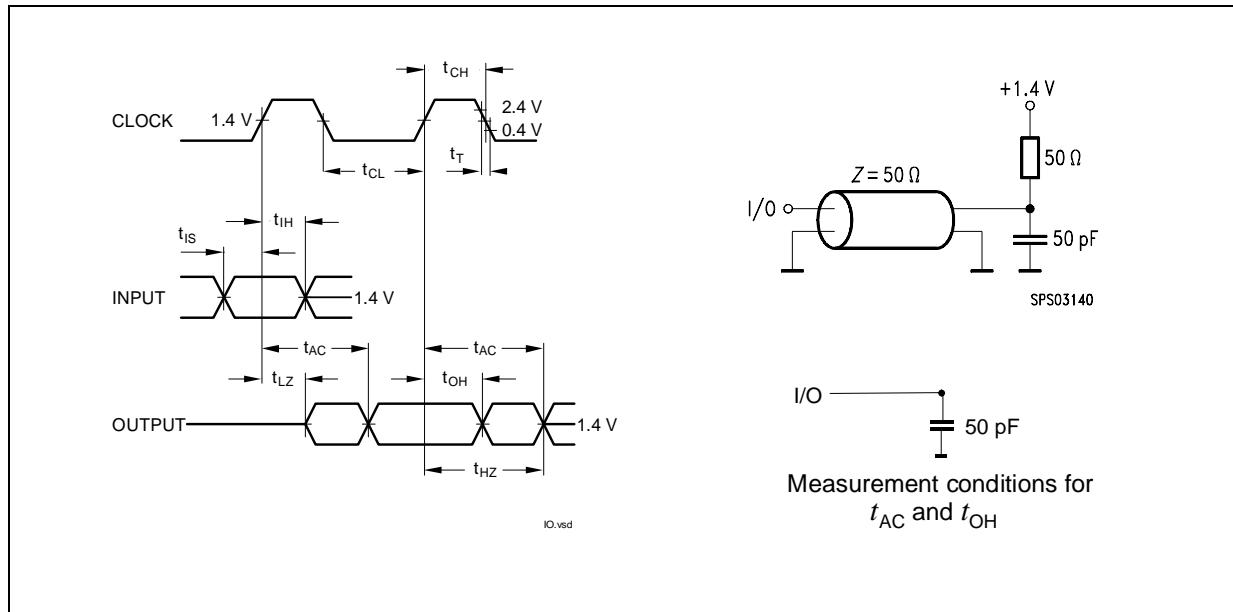
Write Cycle

Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	–

Notes

- All AC characteristics are shown on SDRAM component level.
An initial pause of 100 μs is required after power-up, then a Precharge All Banks command must be given followed by eight Auto-Refresh (CBR) cycles before the Mode Register Set Operation can begin.
- AC timing tests have $V_{IL} = 0.4 \text{ V}$ and $V_{IH} = 2.4 \text{ V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL} . All AC measurements assume $t_T = 1 \text{ ns}$ with the AC output load circuit show. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
- If clock rising time is longer than 1 ns, a time $(t_T/2 - 0.5)$ ns must be added to this parameter.
- Rated at 1.4 V
- If t_T is longer than 1 ns, a time $(t_T - 1)$ ns has to be added to this parameter.
- Anytime the Refresh Period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to “wake-up” the device.
- Timing is asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.

11. Self-Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self-Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
12. This is referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



Serial Presence Detect

A serial presence detect storage device - E²PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus).

SPD-Table for 64M x 64 (512 MByte non-ECC) Modules HYS64V64220GU

Byte #	Description	SPD Entry Value	Hex		
			64M x 64		
			-7	-7.5	-8
0	Number of SPD Bytes	128	80		
1	Total Bytes in Serial PD	256	08		
2	Memory Type	SDRAM	04		
3	Number of Row Addresses	13	0D		
4	Number of Column Addresses	10	0A		
5	Number of DIMM Banks	2	02		
6	Module Data Width	64	40		
7	Module Data Width (cont'd)	0	00		
8	Module Interface Levels	LVTTL	01		
9	SDRAM Cycle Time at CL = 3	7.5 / 10 ns	75	75	A0
10	Access Time from Clock at CL = 3	5.4 / 6 ns	54	54	60
11	DIMM Config	non-ECC	00		
12	Refresh Rate/Type	Self-Refresh, 7.8 μ s	82		
13	SDRAM Width, Primary	x8	08		
14	Error Checking SDRAM Data Width	na	00		
15	Minimum Clock Delay for Back-to-Back Random Column Address	$t_{CCD} = 1$ CLK	01		
16	Burst Length Supported	1, 2, 4 & 8	0F		
17	Number of SDRAM Banks	4	04		
18	Supported CAS Latencies	CL = 2 & 3	06		
19	CS Latencies	CS latency = 0	01		
20	WE Latencies	Write latency = 0	01		
21	SDRAM DIMM Module Attributes	unbuffered	00		
22	SDRAM Device Attributes: General	V_{DD} tol +/- 10%	0E		
23	SDRAM Cycle Time at CL = 2	7.5 / 10.0 ns	75	A0	A0
24	Access Time from Clock for CL = 2	5.4 / 6.0 ns	54	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	00	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	00	FF	FF
27	Minimum Row Precharge Time	15 / 20 ns	0F	14	14
28	Minimum Row Active to Row Active Delay t_{RRD}	14 / 15 / 16 ns	0E	0F	10
29	Minimum RAS to CAS Delay t_{RCD}	15 / 20 ns	0F	14	14
30	Minimum RAS Pulse Width t_{RAS}	42 / 45 / 50 ns	2A	2D	32
31	Module Bank Density (per bank)	256 MByte	40		
32	SDRAM Input Setup Time	1.5 / 2.0 ns	15	15	20
33	SDRAM Input Hold Time	0.8 / 1.0 ns	08	08	10

SPD-Table for 64M x 64 (512 MByte non-ECC) Modules HYS64V64220GU

Byte #	Description	SPD Entry Value	Hex		
			64M x 64		
			-7	-7.5	-8
34	SDRAM Data Input Hold Time	1.5 / 2.0 ns	15	15	20
35	SDRAM Data Input Setup Time	0.8 / 1.0 ns	08	08	10
36-61	Superset Information	–	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12
63	Checksum for Bytes 0 - 62	–	F4	37	9A
64	Manufacturers JEDEC ID Code	–	C1		
65-71	Manufacturer		INFINEON(N)		
72	Module Assembly Location				
73-90	Module Part Number				
91-92	Module Revision Code				
93-94	Module Manufacturing Code				
95-98	Module Serial Number				
99-125	Superset Information				
126	Frequency Specification		64	64	64
127	100 MHz Support Details	–	FF	FF	FF
128+	Unused Storage Locations	–	FF	FF	FF

SPD-Table for 64M x 72 (512 MByte ECC) Modules HYS72V64220GU

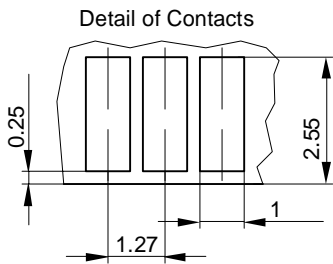
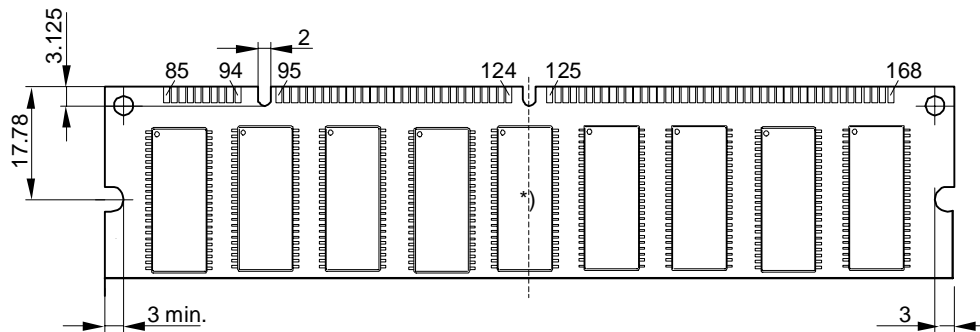
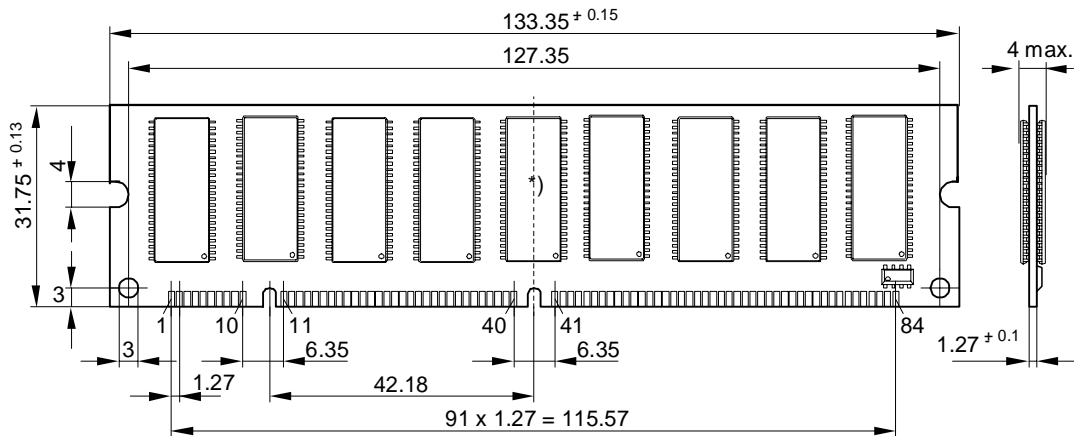
Byte#	Description	SPD Entry Value	Hex		
			64M x 72		
			-7	-7.5	-8
0	Number of SPD Bytes	128	80		
1	Total Bytes in Serial PD	256	08		
2	Memory Type	SDRAM	04		
3	Number of Row Addresses	13	0D		
4	Number of Column Addresses	10	0A		
5	Number of DIMM Banks	2	02		
6	Module Data Width	72	48		
7	Module Data Width (cont'd)	0	00		
8	Module Interface Levels	LVTTL	01		
9	SDRAM Cycle Time at CL = 3	7.5 / 10 ns	75	75	A0
10	Access Time from Clock at CL = 3	5.4 / 6 ns	54	54	60
11	DIMM Config	ECC	02		
12	Refresh Rate/Type	Self-Refresh, 7.8 μ s	82		
13	SDRAM Width, Primary	x8	08		
14	Error Checking SDRAM Data Width	x8	08		
15	Minimum Clock Delay for Back-to-Back Random Column Address	$t_{CCD} = 1$ CLK	01		
16	Burst Length Supported	1, 2, 4 & 8	0F		
17	Number of SDRAM Banks	4	04		
18	Supported CAS Latencies	CL = 2 & 3	06		
19	CS Latencies	CS latency = 0	01		
20	WE Latencies	Write latency = 0	01		
21	SDRAM DIMM Module Attributes	unbuffered	00		
22	SDRAM Device Attributes: General	V_{DD} tol +/- 10%	0E		
23	SDRAM Cycle Time at CL = 2	7.5 / 10.0 ns	75	A0	A0
24	Access Time from Clock for CL = 2	5.4 / 6.0 ns	54	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	00	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	00	FF	FF
27	Minimum Row Precharge Time	15 / 20 ns	0F	14	14
28	Minimum Row Active to Row Active Delay t_{RRD}	14 / 15 / 16 ns	0E	0F	10
29	Minimum RAS to CAS Delay t_{RCD}	15 / 20 ns	0F	14	14
30	Minimum RAS Pulse Width t_{RAS}	42 / 45 / 50 ns	2A	2D	32
31	Module Bank Density (per bank)	256 MByte	40		
32	SDRAM Input Setup Time	1.5 / 2.0 ns	15	15	20
33	SDRAM Input Hold Time	0.8 / 1.0 ns	08	08	10

SPD-Table for 64M x 72 (512 MByte ECC) Modules HYS72V64220GU

Byte#	Description	SPD Entry Value	Hex		
			64M x 72		
			-7	-7.5	-8
34	SDRAM Data Input Hold Time	1.5 / 2.0 ns	15	15	20
35	SDRAM Data Input Setup Time	0.8 / 1.0 ns	08	08	10
36-61	Superset Information	–	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12
63	Checksum for Bytes 0 - 62	–	06	49	AC
64	Manufacturers JEDEC ID Code	–	C1		
65-71	Manufacturer		INFINEO(N)		
72	Module Assembly Location				
73-90	Module Part Number				
91-92	Module Revision Code				
93-94	Module Manufacturing Code				
95-98	Module Serial Number				
99-125	Superset Information				
126	Frequency Specification		64	64	64
127	100 MHz Support Details	–	FF	FF	FF
128+	Unused Storage Locations	–	FF	FF	FF

Package Outlines

L-DIM-168-30 (JEDEC MO-161-BA)
SDRAM DIMM Module Package
HYS 64/72V64220GU



*) on ECC modules only

L-DIM-168-30

Note: All tolerances according to JEDEC standard

Change List:

14.1.1999	Input capacitances adjusted
18.4.1999	-8A speed sort added Infineon logo added SPD codes updated according to new 256M speedsorts
12.5.99	Some ICC current values changed due to new inputs
3.8.99	PC133 merged into this datasheet
23.8.99	Byte 126 changed to 64h for PC133 modules
6.9.99	Template from R&L
20.10.99	CL=2 max. frequency changed to 83 Mhz for -7.5 modules
2.12.99	Some timing parameters adjusted according to INTELs PC133 specification
20.1.2000	Capacitance values for x72 adjusted (new measurements)
10.3.2000	Implemented differences between 256Mbit S20 and S17 PC133 modules 256Mbit S20 based PC133 modules are backward compatible to PC100 3-2-2 256Mbit S17 based modules are backwards compatible to PC100-2-2-2 leading to changes in SPD code of bytes 23, 63 (checksum) and 126 TPCR issued
10.5.2000	Reference to JEDEC MO-161-BA added
5.03.2001	-8A and -8B speed sorts removed PC133 timing parameters only for 256M S17 and later versions References to 256M S20 removed ICC currents according to 256M S17 datasheet
24.07.2001	256M S14 based modules added -7 speed sort added for 256M S14 modules
06.09.2001	SCR : Absolute Maximum Ratings table added