SIEMENS

3.3V 1M x 64-Bit SDRAM Module — HYS64V1000GS-10/-12/-15
3.3V 1M x 72-Bit SDRAM Module — HYS72V1000GS-10/-12/-15

168 pin unbuffered DIMM Modules

Target Information

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual-In-Line SDRAM Module
- 1 bank 1M x 64, 1M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Performance:

		-10	-12	-15	Units
f_{CK}	Clock frequency	100	83	66	MHz
t_{CK3}	Clock cycle time	10	12	15	ns
t_{AC3}	Clock access time $\overline{\text{CAS}}$ latency = 3	9	11	13	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial presence detects
- Utilizes four / five 1M x 16 SDRAMs in TSOPII-50 packages
- 4096 refresh cycles every 64 ms
- Gold contact pad
- Card Size: 133,35mm x 25,40mm x 3,00 mm
- This SDRAM product familiy is intended to be fully pin and architecture compatible with the 168 pin Unbuffered DRAM DIMM module family.

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The HYS64(72)V1000GS-10/-12/-15 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 1M x 64 and 1M x 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use four 1M x 16 SDRAMs for the 1M x 64 organisation and an additional SDRAM for the 1M x 72 organisation. Decoupling capacitors are mounted on the PC board.

The DIMMs use optional serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYS 64V1000GU-50		L-DIM-168-15	100 Mhz 1M x 64 SDRAM module
HYS 64V1000GU-60		L-DIM-168-15	83 Mhz 1M x 64 SDRAM module
HYS 64V1000GU-70		L-DIM-168-15	66 MHz 1M x 64 SDRAM module
HYS 72V1000GU-50		L-DIM-168-15	100 MHz 1M x 72 SDRAM module
HYS 72V1000GU-50		L-DIM-168-15	83 Mhz 1M x 72 SDRAM module
HYS 72V1000GU-70		L-DIM-168-15	66 Mhz 1M x 72 SDRAM module

Pin Names

A0-A10	Address Inputs
A11 (BS)	Bank Select
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bits (x72 organisation only)
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Input
CKE	Clock Enable
CLK0 - CLK3	Clock Input
DQMB0 - DQMB7	Data Mask
CS0 - CS3	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

Address Format:

	Part Number	SDRAM banks	Rows	Columns	Refresh	Period	Interval
1M x 64	HYS 64V1000GS	2	11	8	4k	64 ms	15,6 µs
1M x 72	HYS 72V1000GS	2	11	8	4k	64 ms	15,6 µs

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Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	DU		86	DQ32	128	CKE
3	DQ1	45	CS2		87	DQ33	129	CS3
4	DQ2	46	DQMB2		88	DQ34	130	DQMB6
5	DQ3	47	DQMB3		89	DQ35	131	DQMB7
6	VCC	48	DU		90	VCC	132	NC
7	DQ4	49	VCC		91	DQ36	133	VCC
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	NC (CB2)		94	DQ39	136	CB6
11	DQ8	53	NC (CB3)		95	DQ40	137	CB7
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ16		97	DQ41	139	DQ48
14	DQ10	56	DQ17		98	DQ42	140	DQ49
15	DQ11	57	DQ18		99	DQ43	141	DQ50
16	DQ12	58	DQ19		100	DQ44	142	DQ51
17	DQ13	59	VCC		101	DQ45	143	VCC
18	VCC	60	DQ20		102	VCC	144	DQ52
19	DQ14	61	NC		103	DQ46	145	NC
20	DQ15	62	DU		104	DQ47	146	DU
21	NC (CB0)	63	NC		105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS		106	NC (CB5)	148	VSS
23	VSS	65	DQ21		107	VSS	149	DQ53
24	NC	66	DQ22		108	NC	150	DQ54
25	NC	67	DQ23		109	NC	151	DQ55
26	VCC	68	VSS		110	VCC	152	VSS
27	WE	69	DQ24		111	CAS	153	DQ56
28	DQMB0	70	DQ25		112	DQMB4	154	DQ57
29	DQMB1	71	DQ26		113	DQMB5	155	DQ58
30	CS0	72	DQ27		114	CS1	156	DQ59
31	DU	73	VCC		115	RAS	157	VCC
32	VSS	74	DQ28		116	VSS	158	DQ60
33	A0	75	DQ29		117	A1	159	DQ61
34	A2	76	DQ30		118	A3	160	DQ62
35	A4	77	DQ31		119	A5	161	DQ63
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	CLK2		121	A9	163	CLK3
38	A10	80	NC		122	A11=BS	164	NC
39	NC	81	NC		123	NC	165	SA0
40	VCC	82	SDA		124	VCC	166	SA1
41	VCC	83	SCL		125	CLK1	167	SA2
42	CLK0	84	VCC		126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions

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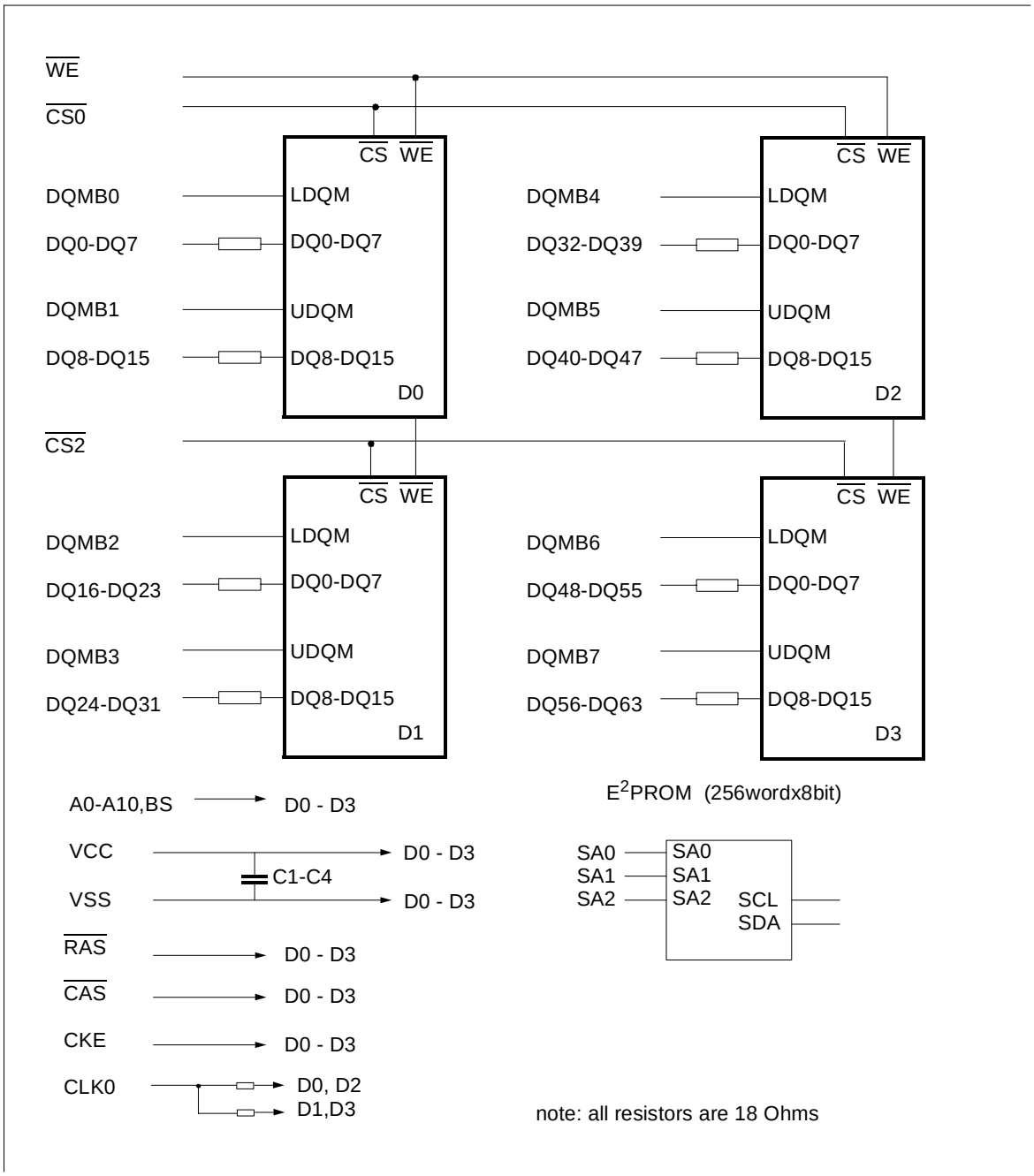

Block Diagram for 1M x 64 SDRAM DIMM module

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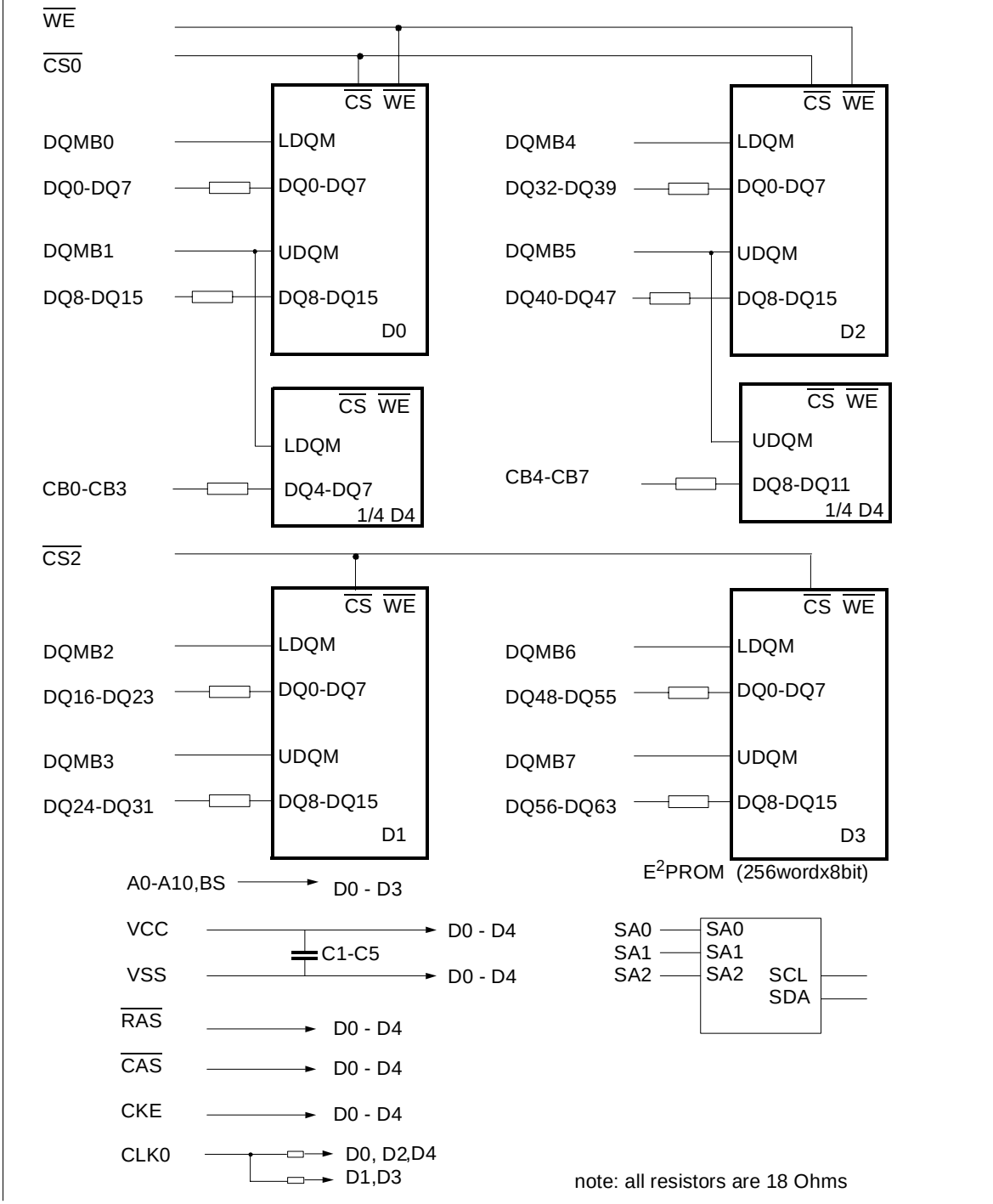

Block Diagram for 1M x 72 SDRAM - DIMM module

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DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA

Standby and Refresh Currents (T_a = 0 to 70°C, VCC = 3.3V ± 0.3V**)**

Parameter	Symbol	Test Condition	Speed Sort				Note
				X64	X72		
Precharged Standby Current in Power Down Mode	Icc1P	CKE=<VIL(max), tCK=15ns		12	15	mA	
	Icc1PS	CKE=<VIL(max), tCK=Infinity		8	10	mA	
Precharged Standby Current in Non-power Down Mode	Icc1N	CKE=>VIH(min), tCK=15ns Input Change in every 30ns		48	60	mA	
	Icc1NS	CKE=>VIH(min), tCK=Infinity No Input Change		24	30	mA	
Active Standby Current in Power Down Mode	Icc2P	CKE=<VIL(max), tCK=15ns		12	15	mA	
	Icc2PS	CKE=<VIL(max), tCK=Infinity		8	10	mA	
Active Standby Current in Non-power Down Mode	Icc2N	CKE=>VIH(min), tCK=15ns Input Change in every 30ns		64	80	mA	
	Icc2NS	CKE=>VIH(min),tCK=Infinity No Input Change		40	50	mA	
Refresh Current	Icc3	tRC=>tRC(min) $\overline{CAS}$ Latency = 3	-10 -12 -15	500 440 360	625 550 450	mA mA mA	
Self Refresh Current	Icc4	CKE=<0,2V		8	10	mA	
Operating Current	Icc5	tRC=tRC(min), tck>tck,min Io = 0mA CAS Latency=3,Burst = 4	-10 -12 -15	560 500 400	700 625 500	mA mA mA	

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Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS0}$, $\overline{CS2}$,CLK0, CKE, DQMB0-7)	C_{I2}	–	25	pF
Output capacitance (DQ0-DQ63,CB0-CB7)	C_{IO}	–	11	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	–	8	pF
Input/Output Capacitance	C_{sd}	–	10	pF

AC characteristics and waveforms

For AC characteristics, detailed function description and waveforms see the SDRAM datasheet HYB39S164/8/160T.

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Serial Presence Detect

A serial presence detect storage device - E^2PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I2C synchronous 2-wire bus)

Byte#	Description	SPD Entry Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex
0	Number of SPD bytes	128	1	0	0	0	0	0	0	0	80
1	Total bytes in Serial PD	256	0	0	0	0	1	0	0	0	08
2	Memory Type	SDRAM	0	0	0	0	0	1	0	0	04
3	Number of Row Addresses	12	0	0	0	0	1	1	0	0	0C
4	Number of Column Addresses	8	0	0	0	0	1	0	0	0	08
5	Number of DIMM Banks	1	0	0	0	0	0	0	0	1	01
6	Module Data Width	64	0	1	0	0	0	0	0	0	40
		72	0	1	0	0	1	0	0	0	48
7	Module Data Width (cont'd)	0	0	0	0	0	0	0	0	0	00
8	Module Interface Levels	LVTTL	0	0	0	0	0	0	0	1	01
9	SDRAM Cycle Time	10 ns	1	0	1	0	0	0	0	0	A0
		12 ns	1	1	0	0	0	0	0	0	C0
		15 ns	1	1	1	1	0	0	0	0	F0
10	SDRAM Access time from	9 ns	1	0	0	1	0	0	0	0	90
	Clock	11 ns	1	0	1	1	0	0	0	0	B0
		13 ns	1	1	0	1	0	0	0	0	D0
11	Dimm Config (Error Det/Corr.)	none	0	0	0	0	0	0	0	0	00
		ECC	0	0	0	0	0	0	1	0	02
12	Refresh Rate/Type	norrmal 15.6µs	0	0	0	0	0	0	0	0	00
13	SDRAM Module Attributes	*)									
14	SDRAM Device Attributes	*)									
15	SDRAM Device Attributes	*)									
16	Burst Length supported		1	0	0	0	1	1	1	1	
17	Number of SDRAM banks	2	0	0	0	0	0	0	0	0	01
18	Supported CAS Latencies		0	1	1	1	1	1	1	1	
19	CS Latencies	*)									
20	WE Latencies	*)									

note : *) not decided yet

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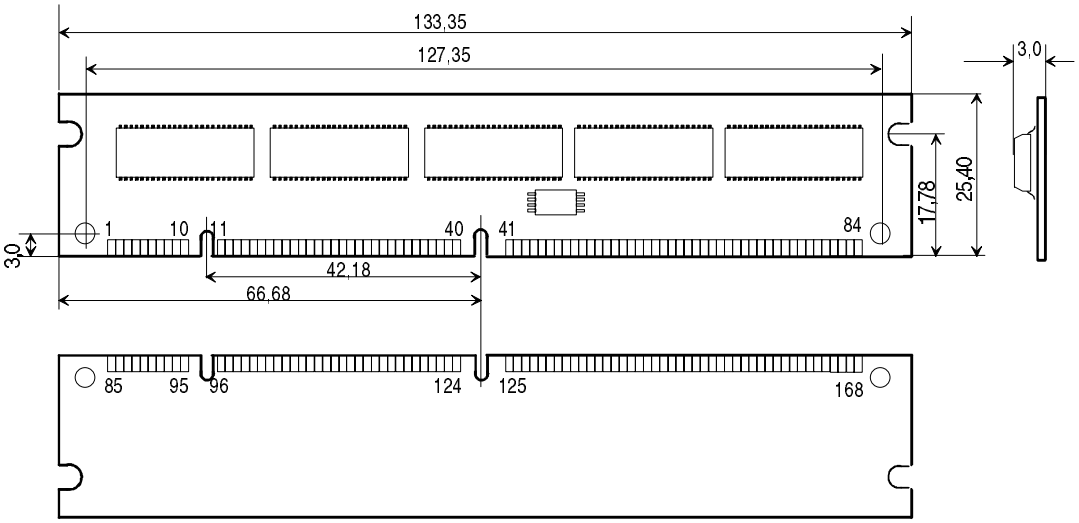
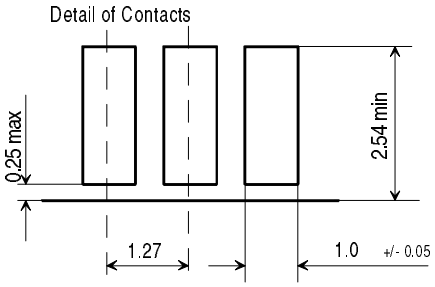
L-DIM-168-15
SDRAM DIMM Module package





DM168-15.WMF

preliminary drawing

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