

100-Pin TQFP
Commercial Temp
Industrial Temp

512K x 18, 256K x 32, 256K x 36
9Mb Sync Burst SRAMs

250 MHz–150 MHz
1.8 V or 2.5 V V_{DD}
1.8 V or 2.5 V I/O

Features

- \overline{FT} pin for user-configurable flow through or pipeline operation
- Dual Cycle Deselect (DCD) operation
- 1.8 V or 2.5 V +10%/–10% core power supply
- 1.8 V or 2.5 V I/O supply
- \overline{LBO} pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write (\overline{BW}) and/or Global Write (\overline{GW}) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package
- RoHS-compliant 100-lead TQFP package available

Functional Description

Applications

The GS880E18/32/36BT is a 9,437,184-bit (8,388,608-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$, $E2$, $\overline{E3}$), address burst control inputs (\overline{ADSP} , \overline{ADSC} , \overline{ADV}), and write control inputs (\overline{Bx} , \overline{BW} , \overline{GW}) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (\overline{G}) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either \overline{ADSP} or \overline{ADSC} inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by \overline{ADV} . The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order (\overline{LBO}) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the \overline{FT} mode pin (Pin 14). Holding the \overline{FT} mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding \overline{FT} high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

DCD Pipelined Reads

The GS880E18/32/36BT is a DCD (Dual Cycle Deselect) pipelined synchronous SRAM. SCD (Single Cycle Deselect) versions are also available. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (\overline{BW}) input combined with one or more individual byte write signals (\overline{Bx}). In addition, Global Write (\overline{GW}) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

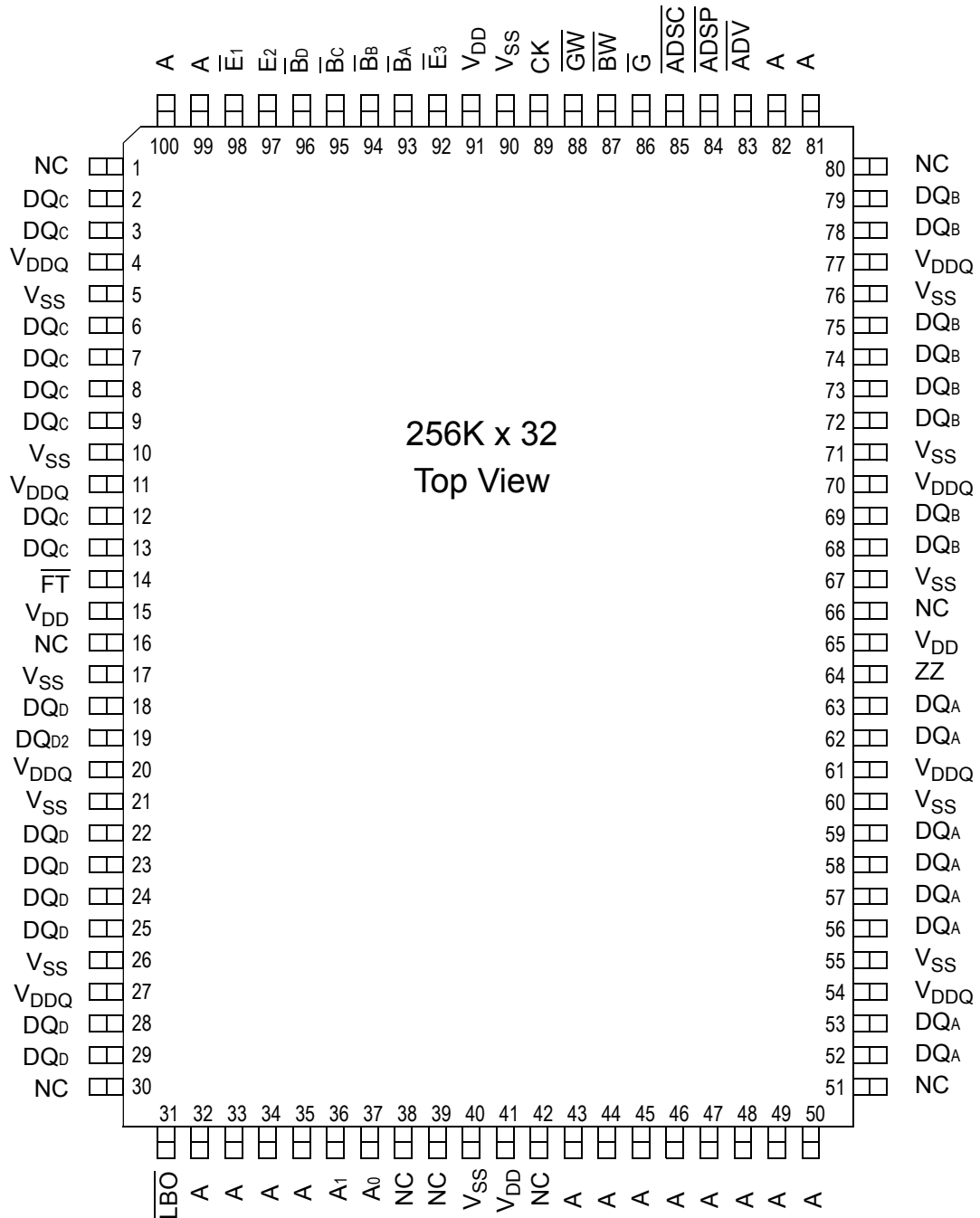
Core and Interface Voltages

The GS880E18/32/36BT operates on a 1.8 V or 2.5 V power supply. All input are 2.5 V and 1.8 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 2.5 V and 1.8 V compatible.

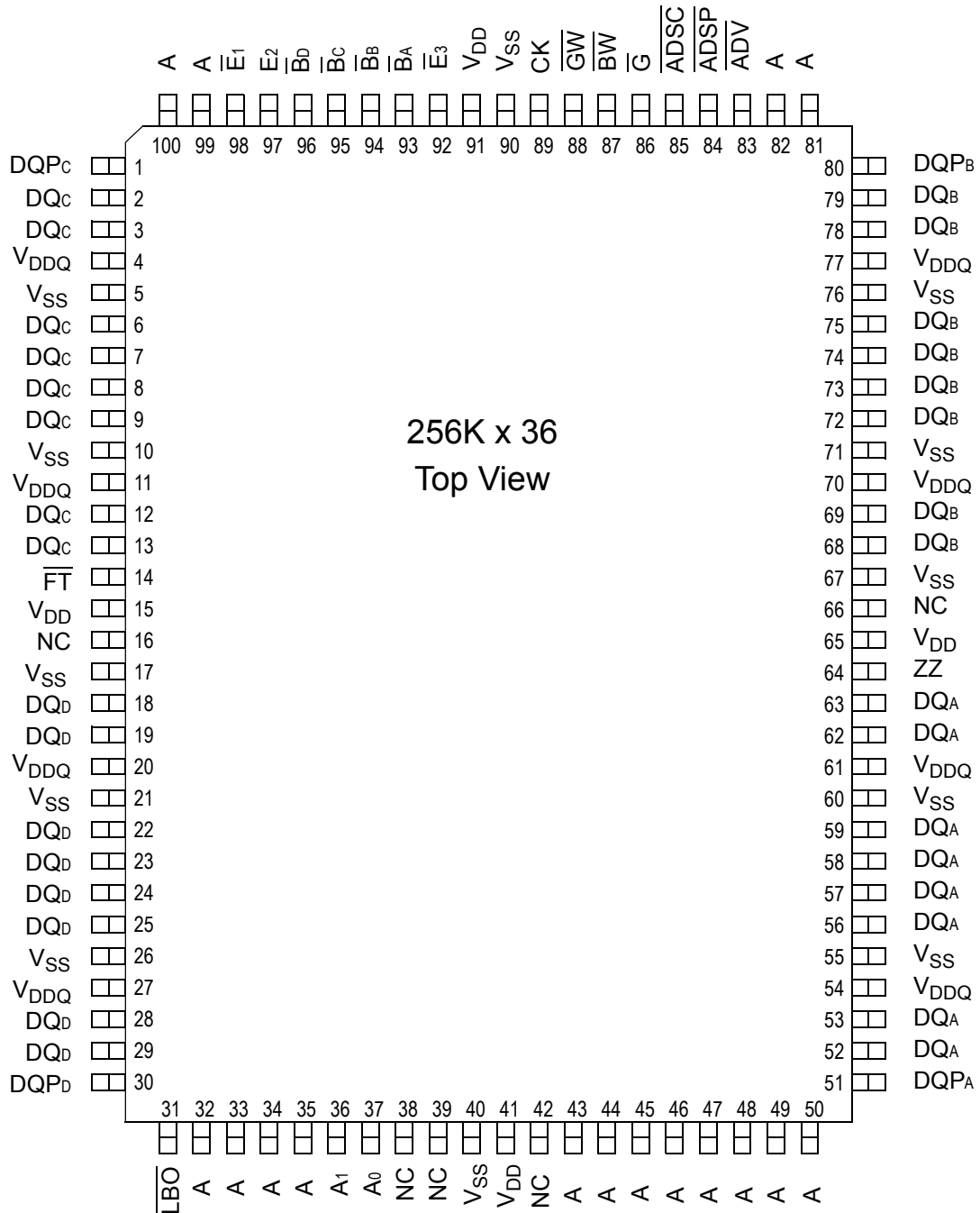
Parameter Synopsis

| | | -250 | -200 | -150 | Unit |
|-------------------------|----------------|------|------|------|------|
| Pipeline 3-1-1-1 | t_{kQ} | 3.0 | 3.0 | 3.8 | ns |
| | tCycle | 4.0 | 5.0 | 6.7 | ns |
| | Curr (x18) | 200 | 170 | 140 | mA |
| | Curr (x32/x36) | 230 | 195 | 160 | mA |
| Flow Through 2-1-1-1 | t_{kQ} | 5.5 | 6.5 | 7.5 | ns |
| | tCycle | 5.5 | 6.5 | 7.5 | ns |
| | Curr (x18) | 160 | 140 | 128 | mA |
| | Curr (x32/x36) | 185 | 160 | 145 | mA |

GS880E32BT-xxxV 100-Pin TQFP Pinout (Package T)



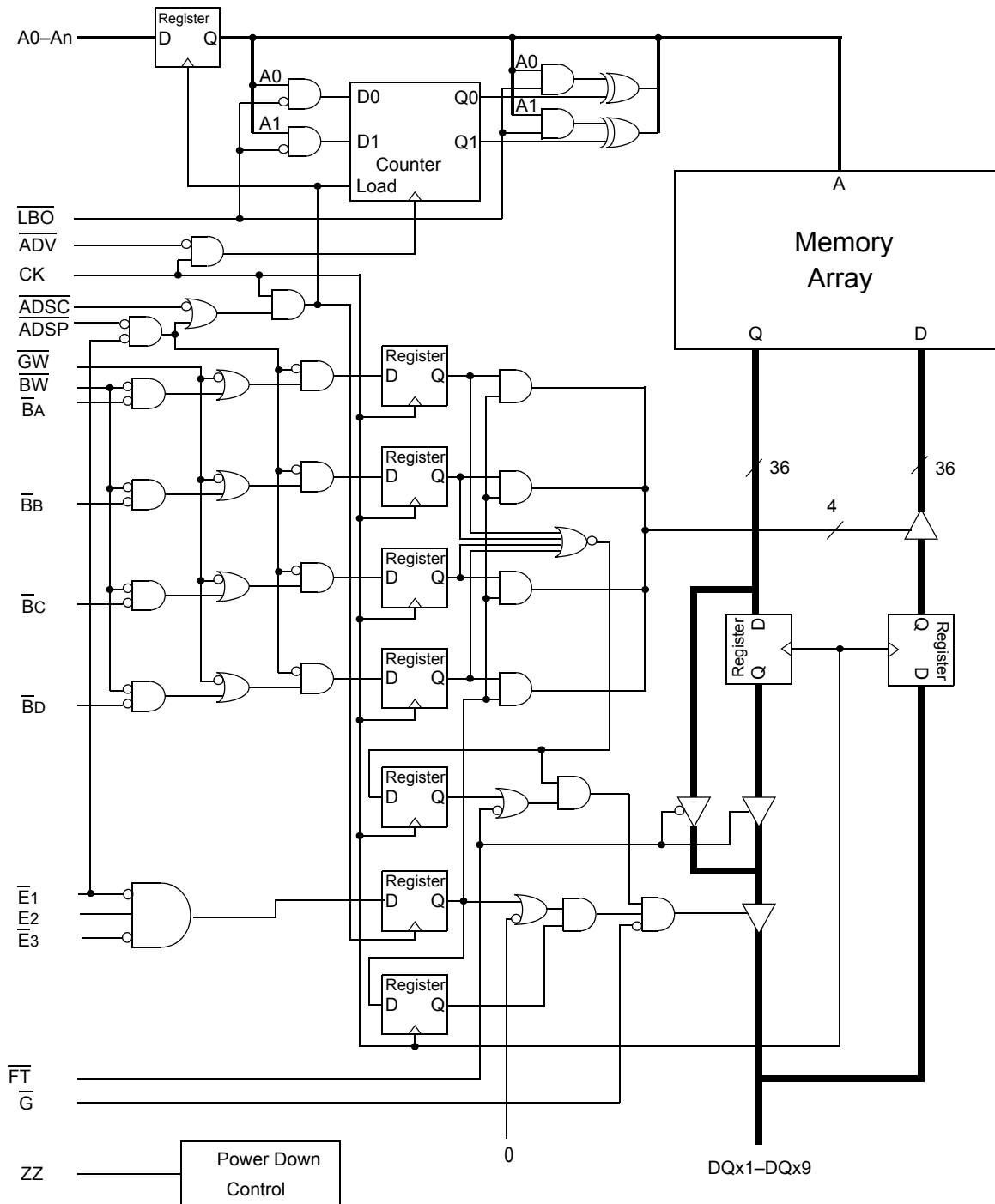
GS880E36BT-xxxV 100-Pin TQFP Pinout (Package T)



TQFP Pin Description

| Symbol | Type | Description |
|--------------------------------------------------------------------------|-------------|-------------------------------------------------------------------------------|
| A ₀ , A ₁ | I | Address field LSBs and Address Counter preset Inputs |
| A | I | Address Inputs |
| DQ _A DQ _B DQ _C DQ _D | I/O | Data Input and Output pins |
| NC | — | No Connect |
| $\overline{\text{BW}}$ | I | Byte Write—Writes all enabled bytes; active low |
| B _A , B _B , B _C , B _D | I | Byte Write Enable for DQ _A , DQ _B Data I/Os; active low |
| CK | I | Clock Input Signal; active high |
| $\overline{\text{GW}}$ | I | Global Write Enable—Writes all bytes; active low |
| $\overline{\text{E}}_1$, E ₃ | I | Chip Enable; active low |
| E ₂ | I | Chip Enable; active high |
| $\overline{\text{G}}$ | I | Output Enable; active low |
| $\overline{\text{ADV}}$ | I | Burst address counter advance enable; active low |
| $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ | I | Address Strobe (Processor, Cache Controller); active low |
| ZZ | I | Sleep Mode control; active high |
| $\overline{\text{FT}}$ | I | Flow Through or Pipeline mode; active low |
| LBO | I | Linear Burst Order mode; active low |
| V _{DD} | I | Core power supply |
| V _{SS} | I | I/O and Core Ground |
| V _{DDQ} | I | Output driver power supply |

GS880E18/32/36BT-xxxV Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

| Mode Name | Pin Name | State | Function |
|------------------------------------|-------------------------|---------|----------------------------|
| Burst Order Control | $\overline{\text{LBO}}$ | L | Linear Burst |
| | | H | Interleaved Burst |
| Output Register Control | $\overline{\text{FT}}$ | L | Flow Through |
| | | H or NC | Pipeline |
| Power Down Control | ZZ | L or NC | Active |
| | | H | Standby, $I_{DD} = I_{SB}$ |
| Single/Dual Cycle Deselect Control | SCD | L | Dual Cycle Deselect |
| | | H or NC | Single Cycle Deselect |
| FLXDrive Output Impedance Control | ZQ | L | High Drive (Low Impedance) |
| | | H or NC | Low Drive (High Impedance) |

Note:

There is a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above table.

There is a pull-up device on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above table.

There is a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above table.

There are pull-up devices on the ZQ, and SCD, and $\overline{\text{FT}}$ pins and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

There are pull-up devices on the ZQ and $\overline{\text{FT}}$ pins and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences
Linear Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 10 | 11 | 00 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 00 | 01 | 10 |

Note:

The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 00 | 11 | 10 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 10 | 01 | 00 |

Note:

The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

| Function | \overline{GW} | \overline{BW} | \overline{BA} | \overline{BB} | \overline{BC} | \overline{BD} | Notes |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------|
| Read | H | H | X | X | X | X | 1 |
| Read | H | L | H | H | H | H | 1 |
| Write byte a | H | L | L | H | H | H | 2, 3 |
| Write byte b | H | L | H | L | H | H | 2, 3 |
| Write byte c | H | L | H | H | L | H | 2, 3, 4 |
| Write byte d | H | L | H | H | H | L | 2, 3, 4 |
| Write all bytes | H | L | L | L | L | L | 2, 3, 4 |
| Write all bytes | L | X | X | X | X | X | |

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs \overline{BA} , \overline{BB} , \overline{BC} and/or \overline{BD} may be used in any combination with \overline{BW} to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

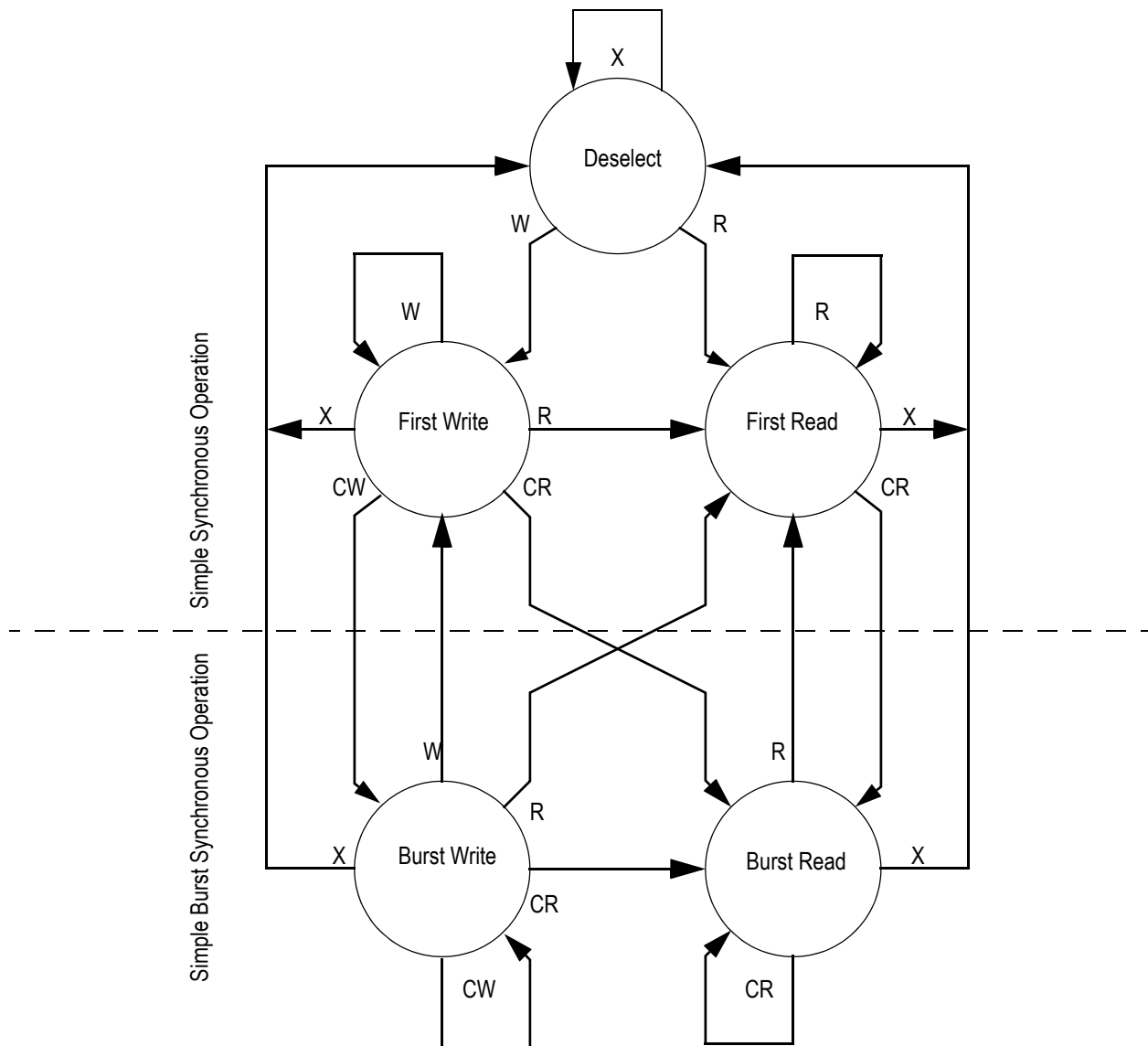
Synchronous Truth Table

| Operation | Address Used | State Diagram Key ⁵ | \bar{E}_1 | E^2 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \bar{W}^3 | DQ ⁴ |
|------------------------------------|-----------------|--------------------------------|-------------|----------|-------------------|-------------------|------------------|-------------|-----------------|
| Deselect Cycle, Power Down | None | X | H | X | X | L | X | X | High-Z |
| Deselect Cycle, Power Down | None | X | L | F | L | X | X | X | High-Z |
| Deselect Cycle, Power Down | None | X | L | F | H | L | X | X | High-Z |
| Read Cycle, Begin Burst | External | R | L | T | L | X | X | X | Q |
| Read Cycle, Begin Burst | External | R | L | T | H | L | X | F | Q |
| Write Cycle, Begin Burst | External | W | L | T | H | L | X | T | D |
| <i>Read Cycle, Continue Burst</i> | <i>Next</i> | <i>CR</i> | <i>X</i> | <i>X</i> | <i>H</i> | <i>H</i> | <i>L</i> | <i>F</i> | <i>Q</i> |
| Read Cycle, Continue Burst | Next | CR | H | X | X | H | L | F | Q |
| <i>Write Cycle, Continue Burst</i> | <i>Next</i> | <i>CW</i> | <i>X</i> | <i>X</i> | <i>H</i> | <i>H</i> | <i>L</i> | <i>T</i> | <i>D</i> |
| Write Cycle, Continue Burst | Next | CW | H | X | X | H | L | T | D |
| Read Cycle, Suspend Burst | Current | | | X | H | H | H | F | Q |
| Read Cycle, Suspend Burst | Current | | | X | X | H | H | F | Q |
| Write Cycle, Suspend Burst | Current | | | X | H | H | H | T | D |
| Write Cycle, Suspend Burst | Current | | | X | X | H | H | T | D |

Notes:

1. X = Don't Care, H = High, L = Low
2. $E = T$ (True) if $E_2 = 1$ and $\bar{E}_3 = 0$; $E = F$ (False) if $E_2 = 0$ or $\bar{E}_3 = 1$
3. $W = T$ (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. \bar{G} is an asynchronous input. \bar{G} can be driven high at any time to disable active output drivers. \bar{G} low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying \overline{ADSP} high and \overline{ADSC} low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying \overline{ADSP} high and \overline{ADV} low while using \overline{ADSC} to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram


Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes \overline{G} is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$, $E2$, and $E3$) and Write (\overline{BA} , \overline{BB} , \overline{BC} , \overline{BD} , \overline{BW} , and \overline{GW}) control inputs, and that \overline{ADSP} is tied high and \overline{ADSC} is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and \overline{ADSC} control inputs, and assumes \overline{ADSP} is tied high and \overline{ADV} is tied low.

Simplified State Diagram with \overline{G}

Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of \overline{G} .
2. Use of "Dummy Reads" (Read Cycles with \overline{G} High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume \overline{G} has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

 (All voltages reference to V_{SS})

| Symbol | Description | Value | Unit |
|------------|-------------------------------|----------------------------------------------|------|
| V_{DD} | Voltage on V_{DD} Pins | -0.5 to 4.6 | V |
| V_{DDQ} | Voltage on V_{DDQ} Pins | -0.5 to V_{DD} | V |
| $V_{I/O}$ | Voltage on I/O Pins | -0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.) | V |
| V_{IN} | Voltage on Other Input Pins | -0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.) | V |
| I_{IN} | Input Current on Any Pin | +/-20 | mA |
| I_{OUT} | Output Current on Any I/O Pin | +/-20 | mA |
| P_D | Package Power Dissipation | 1.5 | W |
| T_{STG} | Storage Temperature | -55 to 125 | °C |
| T_{BIAS} | Temperature Under Bias | -55 to 125 | °C |

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges (1.8 V/2.5 V Version)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------|------------|------|------|----------|------|-------|
| 1.8 V Supply Voltage | V_{DD1} | 1.7 | 1.8 | 2.0 | V | |
| 2.5 V Supply Voltage | V_{DD2} | 2.3 | 2.5 | 2.7 | V | |
| 1.8 V V_{DDQ} I/O Supply Voltage | V_{DDQ1} | 1.7 | 1.8 | V_{DD} | V | |
| 2.5 V V_{DDQ} I/O Supply Voltage | V_{DDQ2} | 2.3 | 2.5 | V_{DD} | V | |

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ2} & V_{DDQ1} Range Logic Levels

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|----------|--------------------|------|--------------------|------|-------|
| V_{DD} Input High Voltage | V_{IH} | $0.6 \cdot V_{DD}$ | — | $V_{DD} + 0.3$ | V | 1 |
| V_{DD} Input Low Voltage | V_{IL} | -0.3 | — | $0.3 \cdot V_{DD}$ | V | 1 |

Notes:

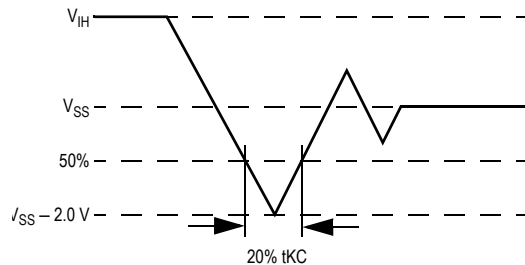
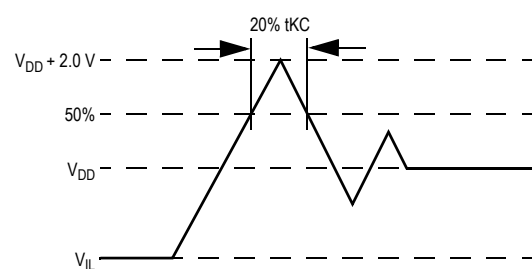
- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Recommended Operating Temperatures

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------------------------|--------|------|------|------|--------------------|-------|
| Ambient Temperature (Commercial Range Versions) | T_A | 0 | 25 | 70 | $^{\circ}\text{C}$ | 2 |
| Ambient Temperature (Industrial Range Versions) | T_A | -40 | 25 | 85 | $^{\circ}\text{C}$ | 2 |

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing

Overshoot Measurement and Timing

Capacitance

($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

| Parameter | Symbol | Test conditions | Typ. | Max. | Unit |
|--------------------------|-----------|------------------------|------|------|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0\text{ V}$ | 4 | 5 | pF |
| Input/Output Capacitance | $C_{I/O}$ | $V_{OUT} = 0\text{ V}$ | 6 | 7 | pF |

Note:

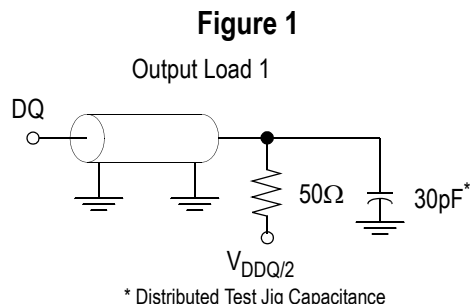
These parameters are sample tested.

AC Test Conditions

| Parameter | Conditions |
|------------------------|-------------------------|
| Input high level | $V_{DD} - 0.2\text{ V}$ |
| Input low level | 0.2 V |
| Input slew rate | 1 V/ns |
| Input reference level | $V_{DD}/2$ |
| Output reference level | $V_{DDQ}/2$ |
| Output load | Fig. 1 |

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.


DC Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|---------------------------------------------|----------|--------------------------------------------------|--------------------|-------------------|
| Input Leakage Current (except mode pins) | I_{IL} | $V_{IN} = 0 \text{ to } V_{DD}$ | -1 μA | 1 μA |
| \overline{FT} , SCD, ZQ, ZZ Input Current | I_{IN} | $V_{DD} \geq V_{IN} \geq 0\text{ V}$ | -100 μA | 100 μA |
| Output Leakage Current | I_{OL} | Output Disable, $V_{OUT} = 0 \text{ to } V_{DD}$ | -1 μA | 1 μA |

DC Output Characteristics (1.8 V/2.5 V Version)

| Parameter | Symbol | Test Conditions | Min | Max |
|---------------------------|-----------|------------------------------------------------------|--------------------------|-------|
| 1.8 V Output High Voltage | V_{OH1} | $I_{OH} = -4\text{ mA}$, $V_{DDQ} = 1.6\text{ V}$ | $V_{DDQ} - 0.4\text{ V}$ | — |
| 2.5 V Output High Voltage | V_{OH2} | $I_{OH} = -8\text{ mA}$, $V_{DDQ} = 2.375\text{ V}$ | 1.7 V | — |
| 1.8 V Output Low Voltage | V_{OL1} | $I_{OL} = 4\text{ mA}$ | — | 0.4 V |
| 2.5 V Output Low Voltage | V_{OL2} | $I_{OL} = 8\text{ mA}$ | — | 0.4 V |

Operating Currents

| Parameter | Test Conditions | Mode | Symbol | -250 | | -200 | | -150 | | Unit | |
|-------------------|------------------------------------------------------------------------------------|-----------|--------------|-----------------------|-------------|-----------|-------------|-----------|-------------|-----------|----|
| | | | | 0 to 70°C | -40 to 85°C | 0 to 70°C | -40 to 85°C | 0 to 70°C | -40 to 85°C | | |
| Operating Current | Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open | (x32/x36) | Pipeline | I_{DD} I_{DDQ} | 200 30 | 220 30 | 170 25 | 190 25 | 140 20 | 160 20 | mA |
| | | | Flow Through | I_{DD} I_{DDQ} | 160 25 | 180 25 | 140 20 | 160 20 | 130 15 | 150 15 | mA |
| | | (x18) | Pipeline | I_{DD} I_{DDQ} | 185 15 | 205 15 | 155 15 | 175 15 | 130 10 | 150 10 | mA |
| | | | Flow Through | I_{DD} I_{DDQ} | 145 15 | 165 15 | 130 10 | 150 10 | 120 8 | 140 8 | mA |
| Standby Current | $ZZ \geq V_{DD} - 0.2 V$ | — | Pipeline | I_{SB} | 40 | 50 | 40 | 50 | 40 | 50 | mA |
| | | | Flow Through | I_{SB} | 40 | 50 | 40 | 50 | 40 | 50 | mA |
| Deselect Current | Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ | — | Pipeline | I_{DD} | 85 | 90 | 75 | 80 | 60 | 65 | mA |
| | | | Flow Through | I_{DD} | 60 | 65 | 50 | 55 | 50 | 55 | mA |

Notes:

- I_{DD} and I_{DDQ} apply to any combination of V_{DD2} , V_{DD1} , V_{DDQ2} , and V_{DDQ1} operation.
- All parameters listed are worst case scenario.

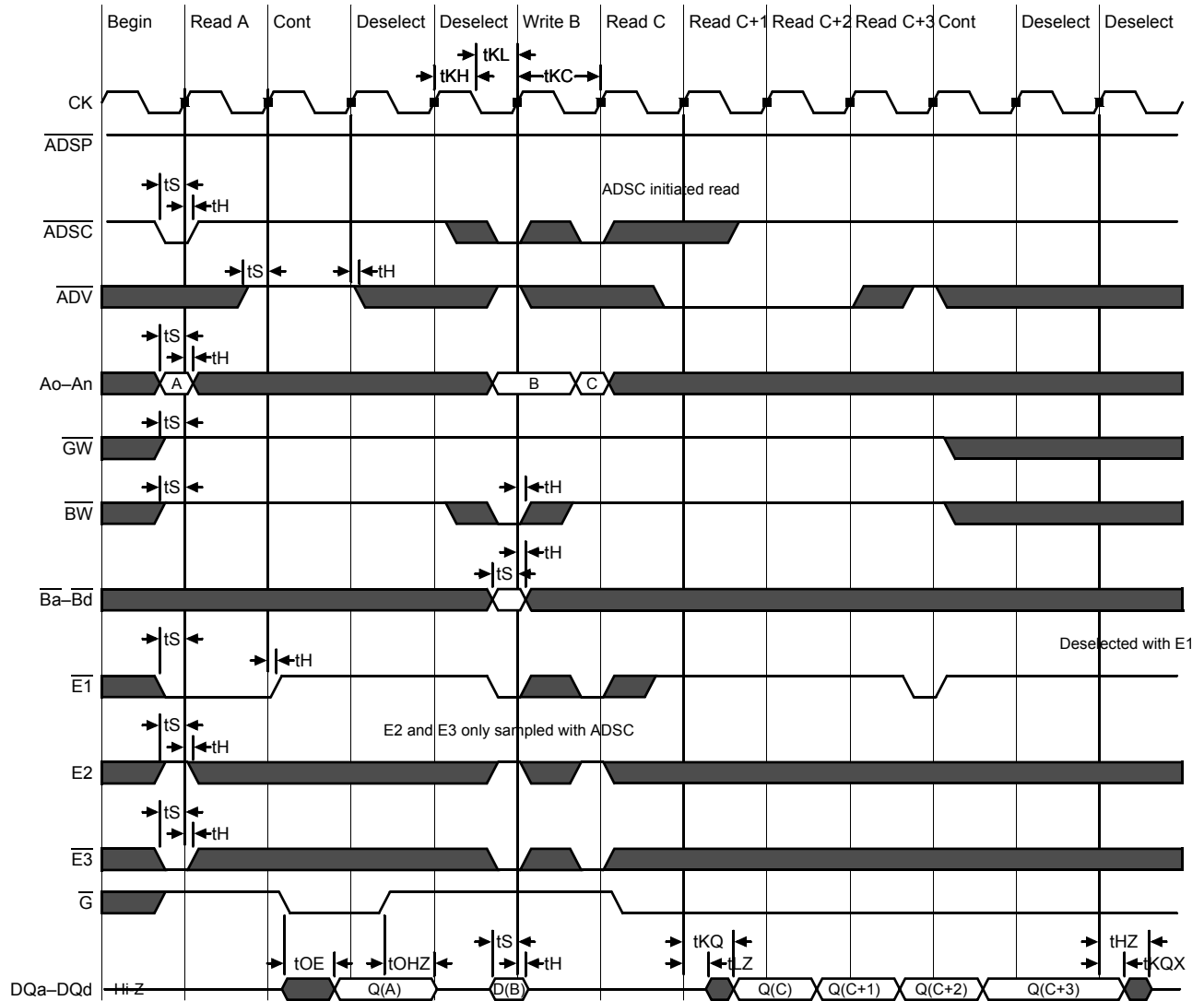
AC Electrical Characteristics

| | Parameter | Symbol | -250 | | -200 | | -150 | | Unit |
|---------------------|-------------------------------|-------------------------------|------|-----|------|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Pipeline | Clock Cycle Time | t _{KC} | 4.0 | — | 5.0 | — | 6.7 | — | ns |
| | Clock to Output Valid | t _{KQ} | — | 3.0 | — | 3.0 | — | 3.8 | ns |
| | Clock to Output Invalid | t _{KQX} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Clock to Output in Low-Z | t _{LZ} ¹ | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Setup time | t _S | 1.2 | — | 1.4 | — | 1.5 | — | ns |
| | Hold time | t _H | 0.2 | — | 0.4 | — | 0.5 | — | ns |
| Flow Through | Clock Cycle Time | t _{KC} | 5.5 | — | 6.5 | — | 7.5 | — | ns |
| | Clock to Output Valid | t _{KQ} | — | 5.5 | — | 6.5 | — | 7.5 | ns |
| | Clock to Output Invalid | t _{KQX} | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| | Clock to Output in Low-Z | t _{LZ} ¹ | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| | Setup time | t _S | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Hold time | t _H | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| | Clock HIGH Time | t _{KH} | 1.3 | — | 1.3 | — | 1.5 | — | ns |
| | Clock LOW Time | t _{KL} | 1.7 | — | 1.7 | — | 1.7 | — | ns |
| | Clock to Output in High-Z | t _{HZ} ¹ | 1.5 | 2.5 | 1.5 | 3.0 | 1.5 | 3.0 | ns |
| | \bar{G} to Output Valid | t _{OE} | — | 2.5 | — | 3.0 | — | 3.8 | ns |
| | \bar{G} to output in Low-Z | t _{OLZ} ¹ | 0 | — | 0 | — | 0 | — | ns |
| | \bar{G} to output in High-Z | t _{OHZ} ¹ | — | 2.5 | — | 3.0 | — | 3.8 | ns |
| | ZZ setup time | t _{ZZS} ² | 5 | — | 5 | — | 5 | — | ns |
| | ZZ hold time | t _{ZZH} ² | 1 | — | 1 | — | 1 | — | ns |
| | ZZ recovery | t _{ZZR} | 20 | — | 20 | — | 20 | — | ns |

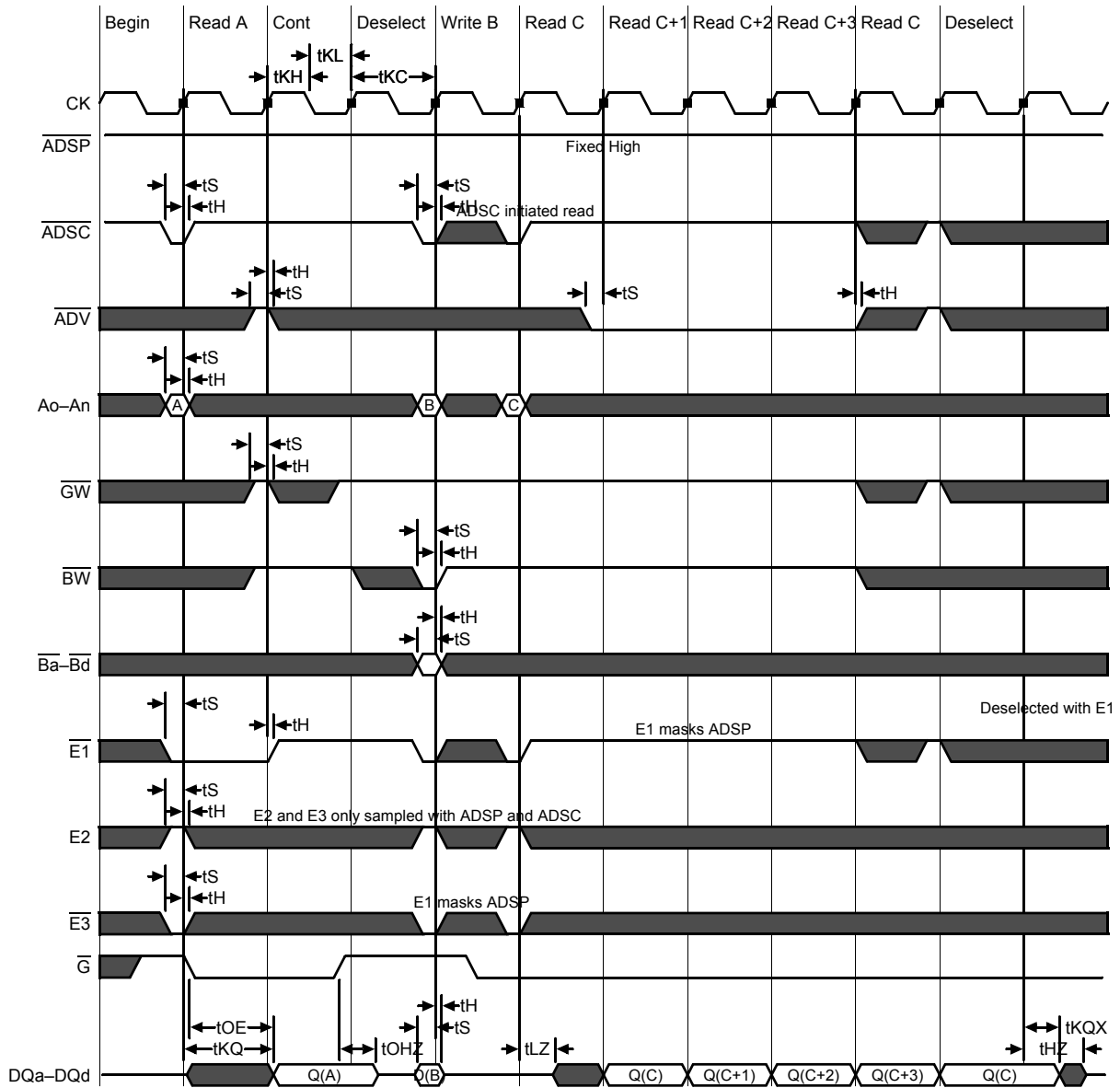
Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing (DCD)



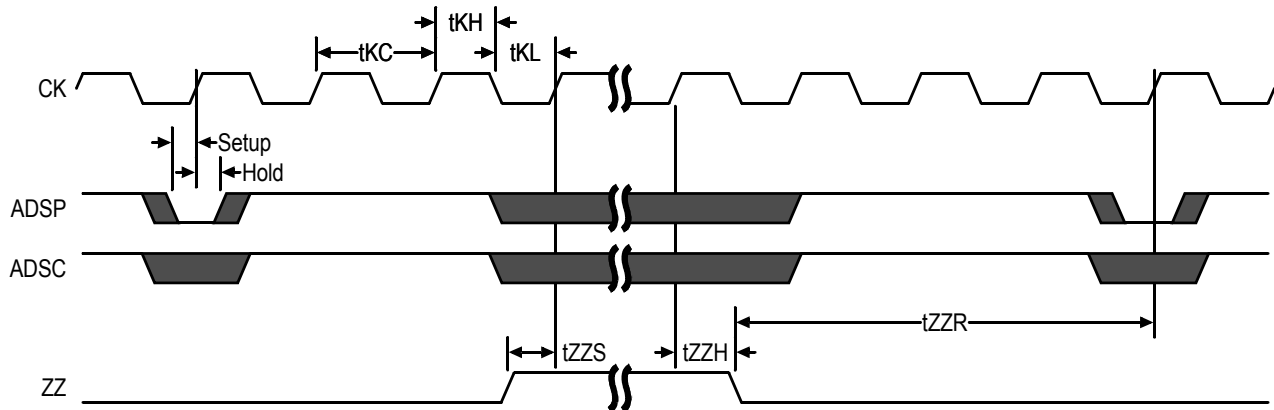
Flow Through Mode Timing (DCD)


Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, I_{SB2} is guaranteed after the time t_{ZZI} is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during t_{ZZR} , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



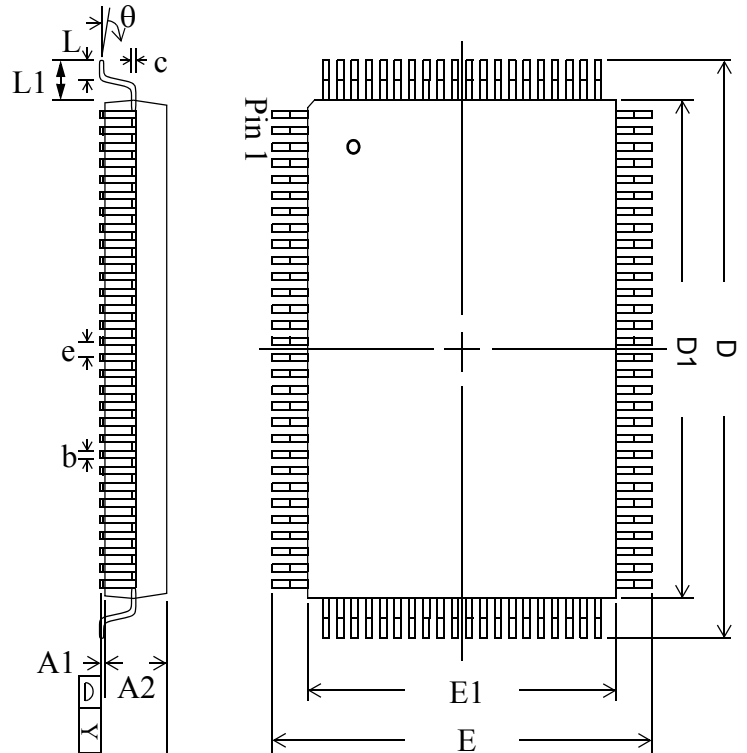
Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of “dummy read cycles” (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs (like this one) do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

TQFP Package Drawing (Package T)

| Symbol | Description | Min. | Nom. | Max |
|----------|--------------------|------|------|------|
| A1 | Standoff | 0.05 | 0.10 | 0.15 |
| A2 | Body Thickness | 1.35 | 1.40 | 1.45 |
| b | Lead Width | 0.20 | 0.30 | 0.40 |
| c | Lead Thickness | 0.09 | — | 0.20 |
| D | Terminal Dimension | 21.9 | 22.0 | 22.1 |
| D1 | Package Body | 19.9 | 20.0 | 20.1 |
| E | Terminal Dimension | 15.9 | 16.0 | 16.1 |
| E1 | Package Body | 13.9 | 14.0 | 14.1 |
| e | Lead Pitch | — | 0.65 | — |
| L | Foot Length | 0.45 | 0.60 | 0.75 |
| L1 | Lead Length | — | 1.00 | — |
| Y | Coplanarity | | | 0.10 |
| θ | Lead Angle | 0° | — | 7° |



Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

| Org | Part Number ¹ | Type | Voltage Option | Package | Speed ² (MHz/ns) | T _A ³ | Status ⁴ |
|-----------|--------------------------|------|----------------|---------------------|--------------------------------|-----------------------------|---------------------|
| 512K x 18 | GS880E18BT-250V | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | C | MP |
| 512K x 18 | GS880E18BT-200V | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | C | MP |
| 512K x 18 | GS880E18BT-150V | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | C | MP |
| 256K x 32 | GS880E32BT-250V | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | C | MP |
| 256K x 32 | GS880E32BT-200V | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | C | MP |
| 256K x 32 | GS880E32BT-150V | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | C | MP |
| 256K x 36 | GS880E36BT-250V | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | C | MP |
| 256K x 36 | GS880E36BT-200V | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | C | MP |
| 256K x 36 | GS880E36BT-150V | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | C | MP |
| 512K x 18 | GS880E18BT-250IV | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | I | MP |
| 512K x 18 | GS880E18BT-200IV | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | I | MP |
| 512K x 18 | GS880E18BT-150IV | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | I | MP |
| 256K x 32 | GS880E32BT-250IV | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | I | MP |
| 256K x 32 | GS880E32BT-200IV | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | I | MP |
| 256K x 32 | GS880E32BT-150IV | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | I | MP |
| 256K x 36 | GS880E36BT-250IV | DCD | 1.8 V or 2.5 V | TQFP | 250/5.5 | I | MP |
| 256K x 36 | GS880E36BT-200IV | DCD | 1.8 V or 2.5 V | TQFP | 200/6.5 | I | MP |
| 256K x 36 | GS880E36BT-150IV | DCD | 1.8 V or 2.5 V | TQFP | 150/7.5 | I | MP |
| 512K x 18 | GS880E18BGT-250V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 250/5.5 | C | PQ |
| 512K x 18 | GS880E18BGT-200V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 200/6.5 | C | PQ |
| 512K x 18 | GS880E18BGT-150V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 150/7.5 | C | PQ |
| 256K x 32 | GS880E32BGT-250V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 250/5.5 | C | PQ |
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| 256K x 36 | GS880E36BGT-250V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 250/5.5 | C | PQ |
| 256K x 36 | GS880E36BGT-200V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 200/6.5 | C | PQ |
| 256K x 36 | GS880E36BGT-150V | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 150/7.5 | C | PQ |
| 512K x 18 | GS880E18BGT-250IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 250/5.5 | I | PQ |
| 512K x 18 | GS880E18BGT-200IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 200/6.5 | I | PQ |

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS880E18BT-200IVT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- MP = Mass Production. PQ = Pre-Qualification.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

Ordering Information for GSI Synchronous Burst RAMs

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| 256K x 32 | GS880E32BGT-150IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 150/7.5 | I | PQ |
| 256K x 36 | GS880E36BGT-250IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 250/5.5 | I | PQ |
| 256K x 36 | GS880E36BGT-200IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 200/6.5 | I | PQ |
| 256K x 36 | GS880E36BGT-150IV | DCD | 1.8 V or 2.5 V | RoHS-compliant TQFP | 150/7.5 | I | PQ |

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9Mb Sync SRAM Datasheet Revision History

| DS/Date Rev. Code: Old; New | Types of Changes Format or Content | Page;Revisions;Reason |
|----------------------------------------|-----------------------------------------------|------------------------------|
| 880ExxB_V_r1 | | • Creation of new datasheet |