HS-80C85RH

Radiation Hardened 8-Bit CMOS Microprocessor

February 1996

Features

- Devices QML Qualified in Accordance With MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-95824 and Intersil' QM Plan
- Radiation Hardened EPI-CMOS
  - Parametrics Guaranteed 1 x 10^5 RAD(Si)
  - Transient Upset > 1 x 10^8 RAD(Si)/s
  - Latch-up Free > 1 x 10^{12} RAD(Si)/s
- Low Standby Current 500μA Max
- Low Operating Current 5.0mA/MHz (X_1 Input)
- Electrically Equivalent to Sandia SA 3000
- 100% Software Compatible with INTEL 8085
- Operation from DC to 2MHz, Post Radiation
- Single 5 Volt Power Supply
- On-Chip Clock Generator and System Controller
- Four Vectored Interrupt Inputs
- Completely Static Design
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

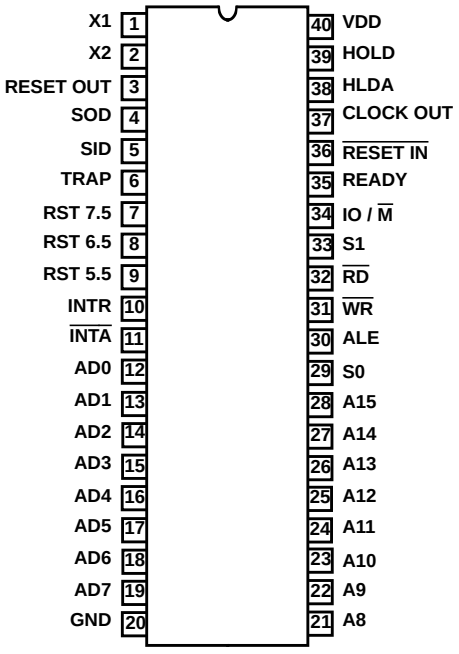
Description

The HS-80C85RH is an 8-bit CMOS microprocessor fabricated using the Intersil radiation hardened self-aligned junction isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

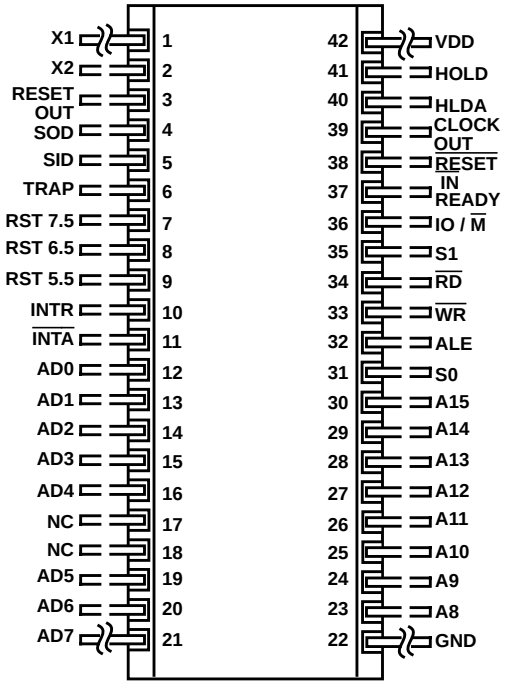
The HS-80C85RH is a functional logic emulation of the HMOS 8085 and its instruction set is 100% software compatible with the HMOS device. The HS80C85RH is designed for operation with a single 5 volt power supply. Its high level of integration allows the construction of a radiation hardened microcomputer system with as few as three ICs (HS-80C85RH CPU, HS83C55RH ROM I/O, and the HS-81C55/56RH RAM I/O.

Pinouts

40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835, CDIP2-T40
TOP VIEW



42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) INTERSIL OUTLINE K42.A
TOP VIEW

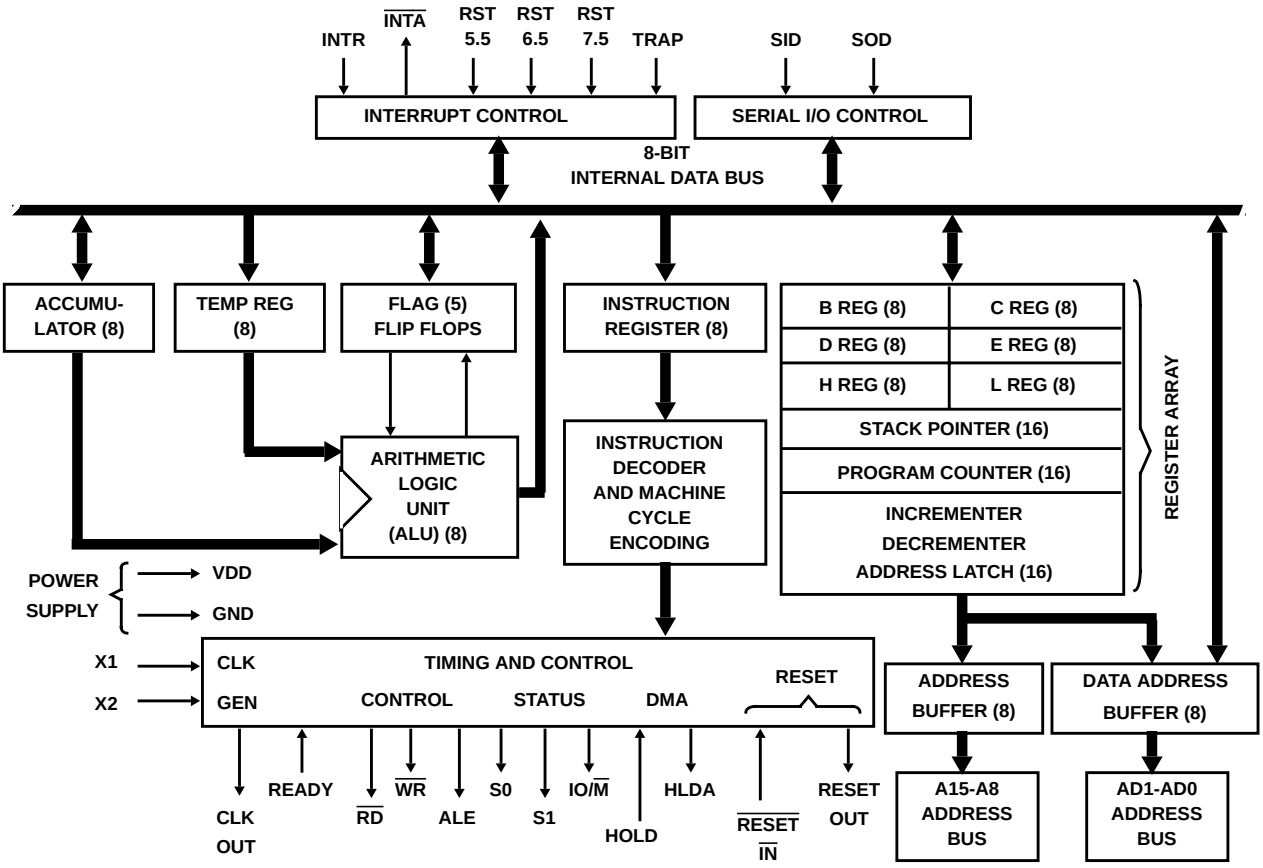


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962R9582401QQC	-55°C to +125°C	MIL-PRF-38535 Level Q	40 Lead SBDIP
5962R9582401QXC	-55°C to +125°C	MIL-PRF-38535 Level Q	42 Lead Ceramic Flatpack
5962R9582401VQC	-55°C to +125°C	MIL-PRF-38535 Level V	40 Lead SBDIP
5962R9582401VXC	-55°C to +125°C	MIL-PRF-38535 Level V	42 Lead Ceramic Flatpack
HS1-80C85RH/SAMPLE	+25°C	Sample	40 Lead SBDIP
HS9-80C85RH/SAMPLE	+25°C	Sample	42 Lead Ceramic Flatpack

Functional Diagram

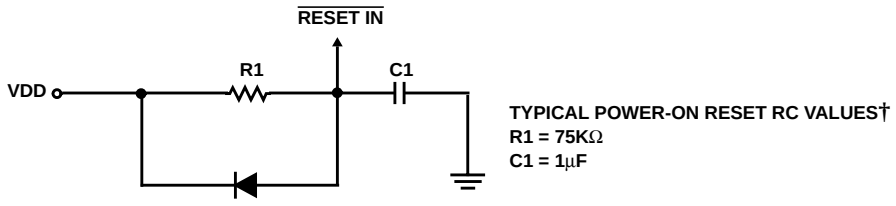


Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
A8 - A15	21-28	O	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD0-7	12-19	I/O	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	32	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S0, S1, and IO/$\overline{M}$	31, 35, & 36	O	Machine Cycle Status: IO/$\overline{M}$ S1 S0 Status 0 0 1 Memory write 0 1 0 Memory write 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Opcode fetch 1 1 1 Interrupt acknowledge T 0 0 Halt T X X Hold T X X Reset T = 3-State (high impedance) X = Unspecified S1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S0 and S1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	34	O	Read Control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	33	O	Write Control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.
READY	35	I	Ready: If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	39	I	Hold: Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data Bus, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	38	O	Hold Acknowledge: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
INTR	10	I	Interrupt Request: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{\text{INTA}}$	11	O	Interrupt Acknowledge: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	9 8 7	I	Restart Interrupts: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 6. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP	6	I	Trap: Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 6.)
$\overline{\text{RESET IN}}$	36	I	Reset In: Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 1). Upon power-up, $\overline{\text{RESET IN}}$ must remain low for at least 10 "clock cycle" after minimum VDD has been reached. For proper reset operation after the power-up duration, $\overline{\text{RESET IN}}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT	3	O	Reset Out: Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X1 X2	1 2	I O	X1 and X2: Are connected to a crystal, LC, or RC network to drive the internal clock generator. X, can also be an external clock Input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	37	O	Clock: Clock output for use as a system clock. The period of CLK is twice the X1, X2 input period.
SID	5	I	Serial Input Data Line: The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	4	O	Serial Output Data Line: The output SOD is set or reset as specified by the SIM instruction.
VCC	40	I	Power: +5V supply.
GND	20	I	Ground: Reference.



† Values may have to vary due to applied power supply ramp up time.

FIGURE 1. POWER-ON RESET CIRCUIT

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VCC+0.3V
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
Junction Temperature . . . . . +175^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C
Typical Derating Factor . . . . . 2.0mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	45^{o}C/W	10^{o}C/W
Ceramic Flatpack Package	77^{o}C/W	13^{o}C/W

Maximum Package Power Dissipation at +125^{o}C Ambient
SBDIP Package 1.11W
Ceramic Flatpack Package 0.65W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . . 22.2mW/^{o}C
Ceramic Flatpack Package . . . . . 13.0mW/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . . +4.75V to +5.25V
Operating Temperature Range (T_A) . . . . . -55^{o}C to +125^{o}C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current	IIH or IIL	VDD = 5.25V, VI = VDD or GND	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-1.0	1.0	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -1.0mA	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	VDD -0.5	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 1.0mA,	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	0.5	V
Static Current	IDDSB	VDD = 5.25V, Clock Out = Hi and Low	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	500	µA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.25V, f = 1MHz (Note 2)	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	5.0	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, TCYC = 500ns, VOL ≤ VDD/2, VOH ≥ VDD/2	7, 8A, 8B	-55^{o}C, +25^{o}C, or +125^{o}C	-	-	-

NOTES:

1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (IDDOP) is proportional to crystal frequency. Parts are tested at 1MHz

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
CLK Low Time (Standard CLK Loading)	T1	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	40	-	ns
CLK High Time (Standard CLK Loading)	T2	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	100	-	ns
CLK Rise Time	Tr	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	115	ns
CLK Fall Time	Tf	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	115	ns
X1 Rising to CLK Rising	TXKR	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	30	250	ns
X1 Rising to CLK Falling	TXKF	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	50	275	ns
A8-15 Valid to Leading Edge of Control (Note 5)	TAC	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	300	-	ns
A0-7 Valid to Leading Edge of Control	TACL	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	300	-	ns
A0-15 Valid to Valid Data In	TAD	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	875	-	ns
Address Float After Leading Edge of READ (INTA)	TAFR	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	70	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
A8-15 Valid Before Trailing Edge of ALE (Note 5)	TAL	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
A0-7 Valid Before Trailing Edge of ALE	tALL	9, 10, 11	-55°C, +25°C, +125°C	125	-	ns
READY Valid from Address Valid	TARY	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Address (A8-15) Valid After Control	TCA	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
Width of Control Low (RD, WR, INTA) Edge of ALE	TCC	9, 10, 11	-55°C, +25°C, +125°C	575	-	ns
Trailing Edge of Control to Leading Edge of ALE	TCL	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Data Valid to Trailing Edge of WRITE	TDW	9, 10, 11	-55°C, +25°C, +125°C	575	-	ns
HLDA to Bus Enable	THABE	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
Bus Float After HLDA	THABF	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
HLDA Valid to Trailing Edge of CLK	THACK	9, 10, 11	-55°C, +25°C, +125°C	90	-	ns
HOLD Hold Time	THDH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
HOLD Setup Time to Trailing Edge of CLK	THDS	9, 10, 11	-55°C, +25°C, +125°C	-	300	ns
INTR Hold Time	TINH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
INTR, RST and TRAP Setup Time to Falling Edge of CLK	TINS	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
Address Hold Time After ALE	TLA	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
Trailing Edge of ALE to Leading Edge of Control	TLC	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
ALE Low During CLK High	TLCK	9, 10, 11	-55°C, +25°C, +125°C	125	-	ns
ALE to Valid Data During Read	TLDR	9, 10, 11	-55°C, +25°C, +125°C	675	-	ns
ALE to Valid Data During Write	TLDW	9, 10, 11	-55°C, +25°C, +125°C	-	350	ns
ALE Width	TLL	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
ALE to READY Stable	TLRY	9, 10, 11	-55°C, +25°C, +125°C	-	175	ns
Trailing Edge of READ to Re-Enabling the Address	TRAE	9, 10, 11	-55°C, +25°C, +125°C	120	-	ns
READ (or INTA) to Valid Data	TRD	9, 10, 11	-55°C, +25°C, +125°C	375	-	ns
Control Trailing Edge to Leading Edge of Next Control	TRV	9, 10, 11	-55°C, +25°C, +125°C	550	-	ns
Data Hold Time After READ INTA	TRDH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
READY Hold Time	TRYH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
READY Setup Time to Leading Edge of CLK	TRYS	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Data Valid After Trailing Edge of WRITE	TWD	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
LEADING Edge of WRITE to Data Valid	TWDL	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns

NOTES:

1. Output timings are measured with a purely capacitive load, CL = 150pF
2. VDD = 4.75V, VIH = 4.25V, VIL = 0.8V
3. Delay times are measured with a 1MHz clock. An algorithm is used to convert the delays into the AC timings above with a TCYC = 500ns.
4. The AC table is tested as shown above to guarantee the processor system timing.
5. A8 - A15 address specifications also apply to IO/M, S0 and S1 except A8 - A15 are undefined during T4-T6 of off cycle whereas IO/M, So, and S1 are stable.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	T_A = +25°C	-	13	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF

NOTE:

1. All measurements referenced to device ground.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C; In Accordance With SMD)

TABLE 6. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

NAME	PRIORITY	ADDRESS BRANCHED TO (1) WHEN INTERRUPT OCCURS	TYPE TRIGGER
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched)
RST 6.5	3	34CH	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note 2	High level until sampled.

NOTES:

1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

TABLE 7. BUS TIMING SPECIFICATION AS A t_{CYC} DEPENDENT

SYMBOL	HS-8OC85RH		SYMBOL	HS-8OC85RH	
tAL	(1/2)T- 175	Minimum	tCC	(3/2 + N)T - 175	Minimum
tLA	(1/2)T- 175	Minimum	tCL	(1/2)T - 190	Minimum
tLL	(1/2)T-50	Minimum	tARY	(3/2)T - 500	Maximum
tLCK	(1/2)T- 125	Minimum	tHACK	(1/2)T - 160	Minimum
tLC	(1/2)T- 100	Minimum	tHABF	(1/2)T +125	Maximum
tAD	(5/2 + N)T - 375	Maximum	tHABE	(1/2)T +125	Maximum
tRD	(3/2 + N)T - 375	Maximum	tAC	(2/2)T - 200	Minimum
tRAE	(1/2)T- 130	Minimum	t1	(1/2)T-210	Minimum
tCA	(1/2)T - 100	Minimum	t2	(1/2)T- 150	Minimum
tDW	(3/2 + N)T - 175	Minimum	tRV	(3/2)T - 200	Minimum
tWD	(1/2)T-100	Minimum	tLDR	(4/2)T - 325	Maximum

NOTE: N is equal to the total WAIT states T = tCYC

Waveforms

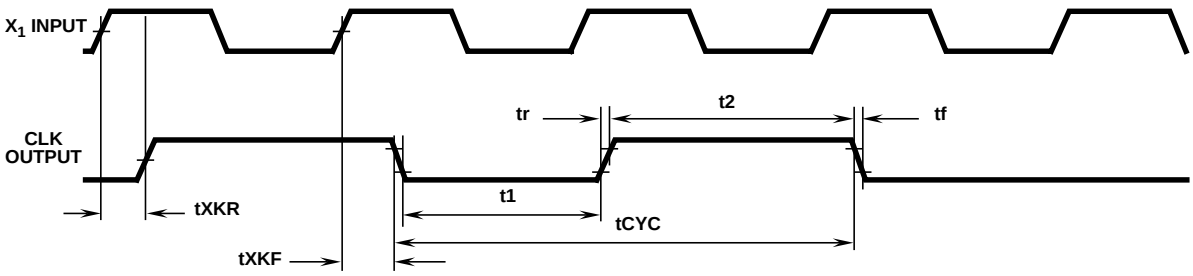


FIGURE 2. CLOCK

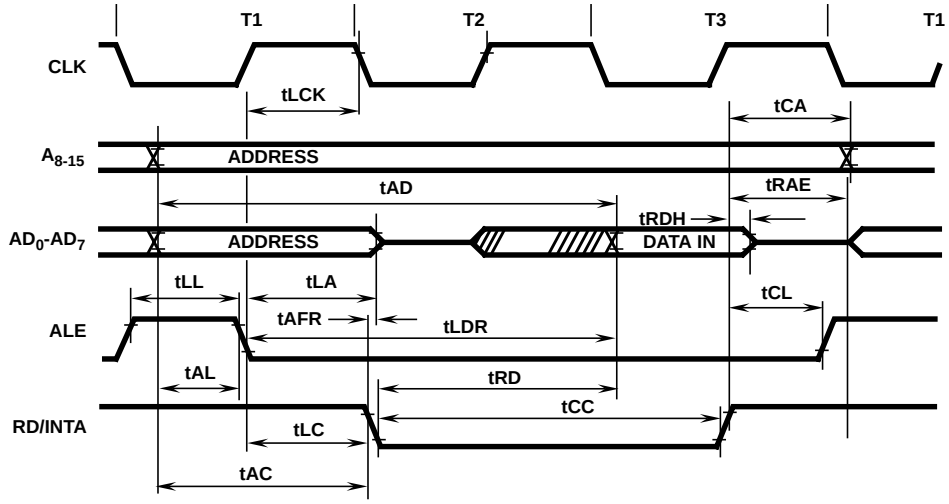


FIGURE 3. READ

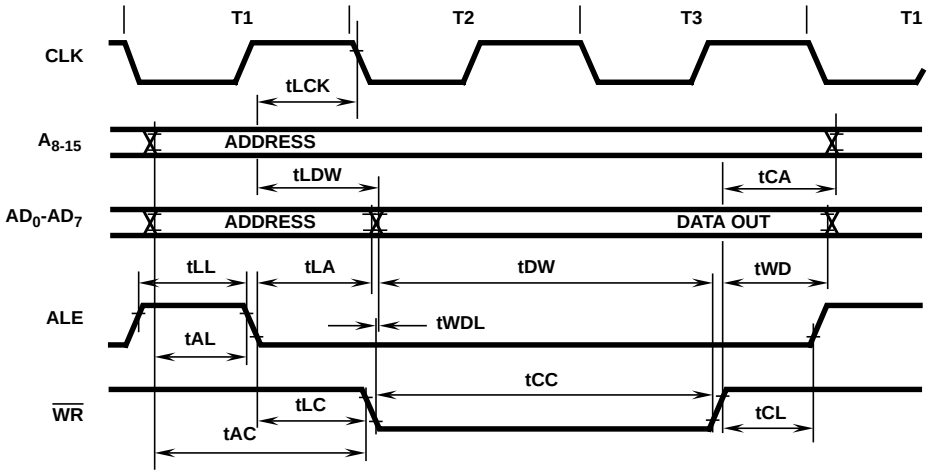


FIGURE 4. WRITE

Waveforms (Continued)

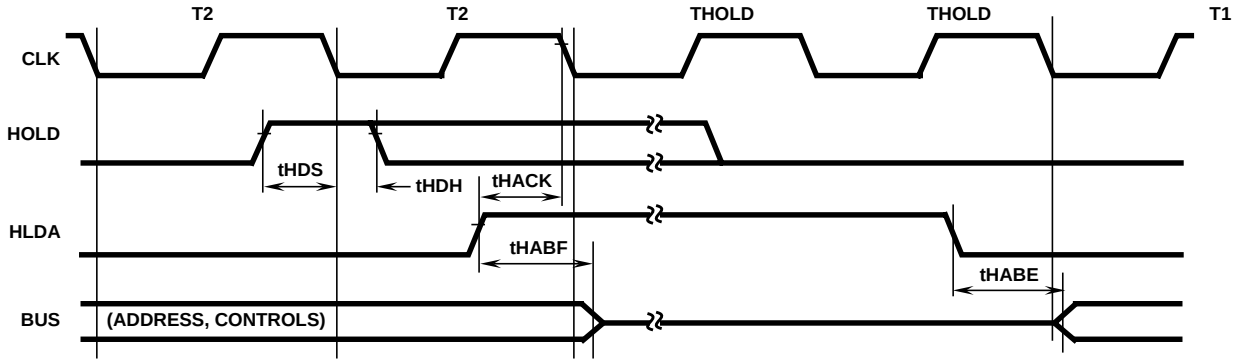
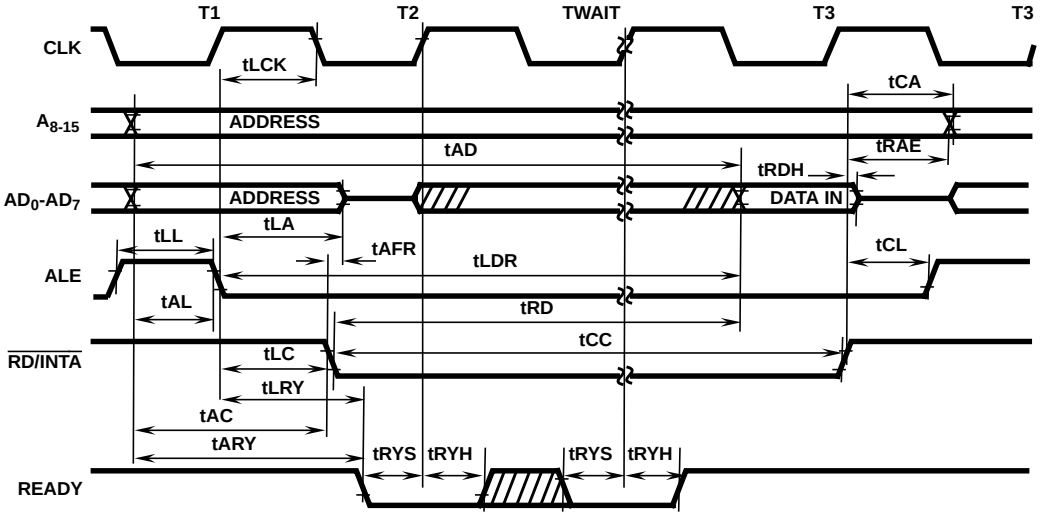
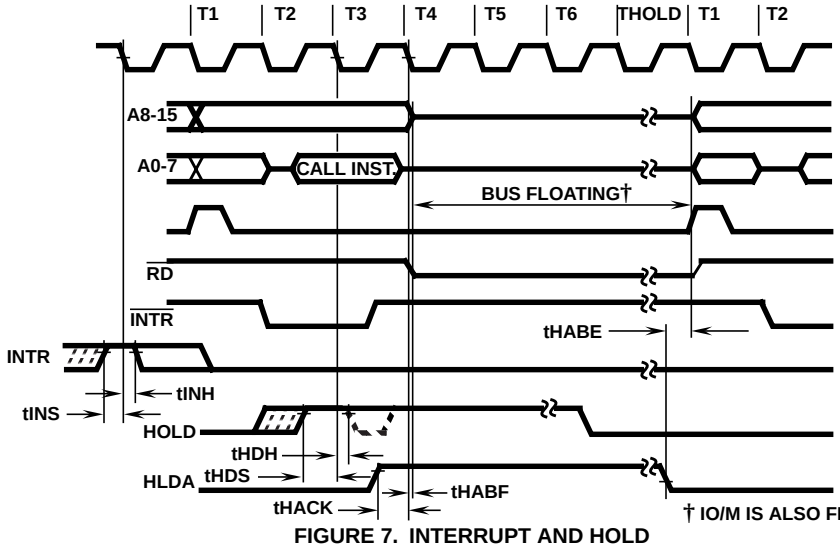


FIGURE 5. HOLD



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

FIGURE 6. READ OPERATION WITH WAIT CYCLE (TYPICAL) - SAME READY TIMING APPLIES TO WRITE



† IO/M IS ALSO FLOATING DURING THIS TIME.

FIGURE 7. INTERRUPT AND HOLD

TABLE 9. INSTRUCTION SET SUMMARY

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
MOVE, LOAD, AND STORE									
MOVr1, r2	0	1	D	D	D	S	S	S	Move register to register
MOV M.r	0	1	1	1	0	S	S	S	Move register to memory
MOV r.M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
CZ	1	1	0	0	1	1	0	0	Call on zero
CNZ	1	1	0	0	0	1	0	0	Call on no zero
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Popregister Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top ot stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus

TABLE 9. INSTRUCTION SET SUMMARY (Continued)

MNEMONIC	INSTRUCTION CODE								OPERATIONS DESCRIPTION
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H&L
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable Interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES:

1. DDS or SSS: B000, C001, D010, E011, H100, L101, Memory 110, A111
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

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Functional Description

The HS-80C85RH is a complete 8-bit parallel central processing unit implemented in a self aligned, silicon gate, CMOS technology. Its static design allows the device to be operated at any external clock frequency from a maximum of 4MHz down to DC. The processor clock can be stopped in either the high or low state and held there indefinitely. This type of operation is especially useful for system debug or power critical applications. The device is designed to fit into a minimum system of three ICs: CPU (HS-80C85RH), RAM/IO (HS-81C55/56RH) and ROM/IO Chip (HS-83C55RH).

Since the HS-80C85RH is implemented in CMOS, all of the advantages of CMOS technology are inherent in the device. These advantages include low standby and operating power, high noise immunity, moderately high speed, wide operating temperature range, and designed-in radiation hardness. Thus the HS-80C85RH is ideal for weapons and space applications.

The HS-80C85RH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The HS-80C85RH register set is as follows:

MNEMONIC	REGISTER	CONTENTS
ACC or A	Accumulator	8 -bits
PC	Program Counter	16-bit Address
BC, DE, HL	General-Purpose Registers; Data Pointer(HL)	8-bits x 6 or 16-bits x 3
SP	Stack Pointer	16-bit Address
Flags or F	Flag Register	5 Flags (8-bit space)

The HS-80C85RH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The HS-80C85RH provides $\overline{RD}$, $\overline{WR}$, S0, S1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The HS-80C85RH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the HS-80C85RH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

Interrupt and Serial I/O

The HS-80C85RH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP INTR is maskable (can be enabled or disabled by EI or DI software instructions), and causes the CPU to fetch in an RST instruction, externally placed on the data bus, which vectors a branch to any one of eight fixed memory locations (Restart addresses). The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 9.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive and are recognized with the same timing as INTR. RST 7.5 is rising edge sensitive.

For RST 7.5, only a pulse is required to set an internal flipflop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 80C85RH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP-highest priority, RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 8illustrates the TRAP interrupt request circuitry within the HS-80C85RH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

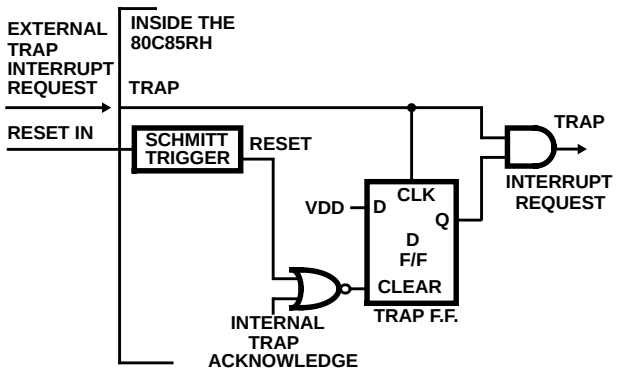


FIGURE 8. TRAP AND RESET IN CIRCUIT

The TRAP interrupt is special in that is disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current interrupt enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

Driving the X1 and X2 Inputs

You may drive the clock inputs of the HS-80C85RH with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency may be any value from DC to 4MHz and must be twice the desired internal clock frequency.

The following guidelines should be observed when a crystal is used to drive the HS-80C85RH clock input:

1. A 20pF capacitor should be connected from X2 to ground to assure oscillator start-up at the correct frequency.
2. A 10MΩ resistor is required between X1 and X2 for bias point stabilization. In addition, the crystal should have the following characteristics:
   1) Parallel resonance at twice the desired internal clock frequency
   2) CL (load capacitance) ≤ 30pF
   3) CS (shunt capacitance) ≤ 7pF
   4) RS (equivalent shunt resistance) ≤ 75Ω
   5) Drive level: 10mW
   6) Frequency tolerance: ±0.005% (suggested)

A parallel-resonant LC circuit may be used as the frequency-determining network for the HS-80C85RH, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

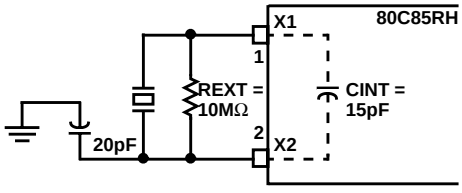
$$f = \frac{1}{2\pi\sqrt{L\,(Cext + Cint)}}$$

To minimize variations in frequency, it is recommended that you choose a value for Cext that is at least twice that of Cint, or 30pF. The use of an LC circuit is not recommended for frequencies higher than approximately 4MHz.

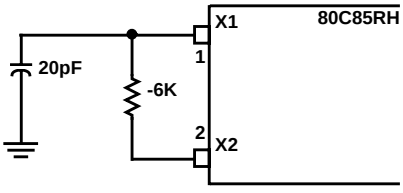
An RC circuit may be used as the frequency-determining network for the HS-80C85RH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 9 shows the recommended clock driver circuits.

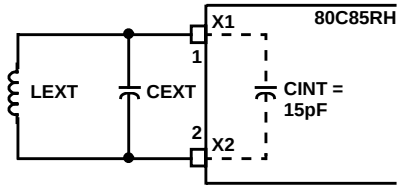
For driving frequencies up to and including 4MHz you may supply the driving signal to X1 and leave X2 open-circuited (Figure 9D).



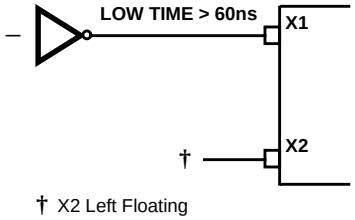
a.) QUARTZ CRYSTAL CLOCK DRIVER



c.) RC CIRCUIT CLOCK DRIVER



b.) LC TUNED CIRCUIT CLOCK DRIVER



† X2 Left Floating

d.) 0-4MHz INPUT FREQUENCY EXTERNAL CLOCK DRIVER CIRCUIT

FIGURE 9. CLOCK DRIVER CIRCUITS

HS-80C85RH Caveats

1. An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule also applies to inputs connected to a tri- state bus. The need for external pull-up resistors during tri-state bus conditions is eliminated by the presence of regenerative latches on the following HS-80C85RH output pins: AD0-AD7, A8-A15, and IO/M. Figure 10 depicts an output and corresponding regenerative latch. When the output driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the tri-state condition. A transient drive current of approximately ±1.0mA at 0.5 VDD for 10nsec is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during tri-state conditions.
2. The $\overline{RD}$ and $\overline{WR}$ pins of the HS-80C85RH contain internal dynamic pull-up transistors to avoid spurious selection of memory devices when the $\overline{RD}$ and $\overline{WR}$ pins assume the high impedance state. This eliminates the need for external resistive pull-ups on these pins.
3. The $\overline{RESET\ IN}$ and X1 inputs on the HS-80C85RH are schmit trigger inputs. This eliminates the possibility of internal oscillations in response to slow rise time input signals at these pins.
4. A high frequency bypass capacitor of approximately 0.1 µF should be connected between VDD and GND to shunt power supply transients.
5. The HS-80C85RH is functional within 10 input clock cycles after application of power (assuming that reset has been asserted from power-on). Start up conditions in the crystal controlled oscillator mode must also account for the characteristics of the oscillator.

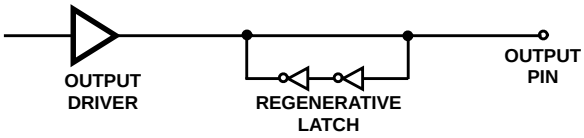


FIGURE 10. OUTPUT DRIVER AND LATCH FOR PINS ADO-AD7, A8-A15 AND IO/$\overline{M}$.

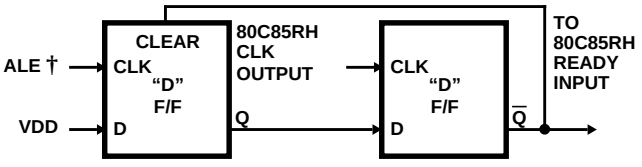
Generating An HS-80C85RH Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 11 may be used to insert one WAIT state in each HS-80C85RH machine cycle.

The D flip-flops should be chosen so that:

1. CLK is rising edge-triggered
2. CLEAR is low-level active.

The READY line is used to extend the read and write pulse lengths so that the 80C85RH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.



†ALE and CLK (OUT) should be buffered if CLK input of latch exceeds 80C85RH IOL or IOH.

FIGURE 11. GENERATION OF A WAIT STATE FOR HS-80C85RH CPU.

System Interface

The HS-80C85RH family includes memory components, which are directly compatible to the HS-8OC8SRH CPU. For example, a system consisting of the three radiation-hardened chips, HS-80C85RH, HS-81C56RH, and HS-83C55RH will have the following features:

1. 2K Bytes ROM
2. 256 Bytes RAM
3. 1 Timer/Counter
4. 4 8-bit I/O Ports
5. 1 6-bit I/O Port
6. 4 Interrupt Levels
7. Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 12.

In addition to standard 1/0, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 13 shows the system configuration of Memory Mapped I/O using HS-80C85RH.

The HS-80C85RH CPU can also interface with the standard radiation-hardened memory that does not have the multiplexed address/data bus. It will require use of the HS-82C12RH (8-bit latch) as shown in Figure 14.

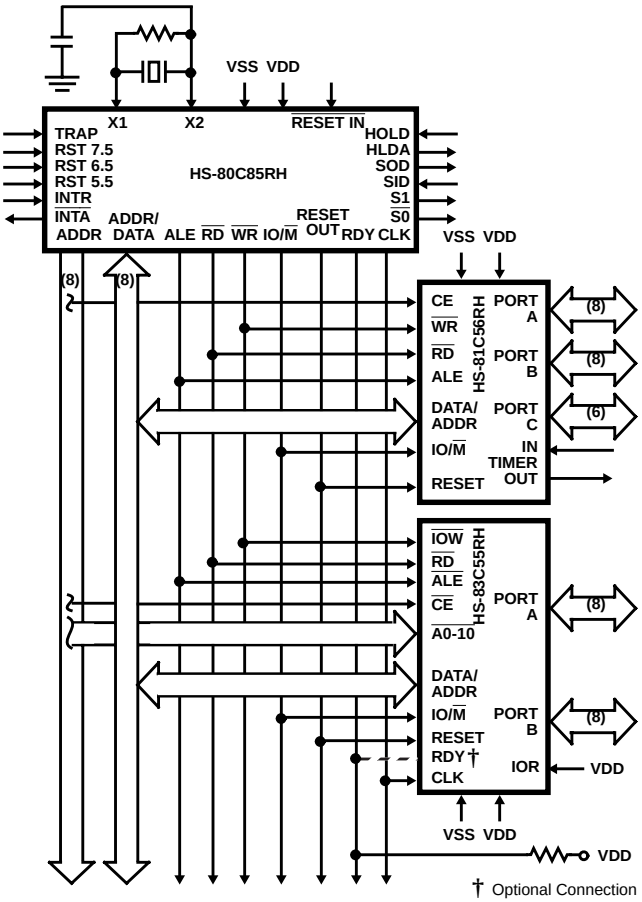
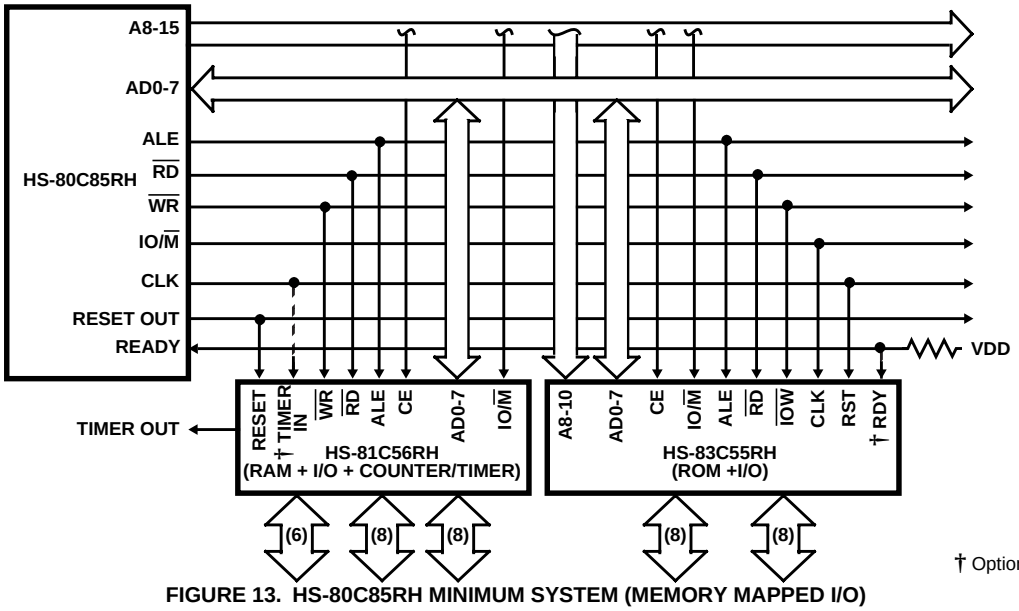


FIGURE 12. HS-80C85RH MINIMUM SYSTEM (STANDARD I/O TECHNIQUE)



† Optional Connection

FIGURE 13. HS-80C85RH MINIMUM SYSTEM (MEMORY MAPPED I/O)

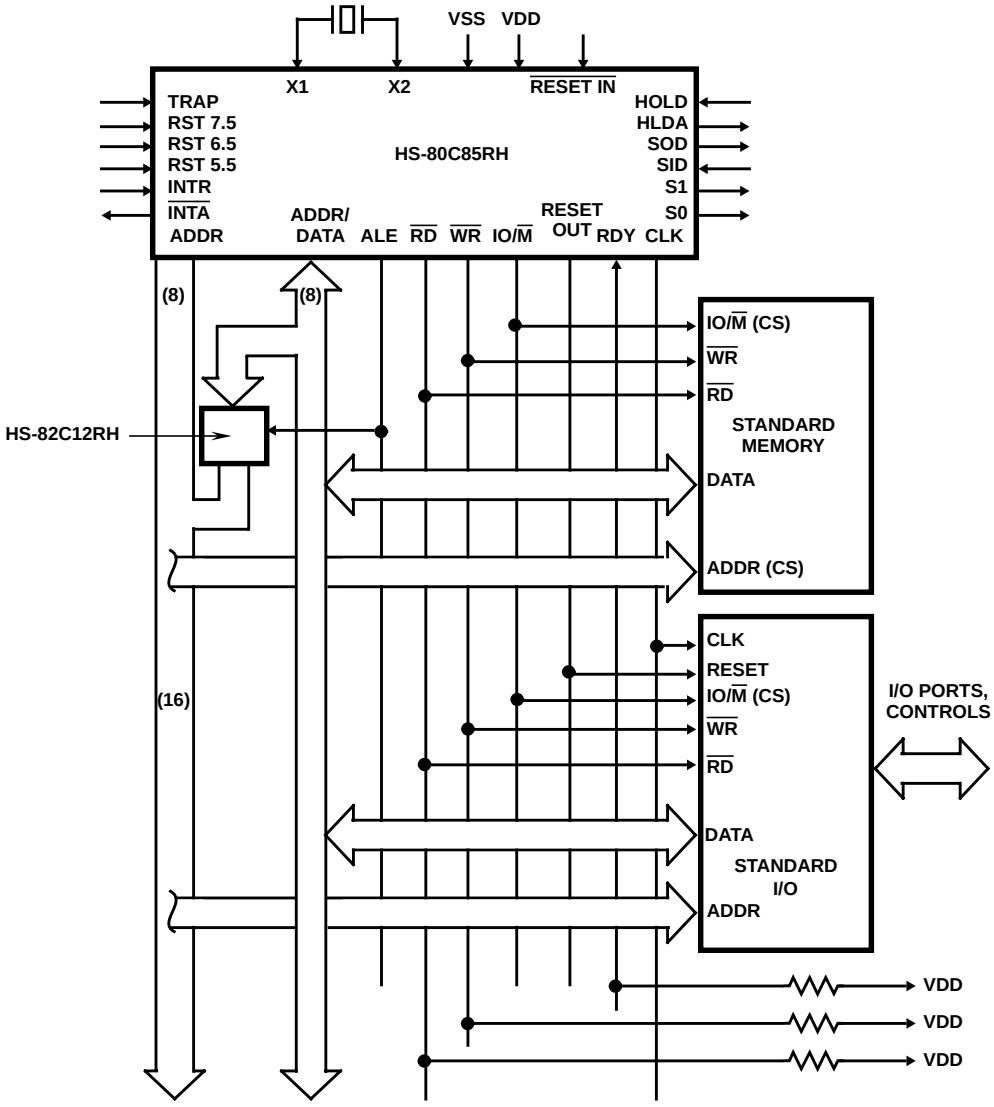


FIGURE 14. HS-80C85RH SYSTEM (USING STANDARD MEMORIES)

Basic System Timing

The HS-80C85RH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 15 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S1, S0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 10.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ are used as command lines since they become active when the transfer of data is to take place.

TABLE 10. HS-80C85RH MACHINE CYCLE CHART

MACHINE CYCLE			STATUS			CONTROL		
			IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)		0	1	1	0	1	1
Memory Read	(MR)		0	1	0	0	1	1
Memory Write	(MW)		0	0	1	1	0	1
I/O Read	(IOR)		1	1	0	0	1	1
I/O Write	(IOW)		1	0	1	1	0	1
Acknowledge of INTR	(INA)		1	1	1	1	1	0
Bus Idle	(BI)	DAD	0	1	0	1	1	1
		Ack. of RST, TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 11.

TABLE 11. HS-80C85RH MACHINE STATE CHART

MACHINE STATE	STATUS & BUSES				CONTROL		
	S1, S0	IO/$\overline{M}$	A8-15	AD0-7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	$\overline{ALE}$
T1	X	X	X	X	1	1	1†
T2	X	X	X	X	X	X	0
TWAIT	X	X	X	X	X	X	0
T3	X	X	X	X	X	X	0
T4	1	0††	X	TS	1	1	0
T5	1	0††	X	TS	1	1	0
T6	1	0††	X	TS	1	1	0
TRESET	X	TS	TS	TS	TS	1	0
THALT	0	TS	TS	TS	TS	1	0
THOLD	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

† ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

†† IO/M = 1 during T4, T6 of INA machine cycle.

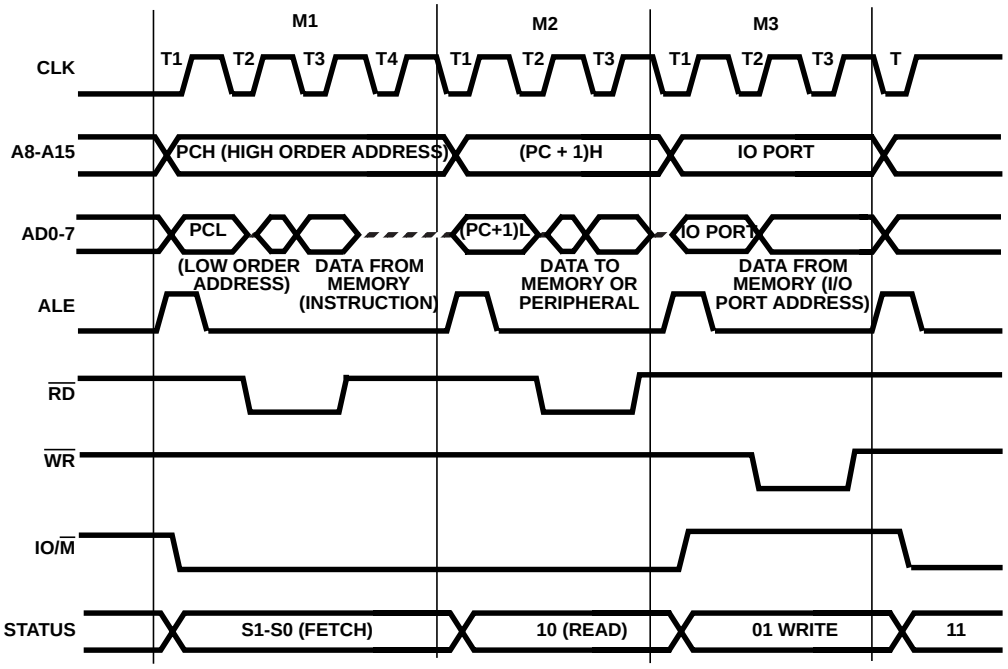


FIGURE 15. 80C85RH BASIC SYSTEM TIMING

Metallization Topology

DIE DIMENSIONS:

229 mils x 240 mils x 14 mils ±1 mil

METALLIZATION:

Type: SiAl

Thickness: 11kÅ ±2kÅ

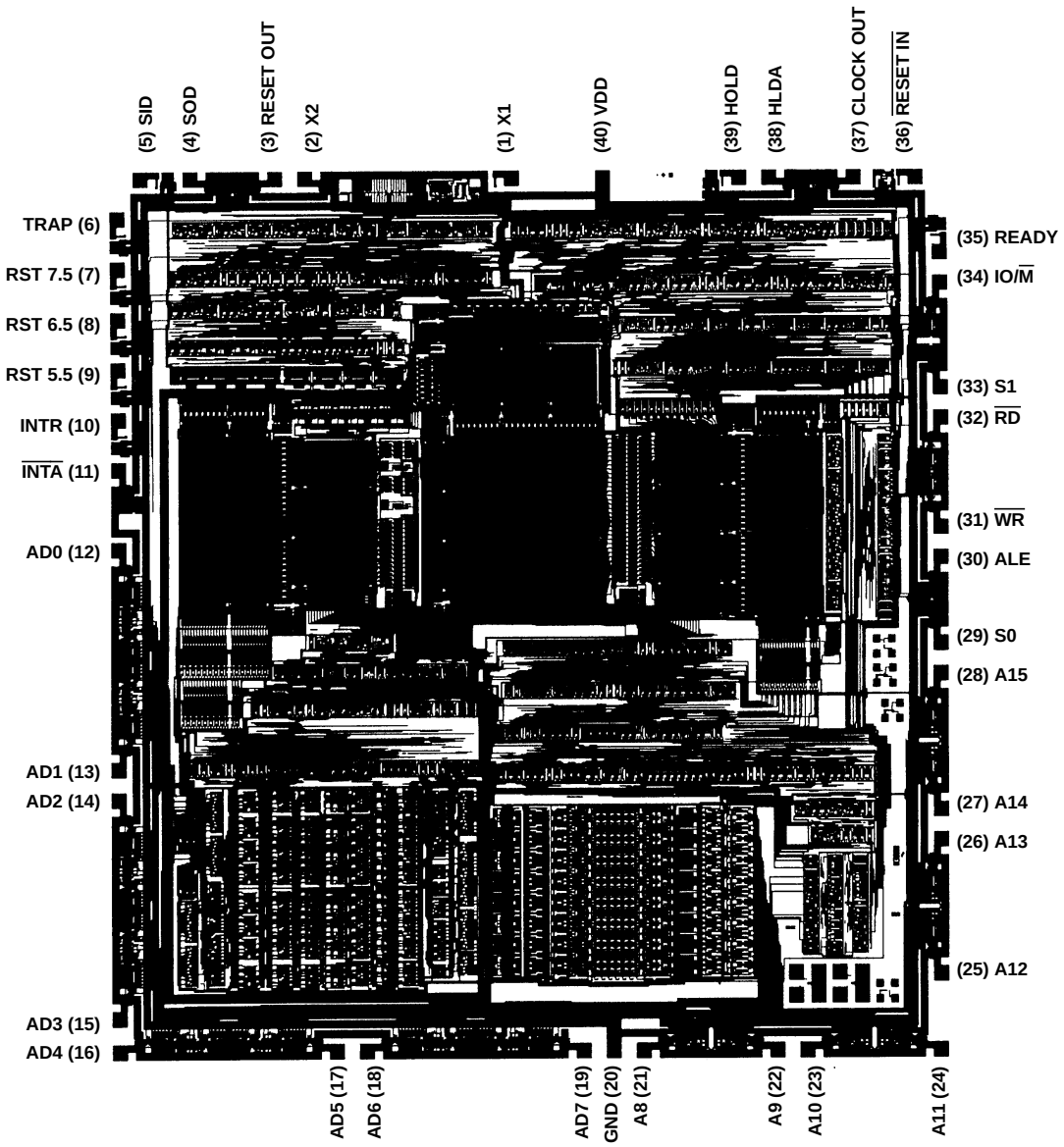
GLASSIVATION:

Type: SiO_2

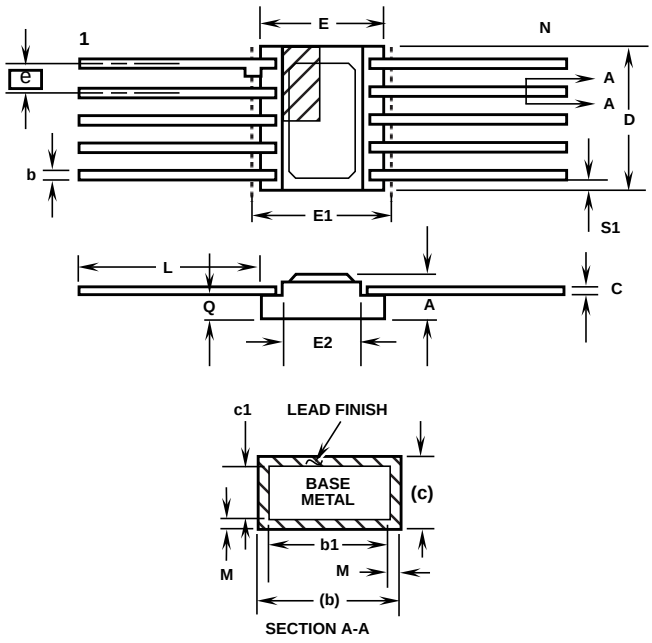
Thickness: 8kÅ ±1kÅ

Metallization Mask Layout

HS-80C85RH



Packaging



K42.A TOP BRAZED
42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.100	-	2.54	-
b	0.017	0.025	0.43	0.64	-
b1	0.017	0.023	0.43	0.58	-
c	0.007	0.013	0.18	0.33	-
c1	0.007	0.010	0.18	0.25	-
D	1.045	1.075	26.54	27.31	3
E	0.630	0.650	16.00	16.51	-
E1	-	0.680	-	17.27	3
E2	0.530	0.550	13.46	13.97	-
e	0.050 BSC		1.27 BSC		11
k	-	-	-	-	-
L	0.320	0.350	8.13	8.89	-
Q	0.045	0.065	1.14	1.65	8
S1	0.000	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	42		42		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.
11. The basic lead spacing is 0.050 inch (1.27mm) between center lines. Each lead centerline shall be located within ±0.005 inch (0.13mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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