

512Kx8 Static RAM CMOS, Module

The EDI8M8512C is a 4096K bit CMOS Static RAM based on four 128Kx8 Static RAMs mounted on a multi-layered ceramic substrate.

Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address (A17 & A18) to select one of the 128Kx8 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

A Low Power version with Data Retention function (EDI8M8512LP) is also available.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8512C requires no clocks or refreshing for operation.

EDI Military Modules are built with RAMs that are compliant to MIL-STD-883, paragraph 1.2.1.

Features

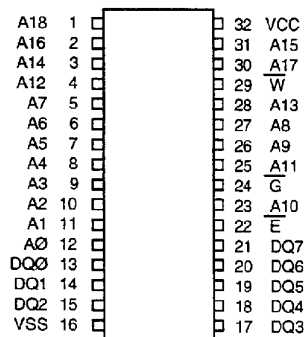
512Kx8 bit CMOS Static Random Access Memory

- Access Times
Commercial: 25 thru 150ns
Military: 35 thru 150ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

32 pin DIP, JEDEC Approved Pinout

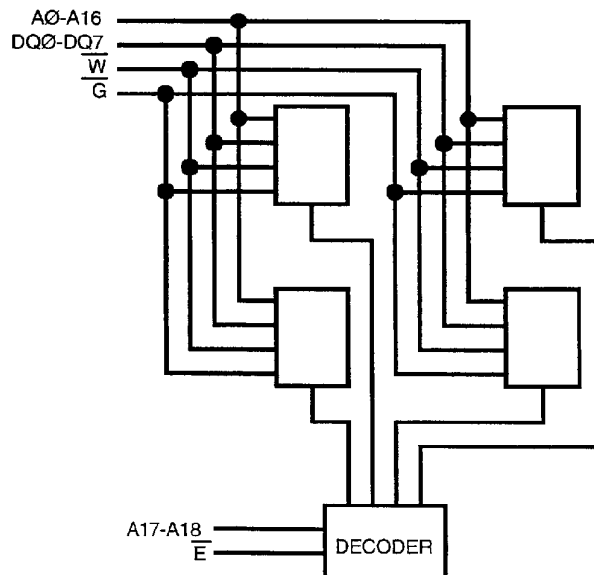
- Ceramic LCCs on Ceramic Substrate, No. 154
- Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram



Pin Names

A0-A18	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS -0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Commercial 0°C to +70°C
 Industrial -40°C to +85°C
 Military -55°C to +125°C
 Storage Temperature
 Power Dissipation 2 Watts
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load 25-55ns 1TTL, CL = 30pF
 70-150ns 1TTL, CL = 100pF
 (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Temp Range	Min	Typ*			Max			Units
					25-30	35-55	70-150	25-30	35-55	70-150	
Operating Power	ICC1	$\bar{W}, \bar{E} = \text{VIL}, \text{I/O} = 0\text{mA}$	C/I	--	240	190	70	350	300	130	mA
Supply Current		Min Cycle	Mil	--	--	190	80	--	300	130	mA
Standby (TTL) Power	ICC2	$\bar{E} \geq \text{VIH}, \text{VIN} \leq \text{VIL}$	C/I	--	60	60	10	125	125	55	mA
Supply Current		$\text{VIN} \geq \text{VIH}$	Mil	--	--	60	20	--	125	55	mA
Full Standby Power	ICC3	$\bar{E} \geq \text{VCC} - 0.2\text{V}$	C/I-C		10	10	2	55	55	5	mA
Supply Current		$\text{VIN} \geq \text{VCC} - 0.2\text{V}$ or $\text{VIN} \leq 0.2\text{V}$	C/I-LP	--	5	5	0.04	35	35	0.4	mA
			Mil-C	--	--	10	5	--	90	10	mA
			Mil-LP	--	--	5	2	--	70	5	mA
Input Leakage Current	ILI	$\text{VIN} = 0\text{V to VCC}$		--	--	--	--	--	±10	--	µA
Output Leakage Current	ILO	$\text{V I/O} = 0\text{V to VCC}$		--	--	--	--	--	±10	--	µA
Output High Voltage	VOH	$\text{IOH} = -1.0\text{mA} (<70\text{ns} = -4.0\text{mA})$		2.4	--	--	--	--	--	--	V
Output Low Voltage	VOL	$\text{IOL} = 2.1\text{mA} (<70\text{ns} = 8.0\text{mA})$		--	--	--	--	--	0.4	--	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{G}	\bar{E}	\bar{W}	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	50	pF
Chip Enable Line	CC	20	pF
Write and Output Enable Lines	CW	45	pF

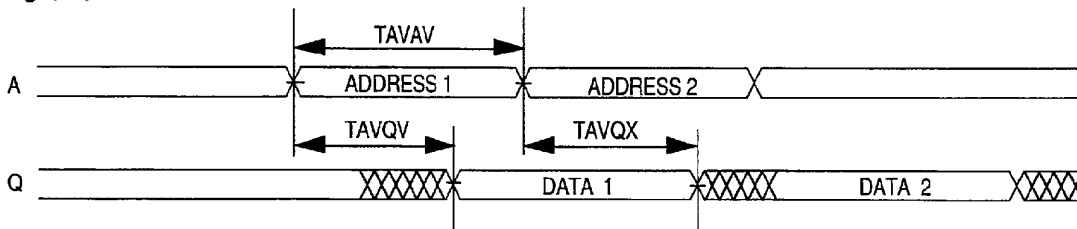
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

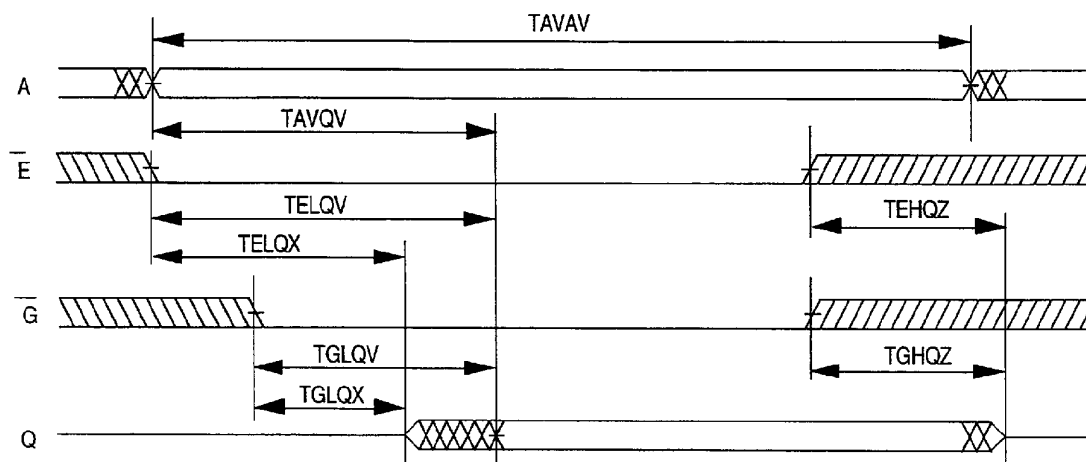
Parameter	Symbol		25ns		30ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	25		30		35		45		55		ns
Address Access Time	TAVQV	TAA		25		30		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		25		30		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		12		15		20		25		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		10		10		15		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		10		12		20		25		25	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High; G, E Low



Read Cycle 2
W High



(2)

Commercial, Industrial & Military

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AC Characteristics
Read Cycle

Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		120		150		ns
Address Access Time	TAVQV	TAA		70		85		100		120		150	ns
Chip Enable Access Time	TELQV	TACS		70		85		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		25		35		40		45		50	ns
Output Hold from Address Change	TAVQX	TOH	5		5		5		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		35		45		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		25		35		40		45		50	ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol		25ns		30ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	25		30		35		45		55		ns
Chip Enable to End of Write	TELWH	TCW	20		25		30		35		40		ns
	TELEH	TCW	20		25		30		35		40		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	20		25		30		35		40		ns
	TAVEH	TAW	20		25		30		35		40		ns
Write Pulse Width	TWLWH	TWP	20		20		25		35		40		ns
	TWLEH	TWP	20		20		25		35		40		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	15	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	TDW	12		15		15		25		25		ns
	TDVEH	TDW	12		15		15		25		25		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		3		ns

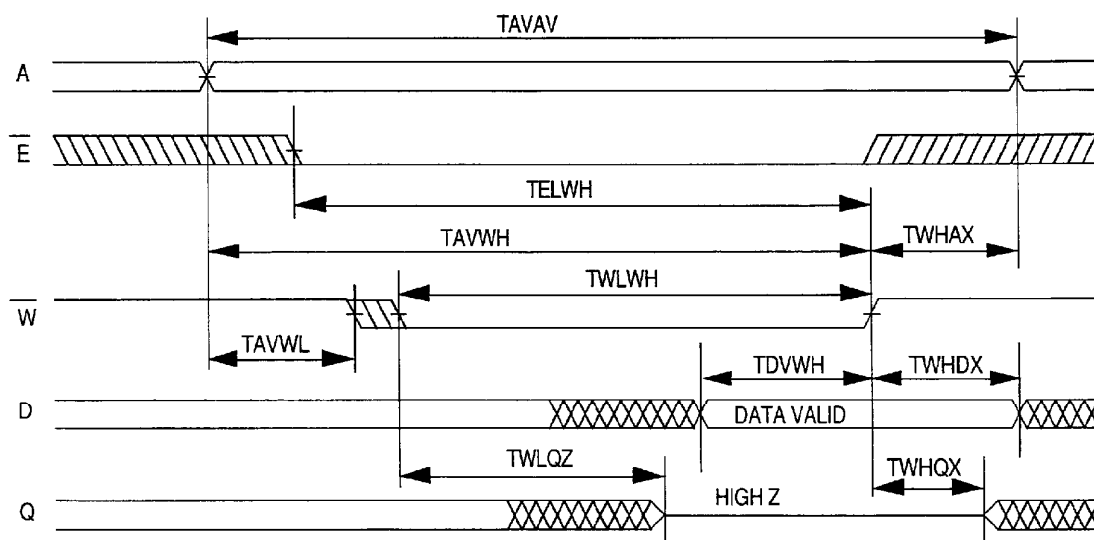
Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	70		85		100		120		150		ns
Chip Enable to End of Write	TELWH	TCW	65		70		80		100		110		ns
	TELEH	TCW	65		70		80		100		110		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	65		70		80		100		110		ns
	TAVEH	TAW	65		70		80		100		110		ns
Write Pulse Width	TWLWH	TWP	65		70		80		100		110		ns
	TWLEH	TWP	65		70		80		100		110		ns
Write Recovery Time	TWHAX	TWR	5		5		5		5		5		ns
	TEHAX	TWR	5		5		5		5		5		ns
Data Hold Time in High Z (1)	TWHDX	TDH	5		5		5		5		5		ns
	TEHDX	TDH	5		5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	0	45	0	50	ns
Data to Write Time	TDVWH	TDW	30		35		40		45		50		ns
	TDVEH	TDW	30		35		40		45		50		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		5		5		ns

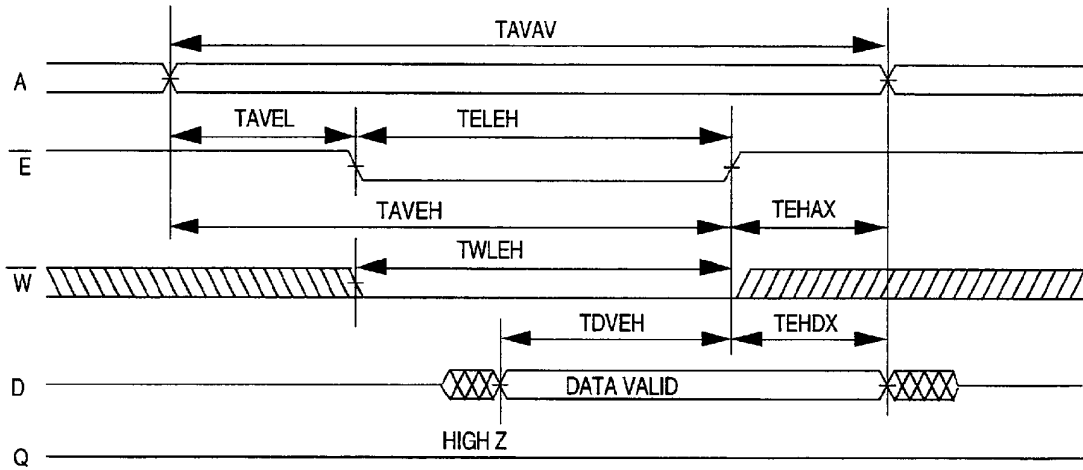
Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W Controlled



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Write Cycle 2
E Controlled



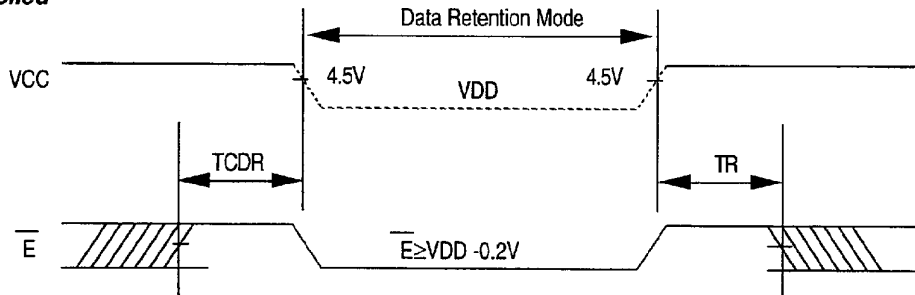
Data Retention Characteristics

ED18M8512LP
85-150ns only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max			Unit
						70°C	85°C	125°C	
Data Retention Voltage	VDD	$\bar{E} \geq VDD - 0.2V$ $VIN \geq VDD - 0.2V$		2	-	-	-	-	V
Data Retention Quiescent Current	ICCDR	or $VIN \leq 0.2V$							
25-55ns			2V	--	0.15	125	185	850	mA
			3V	-	0.30	4	4.5	9	mA
70-150ns			2V	-	10	125	185	850	μA
			3V	-	20	200	250	1100	μA
Chip Disable to Data Retention Time	TCDR			0		-	-	-	ns
Operation Recovery Time	TR			5		-	-	-	ms

*Read Cycle Time

**Data Retention
E Controlled**



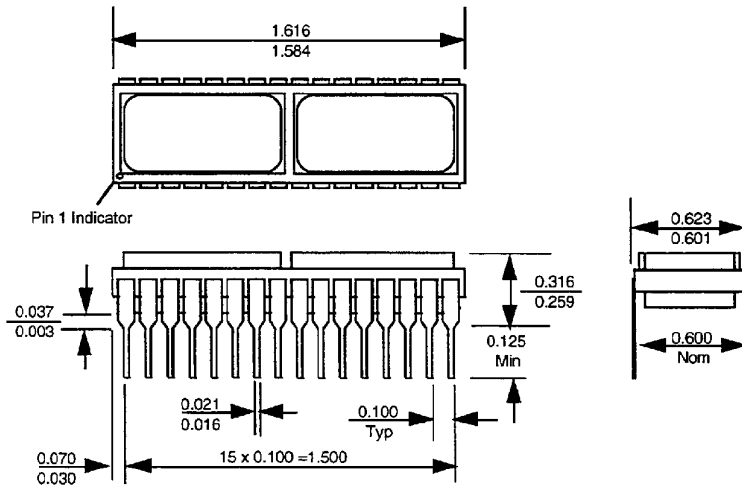
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Standard Power				
Part No.	Speed (ns)	Leads	Packag Style	No.
ED18M8512C25C6B	25*	32	0.6 DIP	154
ED18M8512C30C6B	30*	32	0.6 DIP	154
ED18M8512C35C6B	35	32	0.6 DIP	154
ED18M8512C45C6B	45	32	0.6 DIP	154
ED18M8512C55C6B	55	32	0.6 DIP	154
ED18M8512C70C6B	70	32	0.6 DIP	154
ED18M8512C85C6B	85	32	0.6 DIP	154
ED18M8512C100C6B	100	32	0.6 DIP	154
ED18M8512C120C6B	120	32	0.6 DIP	154
ED18M8512C150C6B	150	32	0.6 DIP	154

Low Power with Data Retention				
Part No.	Speed (ns)	Leads	Packag Style	No.Low
ED18M8512LP25C6C	25*	32	0.6 DIP	154
ED18M8512LP30C6C	30*	32	0.6 DIP	154
ED18M8512LP35C6C	35	32	0.6 DIP	154
ED18M8512LP45C6C	45	32	0.6 DIP	154
ED18M8512LP55C6C	55	32	0.6 DIP	154
ED18M8512LP70C6C	55	32	0.6 DIP	154
ED18M8512LP85C6B	85	32	0.6 DIP	154
ED18M8512LP100C6B	100	32	0.6 DIP	154
ED18M8512LP120C6B	120	32	0.6 DIP	154
ED18M8512LP150C6B	150	32	0.6 DIP	154

*Available in Commercial and Industrial Temperature Ranges.
 Note: Performance grade of part is designated by the last letter in the suffix to the part number. B = Military, I = Industrial, C = Commercial. To order an industrial version of parts listed above, e.g. change ED18M8512C85C6B to ED18M8512C85C6I.

Package No. 154
32 Pin Dual-in-line Package
Ceramic Leadless Chip Carriers
on Sidebrazed Ceramic Substrate



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