

128Kx32 CMOS High Speed Static RAM Module

T-46-23-14

Features

The EDI8M32128C is a high speed, high performance, four megabit density Static RAM module organized as 128Kx32 bits. The module contains four 128Kx8 SRAMs in a Ceramic Pin Grid Array Package.

Four Chip Enables and Write Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip and write enables.

Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

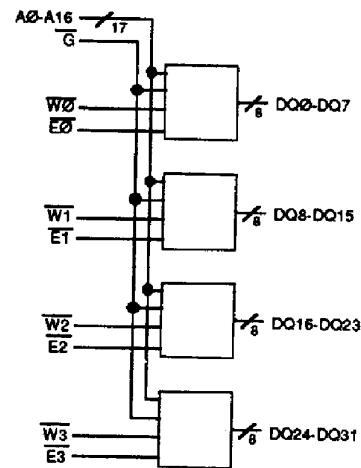
The EDI8M32128C is offered in a 66 lead PGA package which enables 4 megabits of memory to be placed in one square inch of space.

The device is available for both military and commercial applications.

- 128Kx32 bit CMOS Static Random Access Memory Module
 - Fast Access Times: 20, 25, 35, 45, and 55ns
 - Individual Byte Selects
 - Output Enable Function
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- 66 Lead Pin Grid Array Package, 1.1 in. sq. No. 168
 - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram

| | | | | | | | | | | | | | | | | | |
|-----------------|----|---|-----------------|----|---|-----------------|----|---|---|----|------|---|----|-----------------|---|----|------|
| DQ8 | 1 | • | $\overline{W1}$ | 12 | • | DQ15 | 23 | • | • | 34 | DQ24 | • | 45 | VCC | • | 56 | DQ31 |
| DQ9 | 2 | • | $\overline{E1}$ | 13 | • | DQ14 | 24 | • | • | 35 | DQ25 | • | 46 | $\overline{E3}$ | • | 57 | DQ30 |
| DQ10 | 3 | • | VSS | 14 | • | DQ13 | 25 | • | • | 36 | DQ26 | • | 47 | $\overline{W3}$ | • | 58 | DQ29 |
| A15 | 4 | • | DQ11 | 15 | • | DQ12 | 26 | • | • | 37 | A4 | • | 48 | DQ27 | • | 59 | DQ28 |
| A1 | 5 | • | A11 | 16 | • | \overline{G} | 27 | • | • | 38 | A3 | • | 49 | A7 | • | 60 | A10 |
| A16 | 6 | • | A12 | 17 | • | NC | 28 | • | • | 39 | NC | • | 50 | A6 | • | 61 | A9 |
| $\overline{A0}$ | 7 | • | A2 | 18 | • | $\overline{W0}$ | 29 | • | • | 40 | A14 | • | 51 | A5 | • | 62 | A8 |
| NC | 8 | • | VCC | 19 | • | DQ7 | 30 | • | • | 41 | A13 | • | 52 | $\overline{W2}$ | • | 63 | DQ23 |
| DQ0 | 9 | • | $\overline{E0}$ | 20 | • | DQ6 | 31 | • | • | 42 | DQ16 | • | 53 | $\overline{E2}$ | • | 64 | DQ22 |
| DQ1 | 10 | • | NC | 21 | • | DQ5 | 32 | • | • | 43 | DQ17 | • | 54 | VSS | • | 65 | DQ21 |
| DQ2 | 11 | • | DQ3 | 22 | • | DQ4 | 33 | • | • | 44 | DQ18 | • | 55 | DQ19 | • | 66 | DQ20 |



Pin Names

| | |
|--------------------|--------------------------|
| A0-A16 | Address Inputs |
| $\overline{E0-E3}$ | Chip Enables |
| $\overline{W0-W3}$ | Write Enables |
| \overline{G} | Output Enable |
| DQ0-DQ31 | Common Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |
| NC | No Connection |

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Commercial and Military

EDI8M32128C Rev. 1.0 6/92 367

Ordering Information

Military

| Part No. | Speed ns | Leads | Package Style | No. |
|-----------------|---------------------|--------------|--------------------------|------------|
| EDI8M32128C20GB | 20 | 66 | PGA | 168 |
| EDI8M32128C25GB | 25 | 66 | PGA | 168 |
| EDI8M32128C35GB | 35 | 66 | PGA | 168 |
| EDI8M32128C45GB | 45 | 66 | PGA | 168 |
| EDI8M32128C55GB | 55 | 66 | PGA | 168 |

Commercial

| Part No. | Speed ns | Leads | Package Style | No. |
|-----------------|---------------------|--------------|--------------------------|------------|
| EDI8M32128C20GC | 20 | 66 | PGA | 168 |
| EDI8M32128C25GC | 25 | 66 | PGA | 168 |
| EDI8M32128C35GC | 35 | 66 | PGA | 168 |
| EDI8M32128C45GC | 45 | 66 | PGA | 168 |
| EDI8M32128C55GC | 55 | 66 | PGA | 168 |