## Features

DSP Memory Solution
- Texas Instruments TMS320C54x

3.3V Operating Supply Voltage

Access Times of 10, 12 and 15ns

Single Write Control and Output Enable Lines

One Chip Enable Line per Memory Bank

50% Space Savings vs. Monolithic TSOPs

Upgrade Path Available in Same Footprint

Multiple VCC and VSS Pins

Reduced Inductance and Capacitance

74 pin BGA, JEDEC MO-151

### *TMS320C54x External SRAM Memory Solution*

The EDI8L21664VxxBC is a 3.3V, 2x64Kx16 SRAM constructed with two 64Kx16 die mounted on a multi-layer laminate substrate. The device is packaged in a 74 lead, 15mm by 15mm, BGA.

Operating with a 3.3V power supply and with access times as fast as 10ns, the device allows the user to develop a fast external memory for Texas Instuments' TMS320C54x DSP.

The device consists of two separate banks of 64Kx16 of memory. Each bank has a separate Chip Enable pin and higher order address select pin. Bank 'A' is controlled using CE1\ and A15A. Bank 'B' is controlled using CE2\ and A15B. The two banks have common I/Os (DQ0-15) and control lines (WE\ and G\).

## Pin Configurations

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VCC | VCC | DQ15 | DQ14 | VCC | DQ13 | DQ11 | DQ9 | DQ8 | N/C | A |
| B | VSS | VCC | VCC | VSS | VSS | VCC | DQ12 | DQ10 | DQ4 | VCC | VCC | B |
| C | VSS | VSS | | | | VCC | | | | VSS | VCC | C |
| D | VSS | VSS | | | | | | | | VSS | VCC | D |
| E | VSS | VSS | | | | | | | | VSS | VCC | E |
| F | A15A | CE1\ | | | | | | | | DQ3 | DQ7 | F |
| G | N/C | WE\ | | | | | | | | DQ5 | DQ0 | G |
| H | VSS | CE2\ | | | | | | | | DQ6 | DQ1 | H |
| J | VSS | A14 | | | | VCC | | | | DQ2 | N\C | J |
| K | VSS | A12 | VCC | A10 | A8 | VSS | A6 | A4 | A2 | A0 | G\ | K |
| L | A15B | A13 | VCC | A11 | A9 | VSS | A7 | VSS | A5 | A3 | A1 | L |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

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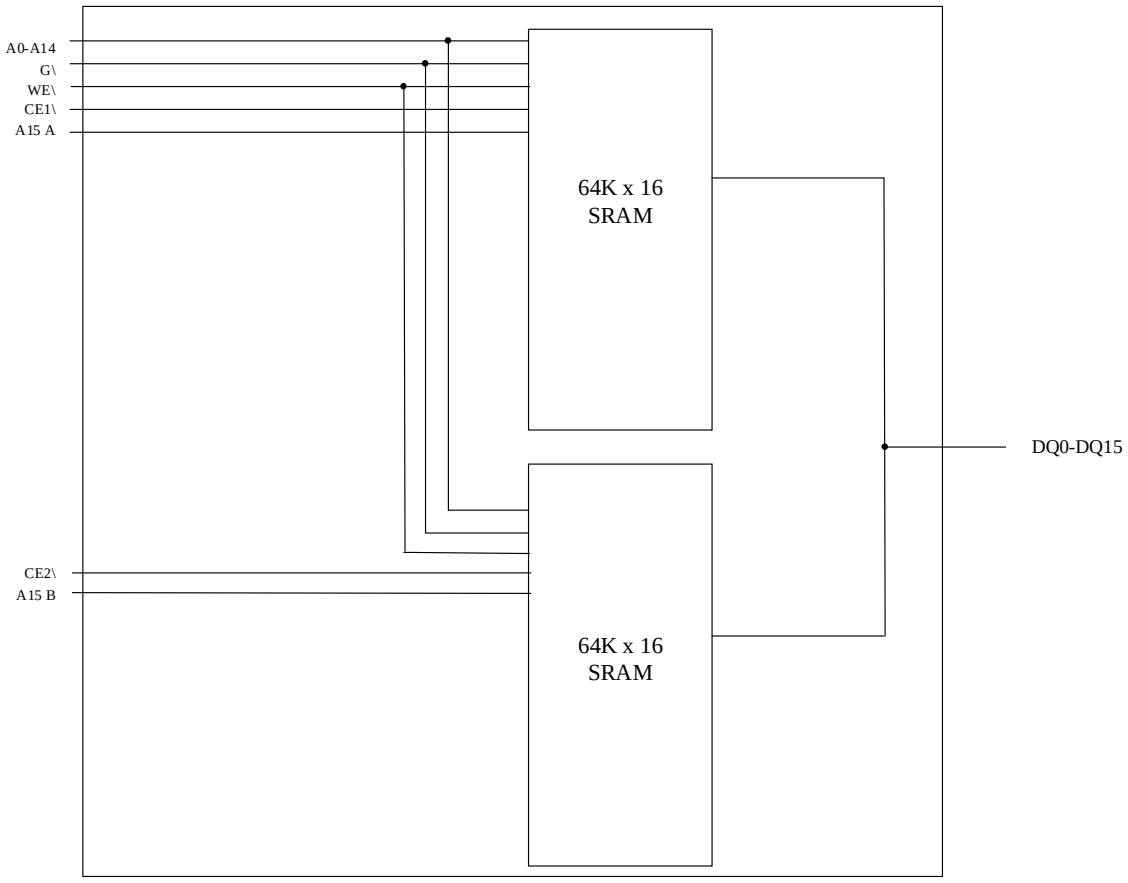
## Block Diagram




## Pin Descriptions

| Pin | Symbol | Type | Description |
|---|---|---|---|
| | A0-A14 | Input | Addresses |
| | A15A | Input | Addresses: A15 on Bank 'A' of memory |
| | A15B | Input | Addresses: A15 on Bank 'B' of memory |
| | WE\ | Input | Write Enable: This active LOW input allows a full 16-bit WRITE to occur. |
| | CE1\ | Input | Chip Enable: This active LOW input is used to enable the 'A' Bank of the device. |
| | CE2\ | Input | Chip Enable: This active LOW input is used to enable the 'B' Bank of the device. |
| | G\ | Input | Output Enable: This active LOW asynchronous input enables the data output drivers. |
| Various | DQ0-15 | Input/Output | Data Inputs/Outputs |
| Various | Vcc | Supply | Core power supply: +3.3V -5%/+10% |
| Various | Vss | Ground | Ground |

## Absolute Maximum Ratings*

| | |
|---|---|
| Voltage on Vcc Supply Relative to Vss | -0.5V to 4.6V |
| $V_{IN}$ | -0.5V to Vcc+0.5V |
| Storage Temperature | -55°C to +125°C |
| Junction Temperature | +125°C |
| Power Dissipation | 3 Watts |
| Short Circuit Output Current (per I/O) | 50 mA |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|---|---|---|---|
| Address Lines | CA | 8 | pF |
| Data Lines | CD/Q | 17 | pF |
| Control Lines | CC | 15 | pF |

## Recommended DC Operating Conditions

| Description | Sym | Min | Max | Units |
|---|---|---|---|---|
| Input High Voltage | VIH | 2.2 | Vcc+0.5 | V |
| Input Low Voltage | VIL | -0.3 | 0.8 | V |
| Supply Voltage | Vcc | 3.0 | 3.6 | V |

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times (Max) | 1.5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | See Figure 1 |

Figure 1

## DC Electrical Characteristics

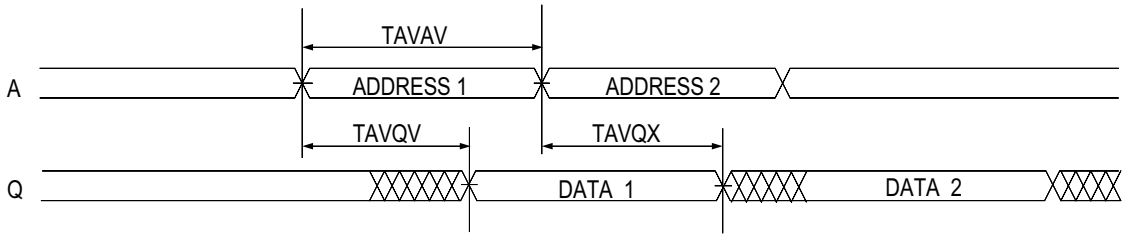
(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Power Supply Current: Operating | ICC1 | Device Selected; all inputs ≤VIL or ≥VIH; cycle time ≥tKC MIN; VCC=MAX; outputs open | -10ns<br>-12ns<br>-15ns | 380<br>360<br>260 | mA |
| CMOS Standby | ISB2 | Device deselected; VCC=MAX; all inputs ≤ VSS +0.2 or ≥ VCC -0.2; all inputs static; CLK frequency = 0 | | 60 | mA |
| TTL Standby | ISB3 | Device deselected; all inputs ≤VIL or ≥VIH; all inputs static; VCC=MAX; CLK frequency = 0 | | 120 | mA |
| Input Leakage Current | ILI | 0V≤VIN≤VCC | -5 | 5 | µA |
| Output Leakage Current | ILO | Output(s) disabled, 0V≤VOUT≤VCC | --5 | 5 | µA |
| Output High Voltage | VOH | IOH = -4.0mA | 2.4 | | V |
| Output Low Voltage | VOL | IOL = 8.0mA | | 0.4 | V |

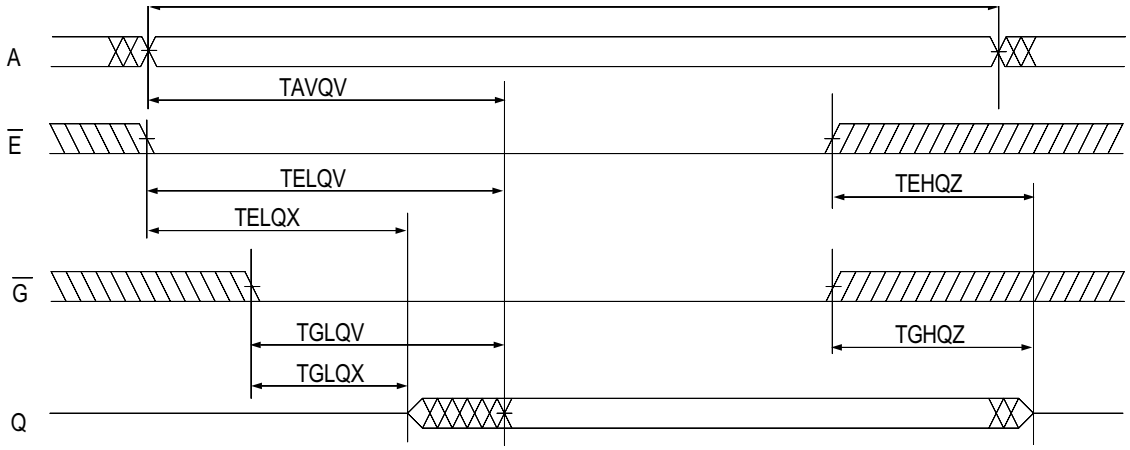
## AC Characteristics Read Cycle

| | Symbol | 10ns | | 12ns | | 15ns | | |
|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Units** |
| Read Cycle Time | tAVAV | 10 | | 12 | | 15 | | ns |
| Address Access Time | tAVQV | | 10 | | 12 | | 15 | ns |
| Chip Enable Access | tELQV | | 10 | | 12 | | 15 | ns |
| Output Hold from Address Change | tAVQX | 3 | | 4 | | 4 | | ns |
| Chip Enable to Output in Low-Z | tELQX | 3 | | 4 | | 4 | | ns |
| Chip Disable to Output in High-Z | tEHQZ | | 5 | | 6 | | 7 | ns |
| Output Enable access time | tGLQV | | 5 | | 6 | | 7 | ns |
| Output Enable to Output in Low-Z | tGLQX | 0 | | 0 | | 0 | | ns |
| Output Disable to Output in High-Z | tGHQZ | | 5 | | 6 | | 7 | ns |
| **Write Cycle** | | | | | | | | |
| Write Cycle Time | tAVAV | 10 | | 12 | | 15 | | ns |
| Chip Enable to End of Write | tELWH | 8 | | 8 | | 9 | | ns |
| Address valid to End of Write, with G\ HIGH | tAVGHWH | 8 | | 8 | | 9 | | ns |
| Address Setup Time | tAVWH | 0 | | 0 | | 0 | | ns |
| Address Hold from End of Write | tAVWH | 0 | | 0 | | 0 | | ns |
| Write Pulse Width | tWLWH | 10 | | 10 | | 11 | | ns |
| Write Pulse Width, with G\ HIGH | tWLGHWH | 8 | | 8 | | 9 | | ns |
| Data Setup Time | tDVWH | 6 | | 6 | | 7 | | ns |
| Data Hold Time | tWHDX | 0 | | 0 | | 0 | | ns |
| Write Disable to Output in Low-Z | tWHQX | 3 | | 4 | | 5 | | ns |
| Write Enable to Output in High-Z | tWLQZ | | 5 | | 6 | | 7 | ns |

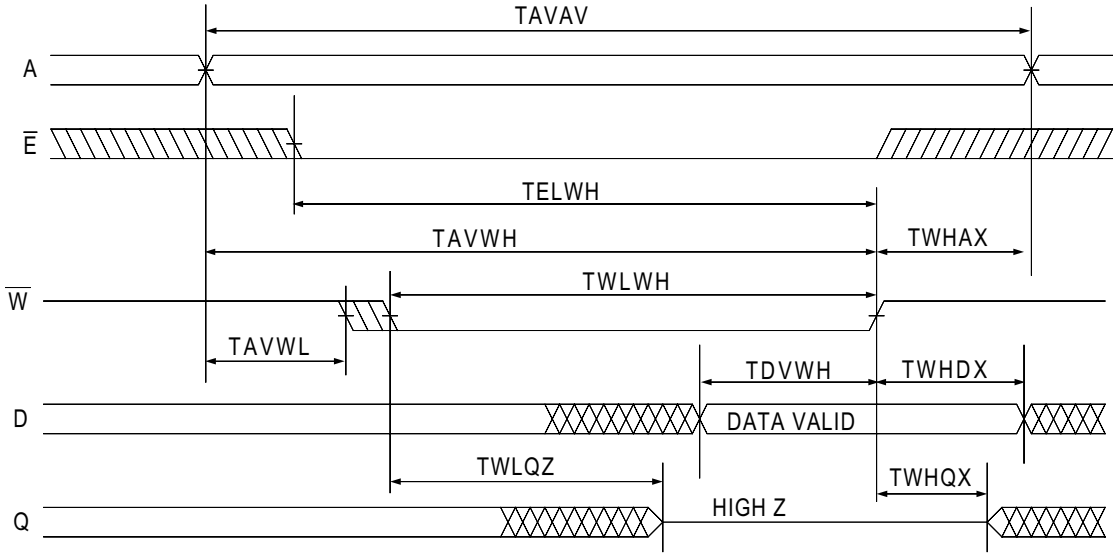
## Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



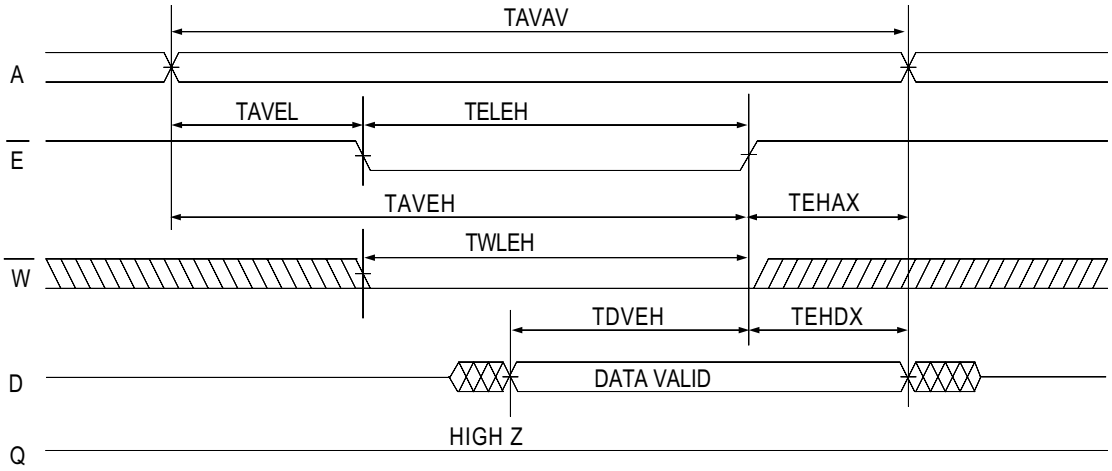

## Read Cycle 2 - $\overline{W}$ High



## Write Cycle 1 - $\overline{W}$ Controlled




## Write Cycle 2 - $\overline{E}$ Controlled



## Ordering Information

**Commercial Temperature Range (0°C to +70°C)**

| Part Number | Speed (ns) | Package No. |
|---|---|---|
| EDI8L21664V10BC | 10 | |
| EDI8L21664V12BC | 12 | |
| EDI8L21664V15BC | 15 | |

**Industrial Temperature Range (-40°C to +85°C)**

| Part Number | Speed (ns) | Package No. |
|---|---|---|
| EDI8L21664V15BI | 15 | |

## Package Description

***74 Pin BGA***
***JEDEC MO-151***