256Kx16 CMOS, High Speed Programmable, Static RAM Module

The EDI8F16256C is a 4096K-bit high speed CMOS Static RAM Module consisting of four (4) 256Kx4 Static RAMs in j-leaded (SOJ) chip carriers surface-mounted onto an epoxy laminate (FR-4) substrate. Four Chip Select lines are provided (one for each 256Kx4 array) allowing the user to configure the memory into a 256Kx16, 512Kx8 or 1024Kx4 organizations.

The EDI8F16256C is available with access times as fast as 25ns. The module is a high density, 48 pin DIP on 900 mil centers.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Multiple ground pins are provided for maximum noise immunity.

Fully asynchronous circuitry requires no clocks or refreshing for operation.

Features

High Density 4096K-bit CMOS Static Random Access Memory Module

- Access Times 20, 25, and 35ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Customer Configured Memory, as 256Kx16, 512Kx8 or 1024Kx4

48 Pin Dual-in-line Package, No. 56

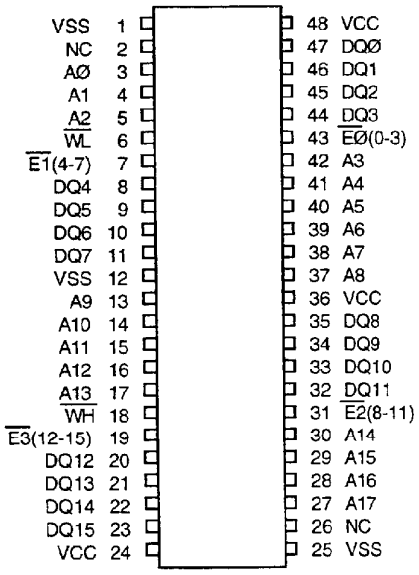
- Multiple Ground Pins for Maximum Noise Immunity

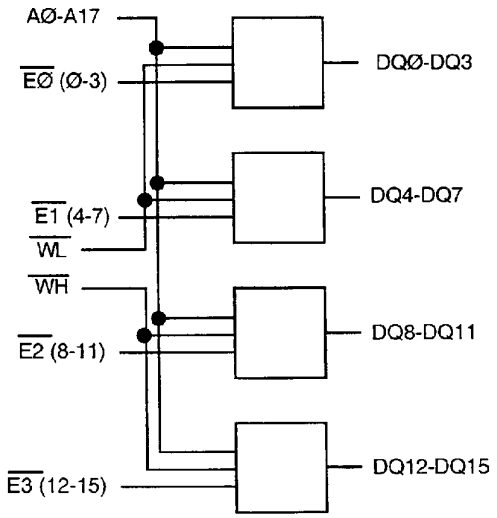
Single +5V (±10%) Supply Operation

Pin Names

AØ-A17	Address Inputs
$\overline{EØ}$-$\overline{E3}$	Chip Enables
$\overline{WL}$, $\overline{WH}$	Write Enables
DQØ-DQ15	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to+70°C
Industrial ..... -40°C to +85°C
Storage Temperature, Plastic ..... -55°C to +125°C
Power Dissipation ..... 8 Watts
Output Current ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Mode	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	x16	--	300	560	mA
			x8	--	200	400	mA
			x4	--	100	300	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	80	240	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		--	1	20	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±80	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±20	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E0}$-$\overline{E3}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Address Lines	CI	40	pF
Chip Enable Lines	CE	7	pF
Write Lines	CW	17	pF
Data Lines	CD/Q	15	pF

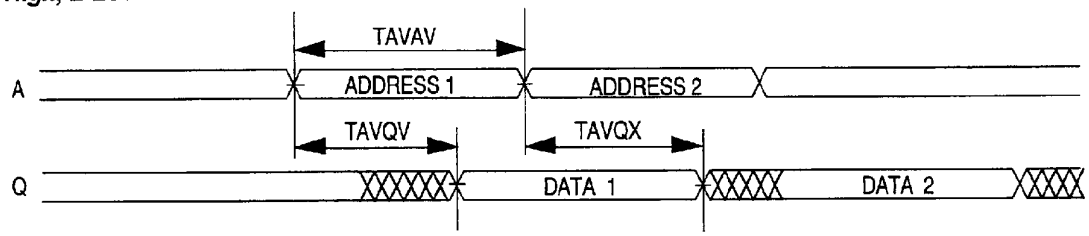
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

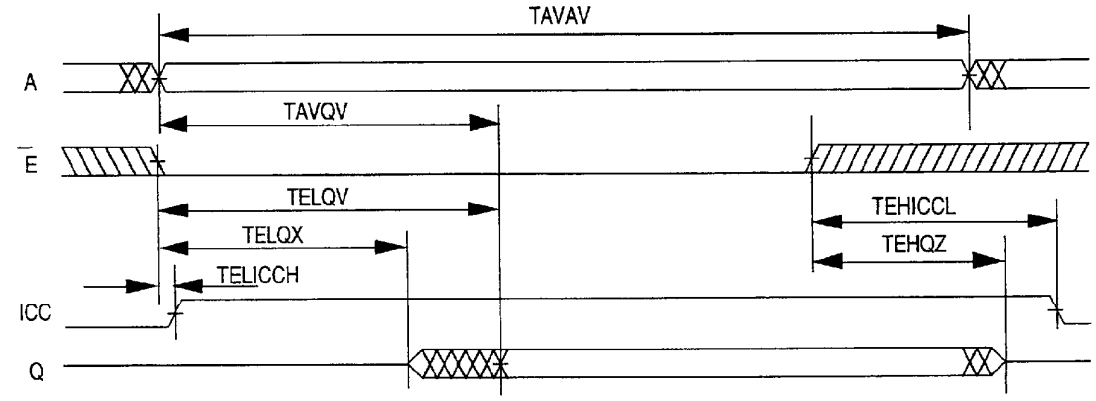
Parameter	Symbol JEDEC	Symbol Alt.		20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	TAVAV	TRC		20		25		35		ns
Address Access Time	TAVQV	TAA			20		25		35	ns
Chip Enable Access Time	TELQV	TACS			20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ			10		15		20	ns
Output Hold from Address Change	TAVQX	TOH		3		3		3		ns
Chip Enable to Power Up	TELICCH	TPU		0		0		0		ns
Chip Disable to Power Down	TEHICCL	TPD			20		25		35	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High, E Low



Read Cycle 2
W High

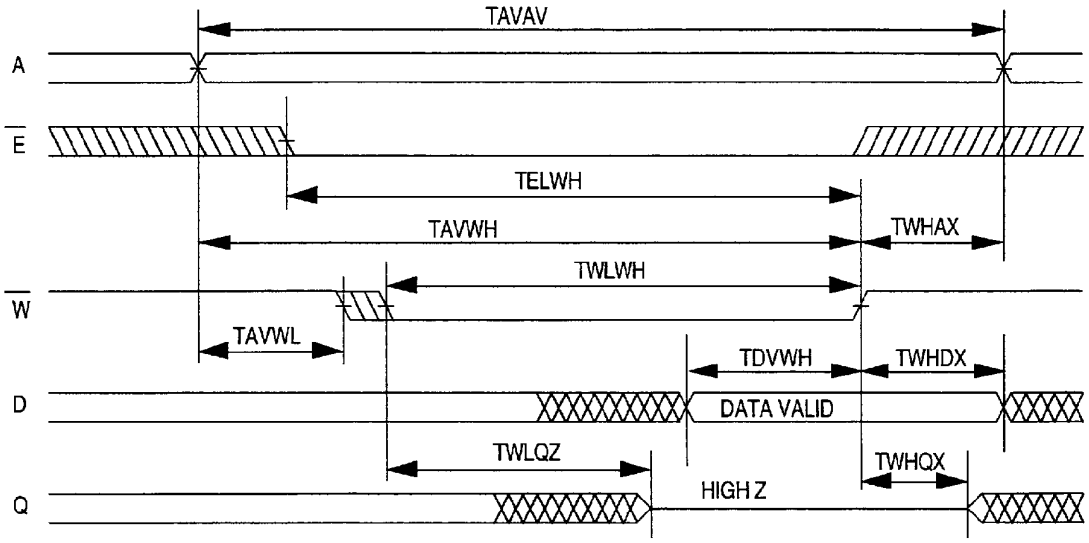


AC Characteristics
Write Cycle

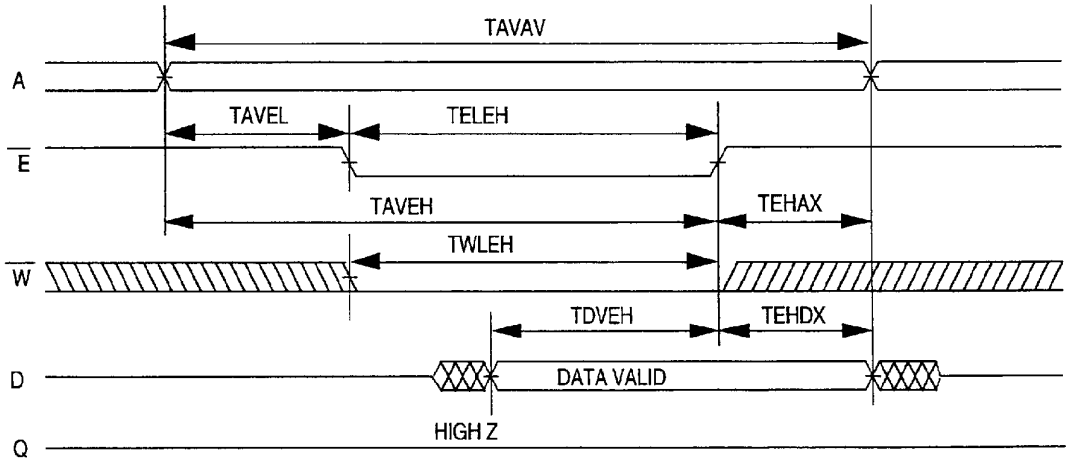
Parameter	Symbol JEDEC	Symbol Alt.		20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Write Cycle Time	TAVAV	TWC		20		25		35		ns
Chip Enable to	TELWH	TCW		15		20		30		ns
End of Write	TELEH	TCW		15		20		30		ns
Address Setup Time	TAVWL	TAS		0		0		0		ns
	TAVEL	TAS		0		0		0		ns
Address Valid to	TAVWH	TAW		15		20		30		ns
End of Write	TAVEH	TAW		15		20		30		ns
Write Pulse Width	TWLWH	TWP		15		20		30		ns
	TWLEH	TWP		15		20		30		ns
Write Recovery Time	TWHAX	TWR		0		0		0		ns
	TEHAX	TWR		0		0		0		ns
Data Hold Time	TWHDX	TDH		3		3		3		ns
	TEHDX	TDH		3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	8	0	10	0	15	ns
Data to Write Time	TDVWH	TDW		12		15		20		ns
	TDVEH	TDW		12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled

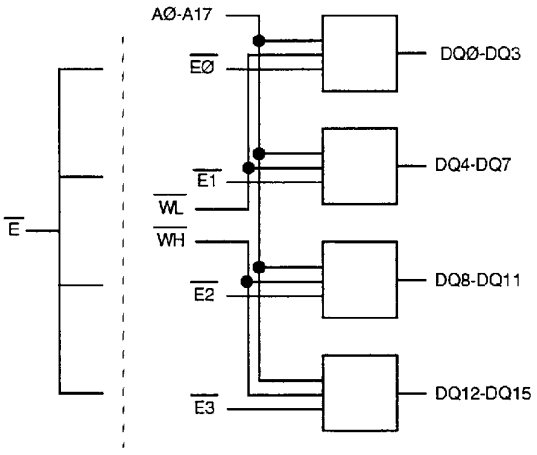


Write Cycle 2
$\overline{E}$ Controlled

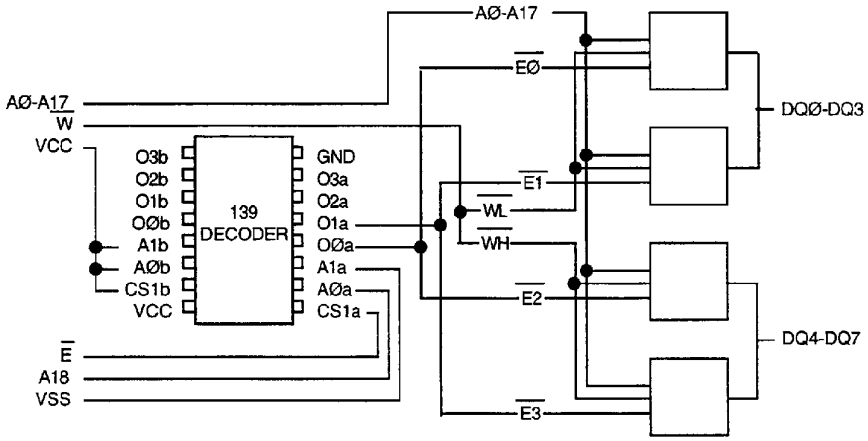


Device Configurations for 139 Decoder Applications

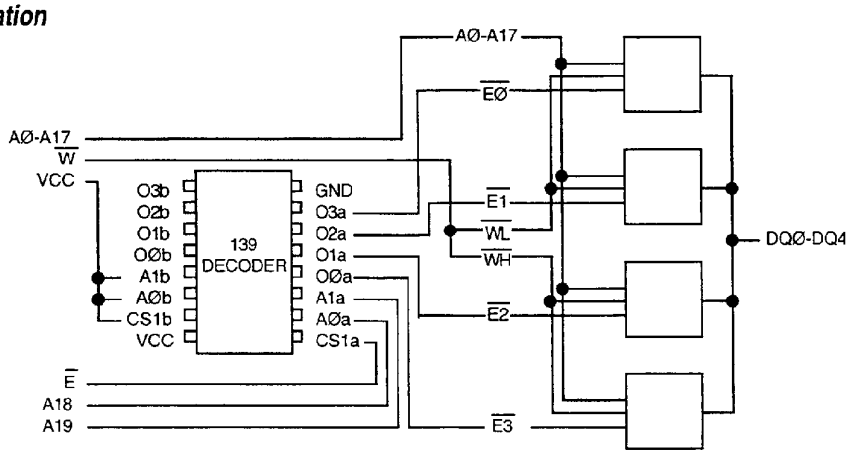
256Kx16 Configuration



512Kx8 Configuration

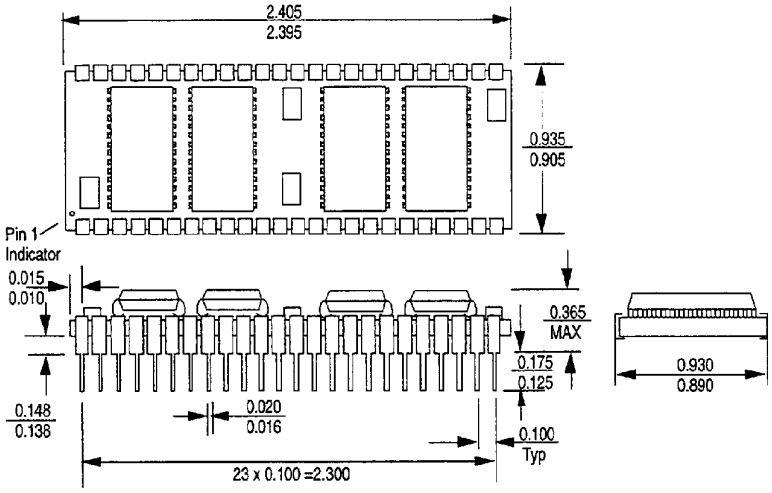


1024Kx4 Configuration



Package Description

Package No. 56
48 Pin Dual-in-line Package,
Plastic SOJ on an Epoxy Laminate (FR-4)
Substrate,
900 mils Wide



Ordering Information

Part No.	Speed (ns)	Temp. Range
EDI8F16256C20M9C	20	Commercial
EDI8F16256C25M9C	25	Commercial
EDI8F16256C35M9C	35	Commercial