128Kx48 3.3V SRAM MODULE

*ADVANCED**

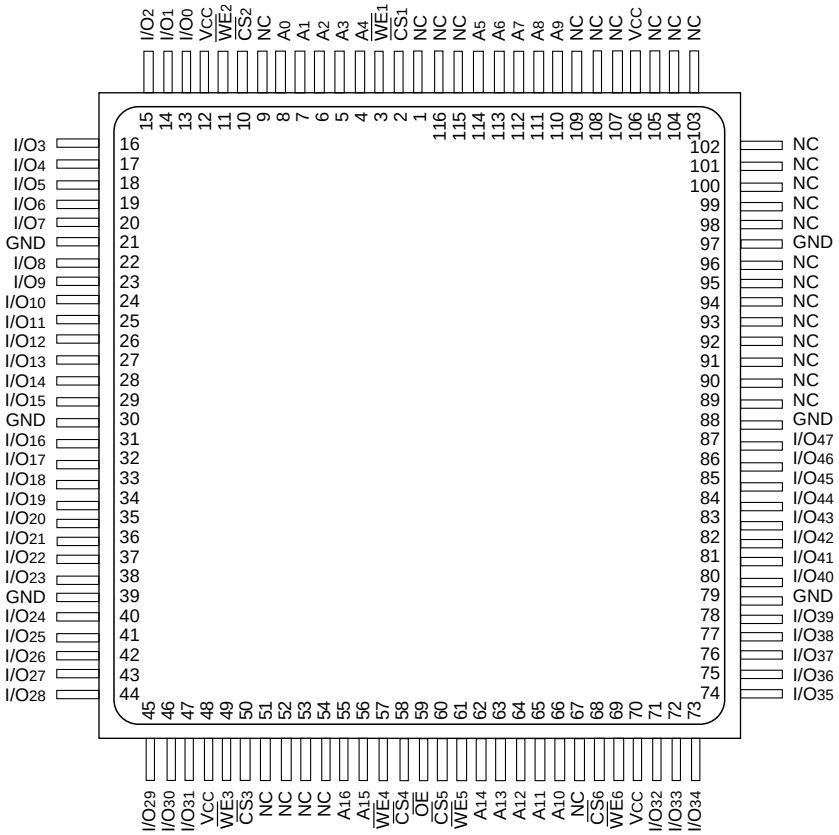
FEATURES

- Access Times 15, 17, 20, 25ns
- Packaging
  - 116 Lead, 40.0mm Hermetic CQFP (Package 504)
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- Organized as 128K x 48, Data Width is user configurable.
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs
- Weight
  WS128K48V-XG4WX - 20 grams typical

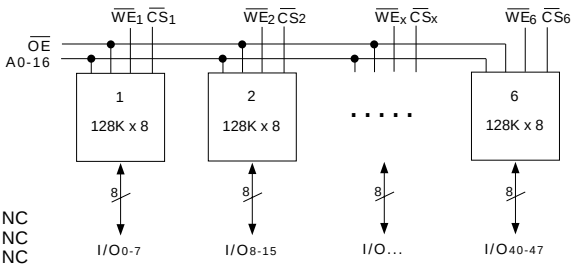
* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PIN CONFIGURATION FOR WS128K48V-XG4WX

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-47	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-6}$	Write Enables
$\overline{CS}_{1-6}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.6	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	100	pF
$\overline{WE}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{CS}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	100	pF

This parameter is guaranteed by design but not tested.

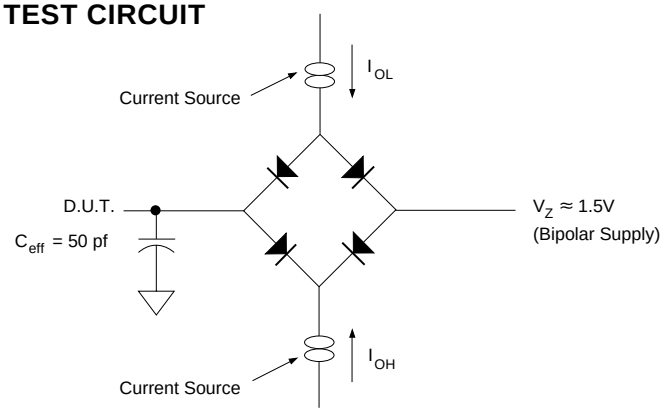
DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 3.6		750	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 3.6		48	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(VCC = 3.3V ±0.3V, TA = -55°C To +125°C)

Parameter Read Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max			
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25	ns
Output Enable to Output Valid	t_{OE}		10		10		12		15	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		10		10		12		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		10		10		12		12	ns

1. This parameter is guaranteed by design but not tested.

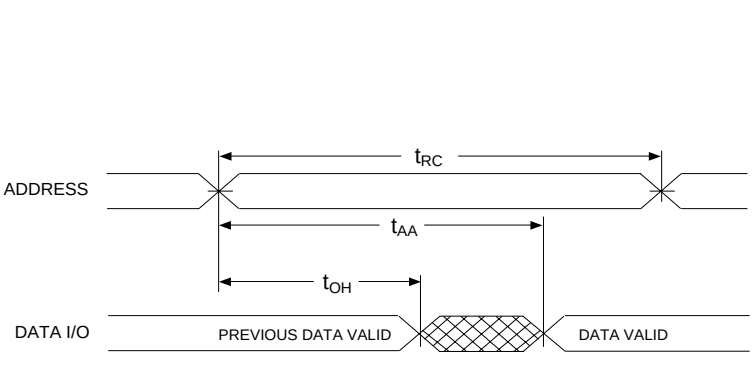
AC CHARACTERISTICS

(VCC = 3.3V ±0.3V, TA = -55°C To +125°C)

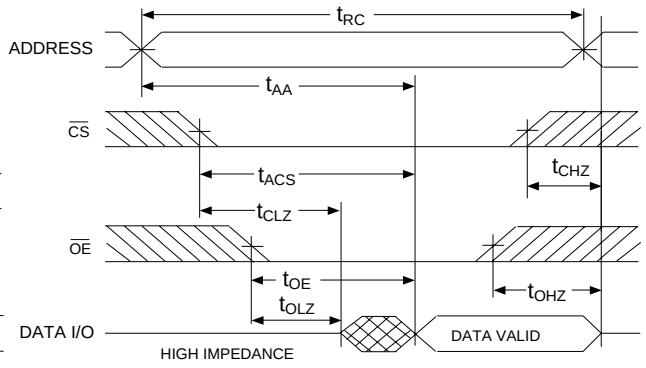
Parameter Write Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	14		14		15		20		ns
Address Valid to End of Write	t_{AW}	14		15		15		20		ns
Data Valid to End of Write	t_{DW}	10		10		12		15		ns
Write Pulse Width	t_{WP}	14		14		15		20		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		10		12		15	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

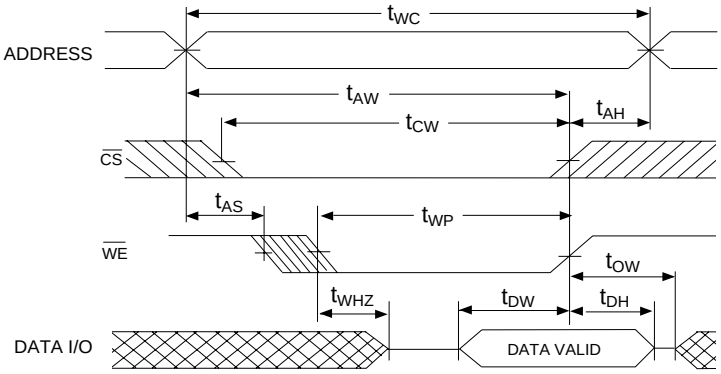


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



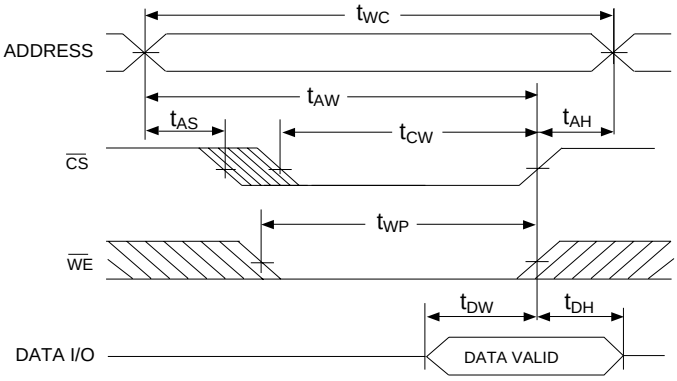
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



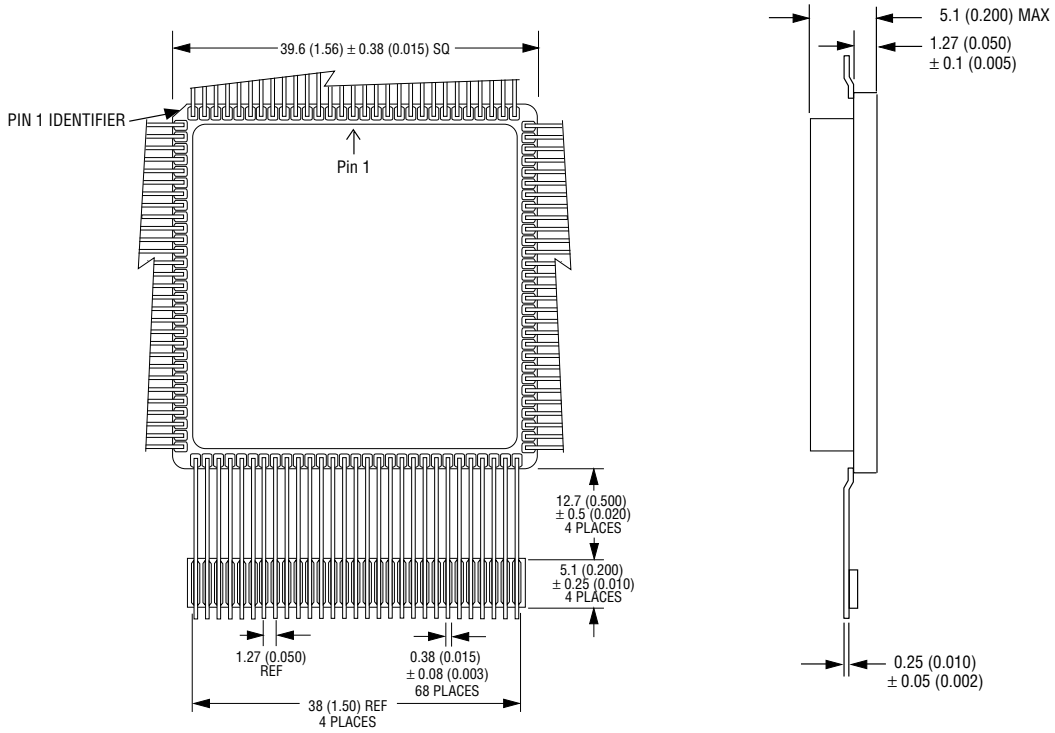
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 128K48 V - XXX G4W X

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to + 70°C

PACKAGE TYPE:

G4W = 116 Lead 40mm Ceramic Quad Flat Pack, CQFP (Package 504)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ±10%

ORGANIZATION, 128K x 48

SRAM

WHITE MICROELECTRONICS