



# 128Kx8 MONOLITHIC SRAM, SMD 5962-89598

## FEATURES

- Access Times of 70, 85, 100ns
- Available with Single Chip Selects (EDI88128) or Dual Chip Selects (EDI88130)
- 2V Data Retention (LP Versions)
- CS# and OE# Functions for Bus Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 128Kx8
- Industrial, Military and Commercial Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
  - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
  - 32 lead Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

The EDI88128C is a high speed, high performance, Monolithic CMOS Static RAM organized as 128Kx8.

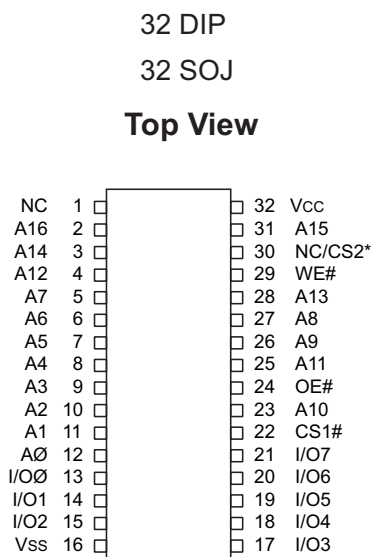
The device is also available as EDI88130C with an additional chip select line (CS2) which will automatically power down the device when proper logic levels are applied.

The second chip select line (CS2) can be used to provide system memory security during power down in non-battery backed up systems and simplify decoding schemes in memory banking where large multiple pages of memory are required.

The EDI88128C and the EDI88130C have eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

Low power versions, EDI88128LP and EDI88130LP, offer a 2V data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

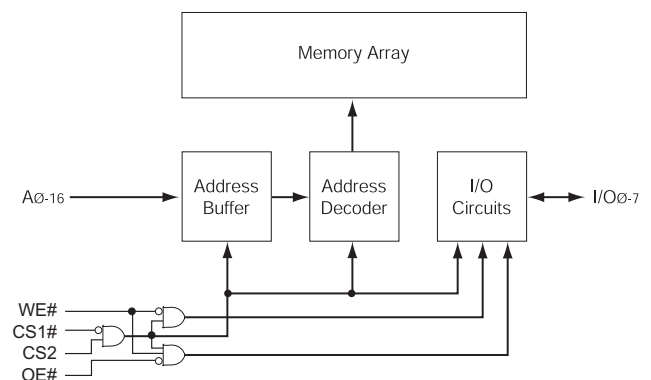
FIGURE 1 – PIN CONFIGURATION



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
WE#	Write Enable
CS1#, CS2	Chip Selects
OE#	Output Enable
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



\* Pin 30 is NC for 88128 or CS2 for 88130.



**ABSOLUTE MAXIMUM RATINGS**

Parameter		Unit
Voltage on any pin relative to V <sub>SS</sub>	-0.5 to 7.0	V
<b>Operating Temperature T<sub>A</sub> (Ambient)</b>		
	Commercial	0 to +70 °C
	Industrial	-40 to +85 °C
Military	-55 to +125 °C	
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T <sub>J</sub>	175	°C

**NOTE:**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE**

T<sub>A</sub> = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	C <sub>I</sub>	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz	12	pF
Input/Output Lines	C <sub>O</sub>	V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

**DC CHARACTERISTICS**

V<sub>CC</sub> = 5V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-5	—	+5	µA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = 0V to V <sub>CC</sub> , CS1# ≥ V <sub>IH</sub> and/or CS2# ≤ V <sub>IL</sub>	-10	—	+10	µA	
Operating Power Supply Current	I <sub>CC1</sub>	WE#, CS1# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA, Min Cycle (70-85ns)	—	—	120	mA	
		CS2# = V <sub>IH</sub> (100ns)	—	—	110	mA	
Standby (TTL) Power Supply Current	I <sub>CC2</sub>	CS1# ≥ V <sub>IH</sub> and/or CS2# ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub>	—	—	10	mA	
Full Standby Power Supply Current	I <sub>CC3</sub>	CS1# ≥ V <sub>CC</sub> - 0.2V and/or CS2# ≤ V <sub>CC</sub> + 0.2V	C	—	1	5	mA
		V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	LP	—	—	1	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	—	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	V	

NOTE: DC test conditions : V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

**TRUTH TABLE**

OE#	CS1#	CS2#	WE#	Mode	Output	Power
X	H	X	X	Standby	High Z	I <sub>CC2</sub> , I <sub>CC3</sub>
X	X	L	X	Standby	High Z	I <sub>CC2</sub> , I <sub>CC3</sub>
X	X	L	X	Output Deselect	High Z	I <sub>CC1</sub>
H	L	H	H	Output Deselect	High Z	I <sub>CC1</sub>
L	L	H	H	Read	Data Out	I <sub>CC1</sub>
X	L	H	L	Write	Data In	I <sub>CC1</sub>

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	+0.8	V



**AC Characteristics – Read Cycle**

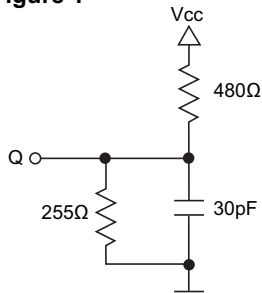
V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	70		85		100		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>AA</sub>		70		85		100	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>ACS</sub>		70		85		100	ns
	t <sub>SHQV</sub>	t <sub>ACS</sub>		70		85		100	ns
Chip Select to Output in Low Z (1)	t <sub>ELQX</sub>	t <sub>CLZ</sub>	3		3		3		ns
	t <sub>SHQX</sub>	t <sub>CLZ</sub>	3		3		3		ns
Chip Disable to Output in High Z (1)	t <sub>EHQZ</sub>	t <sub>CHZ</sub>		30		30		30	ns
	t <sub>SLQZ</sub>	t <sub>CHZ</sub>		30		30		30	ns
Output Hold from Address Change	t <sub>AVQX</sub>	t <sub>OH</sub>	3		3		3		ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		25		30		50	ns
Output Enable to Output in Low Z (1)	t <sub>GLQX</sub>	t <sub>OLZ</sub>	0		0		0		ns
Output Disable to Output in High Z (1)	t <sub>GHQZ</sub>	t <sub>OHZ</sub>	0	30	0	30	0	30	ns

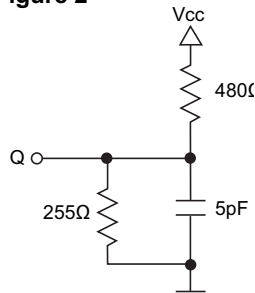
1. This parameter is guaranteed by design but not tested.

**AC Test Conditions**

**Figure 1**



**Figure 2**



Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t<sub>EHQZ</sub>, t<sub>GHQZ</sub> and t<sub>WLQZ</sub>, C<sub>L</sub> = 5pF Figure 2



**AC CHARACTERISTICS – WRITE CYCLE**

V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	70		85		100		ns
Chip Select to End of Write	t <sub>ELWH</sub>	t <sub>CW</sub>	60		75		85		ns
	t <sub>ELEH</sub>	t <sub>CW</sub>	60		75		85		ns
	t <sub>SHWH</sub>	t <sub>CW</sub>	60		75		85		ns
	t <sub>SHSL</sub>	t <sub>CW</sub>	60		75		85		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		ns
	t <sub>AVSH</sub>	t <sub>AS</sub>	0		0		0		ns
Address Valid to End of Write	t <sub>AVWH</sub>	t <sub>AW</sub>	60		75		85		ns
Write Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	35		70		80		ns
	t <sub>WLEH</sub>	t <sub>WP</sub>	35		70		80		ns
	t <sub>WLSL</sub>	t <sub>WP</sub>	35		70		80		ns
Write Recovery Time	t <sub>WHAX</sub>	t <sub>WR</sub>	5		5		5		ns
	t <sub>EHAX</sub>	t <sub>WR</sub>	5		5		5		ns
	t <sub>SLAX</sub>	t <sub>WR</sub>	5		5		5		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		ns
	t <sub>EHDX</sub>	t <sub>DH</sub>	0		0		0		ns
	t <sub>SLDX</sub>	t <sub>DH</sub>	0		0		0		ns
Write to Output in High Z (1)	t <sub>WLQZ</sub>	t <sub>WHZ</sub>	0	30	0	35	0	40	ns
Data to Write Time	t <sub>DVWH</sub>	t <sub>DW</sub>	35		40		40		ns
	t <sub>DVEH</sub>	t <sub>DW</sub>	35		40		40		ns
	t <sub>DVSL</sub>	t <sub>DW</sub>	35		40		40		ns
Output Active from End of Write (1)	t <sub>WHQX</sub>	t <sub>WLZ</sub>	5		5		5		ns

1. This parameter is guaranteed by design but not tested.



FIGURE 2 – TIMING WAVEFORM — READ CYCLE

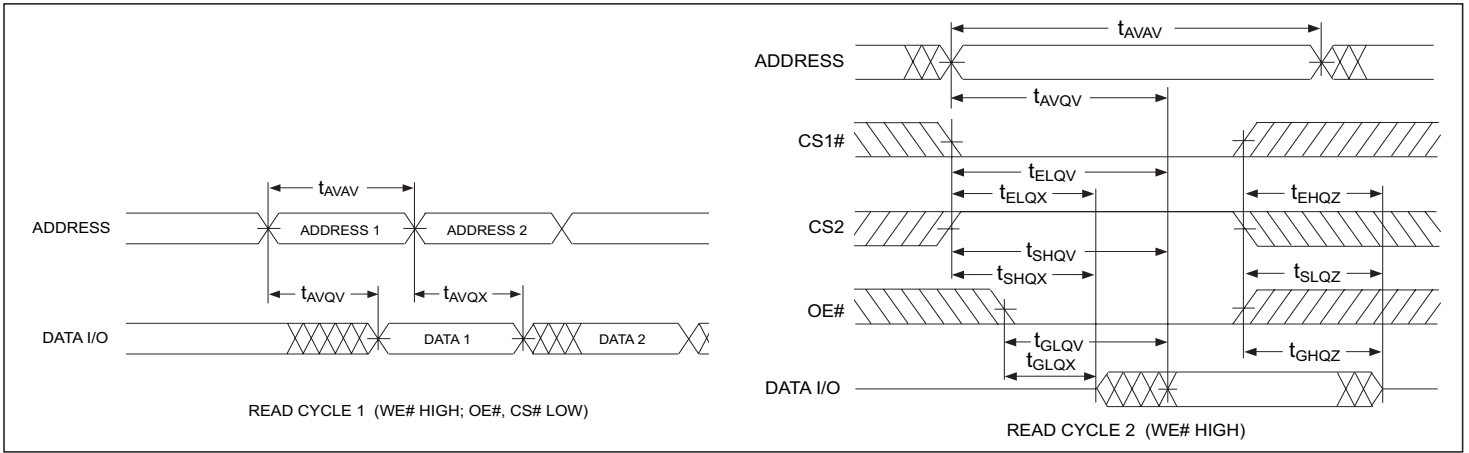


FIGURE 3 – WRITE CYCLE 1

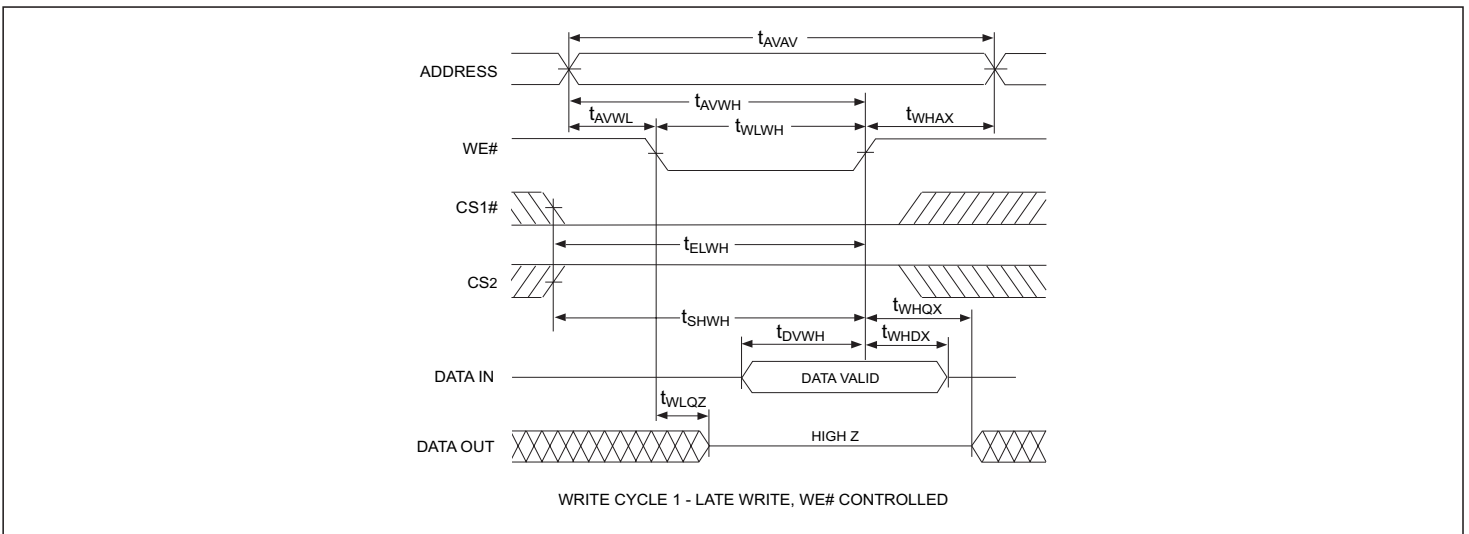
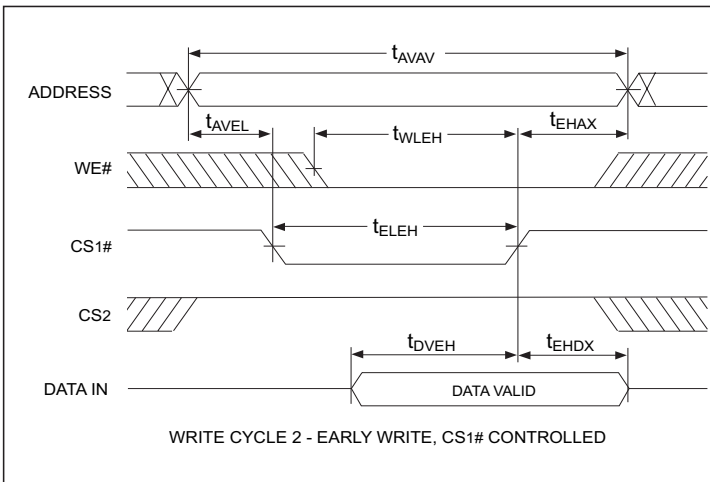
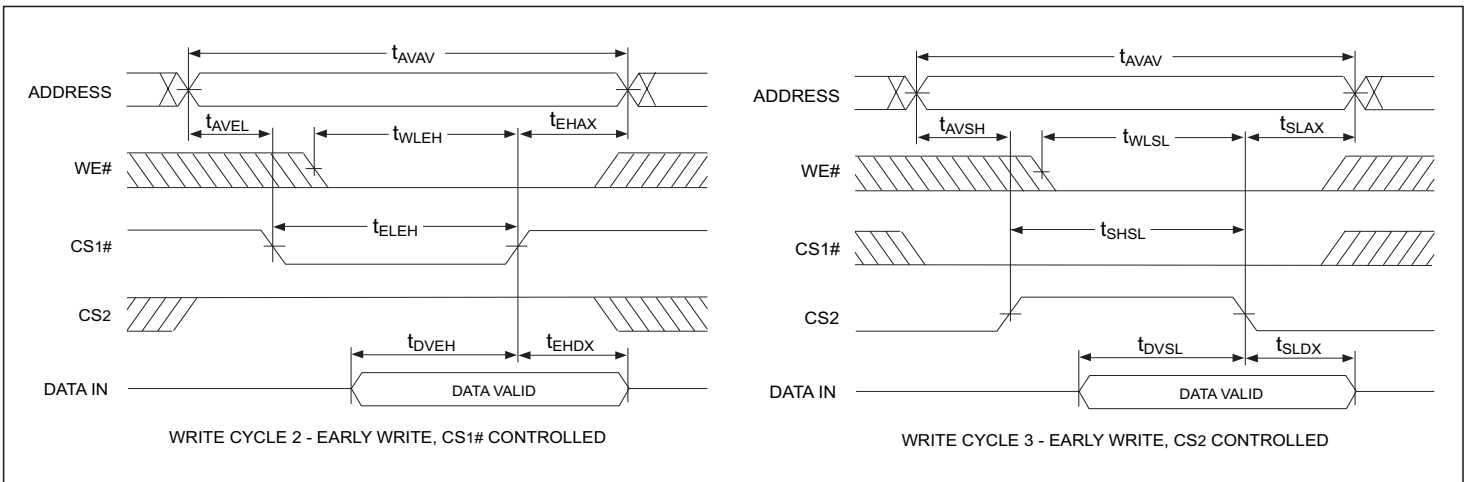


FIGURE 4 – WRITE CYCLE 2



WRITE CYCLE 3





**DATA RETENTION CHARACTERISTICS (EDI88128LP & EDI88130LP ONLY)**

$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

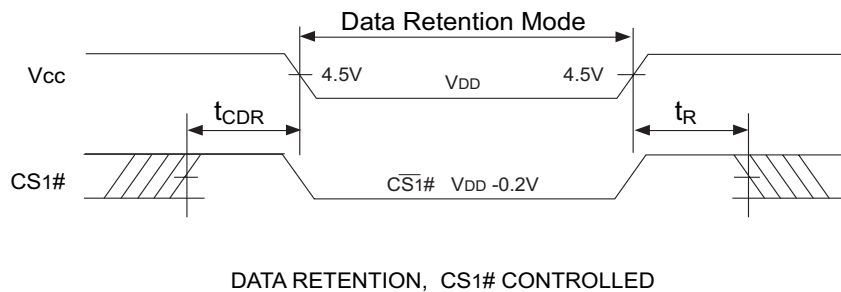
Characteristic Low Power Version only	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Voltage	$V_{DD}$	$V_{DD} = 2.0\text{V}$	2	-	-	V
Data Retention Quiescent Current	$I_{CCDR}$	$CS1\# \geq V_{DD} - 0.2\text{V}$	-	-	400	$\mu\text{A}$
Chip Disable to Data Retention Time (1)	$T_{CDR}$	$V_{IN} \geq V_{DD} - 0.2\text{V}$	0	-	-	ns
Operation Recovery Time (1)	$T_R$	or $V_{IN} \leq 0.2\text{V}$	$T_{AVAV}^*$	-	-	ns

NOTE:

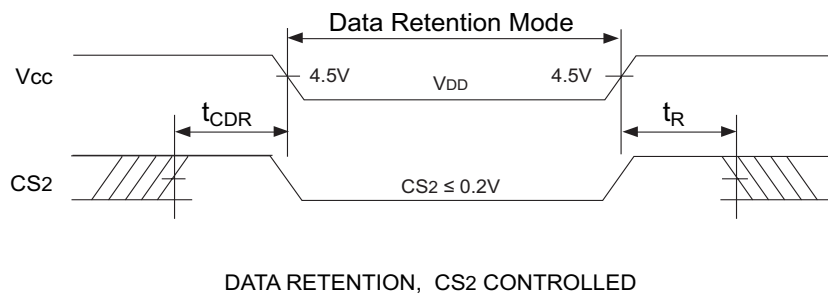
1. Parameter guaranteed by design, but not tested.

\* Read Cycle Time

**FIGURE 5 – DATA RETENTION – CS1# CONTROLLED**

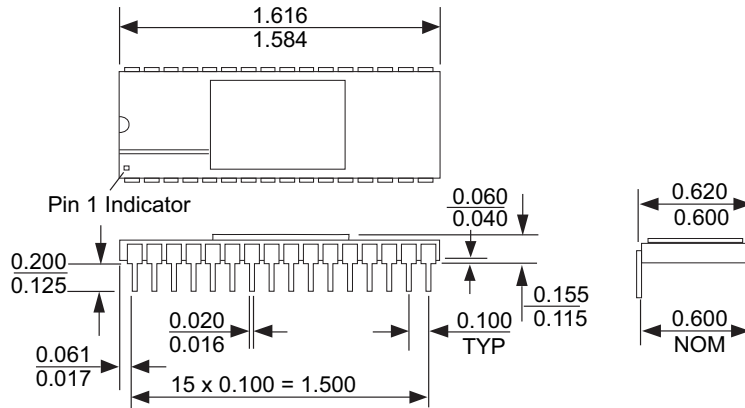


**FIGURE 6 – DATA RETENTION — CS2 CONTROLLED**



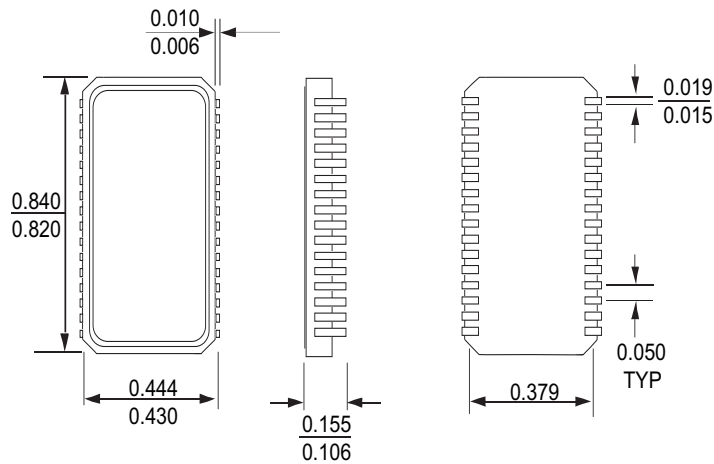


**PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600MILS WIDE)**



ALL DIMENSIONS ARE IN INCHES

**PACKAGE 140: 32 LEAD CERAMIC SOJ**



ALL DIMENSIONS ARE IN INCHES



## ORDERING INFORMATION

**EDI 8 8 128 C X X X**

**WHITE ELECTRONIC DESIGNS** \_\_\_\_\_

**SRAM** \_\_\_\_\_

**ORGANIZATION, 128Kx8** \_\_\_\_\_

8 130 = Dual Chip Select

**TECHNOLOGY:** \_\_\_\_\_

C = CMOS Standard Power

LP = Low Power

**ACCESS TIME (ns)** \_\_\_\_\_

**PACKAGE TYPE:** \_\_\_\_\_

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

N = 32 lead Ceramic SOJ (Package 140)

**DEVICE GRADE:** \_\_\_\_\_

B = MIL-STD-883 Compliant

M = Military Screened      -55°C to +125°C

I = Industrial                -40°C to +85°C

C = Commercial              0°C to +70°C