# 256Kx16 MONOLITHIC SRAM, SMD 5962-96795

## FEATURES

- 256Kx16 bit CMOS Static
- Random Access Memory
  - Access Times of 17, 20, 25, 35ns
  - Data Retention Function (LPA version)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- 44 lead JEDEC Approved Revolutionary Pinout
  - Ceramic SOJ (Package 322)
  - Ceramic Flatpack (Package 323)
- Single +5V (±10%) Supply Operation

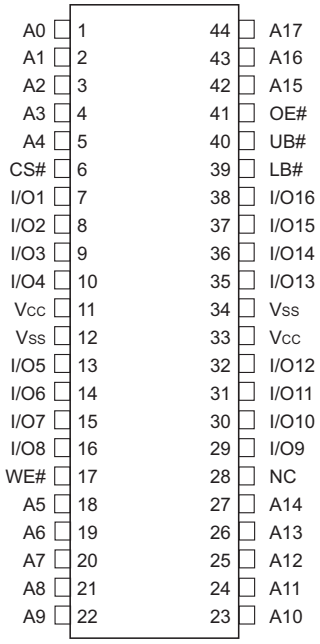
The EDI816256CA is a 4 megabit Monolithic CMOS Static RAM.

The EDI816256CA uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device allows upper and lower byte access by use of the data byte control pins (LB#, UB#).

The devices are available in a fully hermetic 44 lead ceramic SOJ and a 44 lead Ceramic Flatpack. The Ceramic SOJ is pin for pin compatible with the commercially available plastic SOJ. This allows the user the luxury of designing a board that can be used for both the commercial and military market.

A Low Power version with Data Retention (EDI816256LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

### PIN CONFIGURATION
### TOP VIEW




### PIN DESCRIPTION

| | |
|---|---|
| A0-17 | Address Inputs |
| LB# (I/O1-8) | Lower-Byte Control (I/O1-8) |
| UB# (I/O9-16) | Upper-Byte Control (I/O9-16) |
| I/O1-16 | Data Input/Output |
| CS# | Chip Select |
| OE# | Output Enable |
| WE# | Write Enable |
| Vcc | +5.0V Power |
| Vss | Ground |
| NC | No Connection |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Unit |
|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | -0.5 to 7.0 | V |
| Operating Temperature $T_A$ (Ambient) | | |
| Commercial | 0 to +70 | °C |
| Industrial | -40 to +85 | °C |
| Military | -55 to +125 | °C |
| Storage Temperature, Plastic | -65 to +125 | °C |
| Power Dissipation | 1.5 | W |
| Output Current | 20 | mA |
| Junction Temperature, $T_J$ | 175 | °C |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TRUTH TABLE

| CS# | WE# | OE# | LB# | UB# | Mode | Data I/O | | Supply Current |
|---|---|---|---|---|---|---|---|---|
| | | | | | | $I/O_{1-8}$ | $I/O_{9-16}$ | |
| H | X | X | X | X | Not Select | High Z | High Z | $I_{CC2}$, $I_{CC3}$ |
| L | H | H | X | X | Output Disable | | | |
| L | X | X | H | H | | | | |
| L | H | L | L | H | Read | Data Out | High Z | $I_{CC1}$ |
| | | | H | L | | High Z | Data Out | |
| | | | L | L | | Data Out | Data Out | |
| L | L | X | L | H | Write | Data In | High Z | $I_{CC1}$ |
| | | | H | L | | High Z | Data In | |
| | | | L | L | | Data In | Data In | |

## CAPACITANCE

$T_A$ = +25°C

| Parameter | Symbol | Condition | Max | Unit |
|---|---|---|---|---|
| Address Lines | CI | VIN = Vcc or Vss, f = 1.0MHz | 12 | pF |
| Data Lines | CD/Q | VIN = Vcc or Vss, f = 1.0MHz | 14 | pF |

These parameters are sampled, not 100% tested.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Sym | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | — | Vcc +0.5 | V |
| Input Low Voltage | VIL | -0.3 | — | 0.8 | V |

## DC CHARACTERISTICS

$V_{CC}$ = 5V, $V_{SS}$ = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol | Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = 0V to $V_{CC}$ | | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{I/O}$ = 0V to $V_{CC}$ | | | 10 | µA |
| Operating Power Supply Current | $I_{CC1}$ | WE#, CS# = $V_{IL}$, $I_{I/O}$ = OmA, Min Cycle | | | 300 | mA |
| Standby (TTL) Power Supply Current | $I_{CC2}$ | CS# ≥ $V_{IH}$, $V_{IN}$ ≤ $V_{IL}$, $V_{IN}$ ≥ $V_{IH}$ | | | 60 | mA |
| Full Standby Power Supply Current | $I_{CC3}$ | CS# ≥ $V_{CC}$ -0.2V | CA | — | 25 | mA |
| | | $V_{IN}$ ≥ $V_{CC}$ -0.2V or $V_{IN}$ ≤ 0.2V | LPA | — | 16 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 6.0mA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA | | 2.4 | | V |

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc -0.3V

## AC TEST CONDITIONS

**Figure 1**

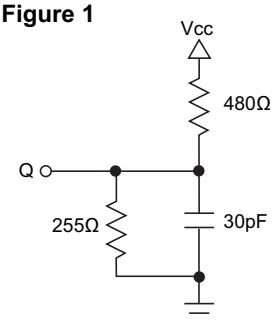
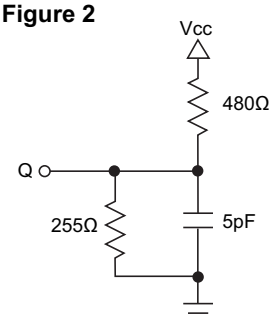



**Figure 2**




| | |
|---|---|
| Input Pulse Levels | Vss to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | Figure 1 |

NOTE: For $t_{EHQZ}$, $t_{GHQZ}$ and $t_{WLQZ}$, CL = 5pF (Figure 2)

## AC CHARACTERISTICS – READ CYCLE

$V_{CC}$ = 5V, $V_{SS}$ = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol JEDEC | Symbol Alt. | 17ns Min | 17ns Max | 20ns Min | 20ns Max | 25ns Min | 25ns Max | 35ns Min | 35ns Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{AVAV}$ | $t_{RC}$ | 17 | | 20 | | 25 | | 35 | | ns |
| Address Access Time | $t_{AVQV}$ | $t_{AA}$ | | 17 | | 20 | | 25 | | 35 | ns |
| Chip Enable Access Time | $t_{ELQV}$ | $t_{ACS}$ | | 17 | | 20 | | 25 | | 35 | ns |
| Chip Enable to Output in Low Z (1) | $t_{ELQX}$ | $t_{CLZ}$ | 2 | | 5 | | 5 | | 5 | | ns |
| Chip Disable to Output in High Z (1) | $t_{EHQZ}$ | $t_{CHZ}$ | 0 | 7 | 0 | 7 | 0 | 8 | 0 | 10 | ns |
| Output Hold from Address Change | $t_{AVQX}$ | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Enable to Output Valid | $t_{GLQV}$ | $t_{OE}$ | | 10 | | 10 | | 12 | | 15 | ns |
| Output Enable to Output in Low Z (1) | $t_{GLQX}$ | $t_{OLZ}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Disable to Output in High Z(1) | $t_{GHQZ}$ | $t_{OHZ}$ | 0 | 7 | 0 | 7 | 0 | 8 | 0 | 10 | ns |
| LB#, UB# Access Time | $t_{UBLQV}$<br>$t_{LBLQV}$ | $t_{BA}$ | | 10 | | 10 | | 12 | | 15 | ns |
| LB#, UB# Enable to Low Z Output | $t_{UBLQX}$<br>$t_{LBLQX}$ | $t_{BLZ}$ | 0 | 0 | | 0 | | 0 | | 0 | ns |
| LB#, UB# Disable to High Z Output | $t_{UBHQZ}$<br>$t_{LBHQZ}$ | $t_{BHZ}$ | 0 | 7 | 0 | 7 | 0 | 8 | 0 | 10 | ns |

**NOTE:**

1. This parameter is guaranteed by design but not tested.

## AC CHARACTERISTICS – WRITE CYCLE

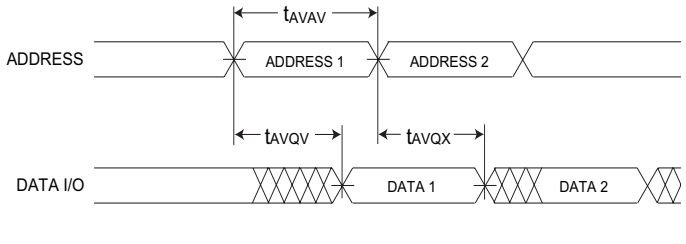
$V_{CC}$ = 5V, $V_{SS}$ = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol JEDEC | Symbol Alt. | 17ns Min | 17ns Max | 20ns Min | 20ns Max | 25ns Min | 25ns Max | 35ns Min | 35ns Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | tAVAV | tWC | 17 | | 20 | | 25 | | 35 | | ns |
| Chip Enable to End of Write | tELWH<br>tELEH | tCW<br>tCW | 14<br>14 | | 15<br>15 | | 17<br>17 | | 20<br>20 | | ns<br>ns |
| Address Setup Time | tAVWL<br>tAVEL<br>tAVUBL | tAS<br>tAS<br>tAS | 0<br>0<br>0 | | 0<br>0<br>0 | | 0<br>0<br>0 | | 0<br>0<br>0 | | ns<br>ns<br>ns |
| Address Valid to End of Write | tAVWH<br>tAVEH<br>tAVUBH | tAW<br>tAW<br>tAW | 14<br>14<br>14 | | 15<br>15<br>15 | | 17<br>17<br>17 | | 20<br>20<br>20 | | ns<br>ns<br>ns |
| Write Pulse Width | tWLWH<br>tWLEH | tWP<br>tWP | 14<br>14 | | 14<br>14 | | 15<br>15 | | 17<br>17 | | ns<br>ns |
| Write Recovery Time | tWHAX<br>tEHAX | tWR<br>tWR | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | | ns<br>ns |
| Data Hold Time | tWHDX<br>tEHDX | tDH<br>tDH | 0<br>0 | | 0<br>0 | | 0<br>0 | | 0<br>0 | | ns<br>ns |
| Write to Output in High Z (1) | tWLQZ | tWHZ | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 10 | ns |
| Data to Write Time | tDVWH<br>tDVEH | tDW<br>tDW | 10<br>10 | | 10<br>10 | | 12<br>12 | | 15<br>15 | | ns<br>ns |
| Output Active from End of Write (1) | tWHQX | tWLZ | 0 | | 0 | | 0 | | 0 | | ns |
| LB, UB Valid to End of Write | tLBLLBH<br>tUBLUBH | tBW | 14 | | 16 | | 18 | | 20 | | ns |

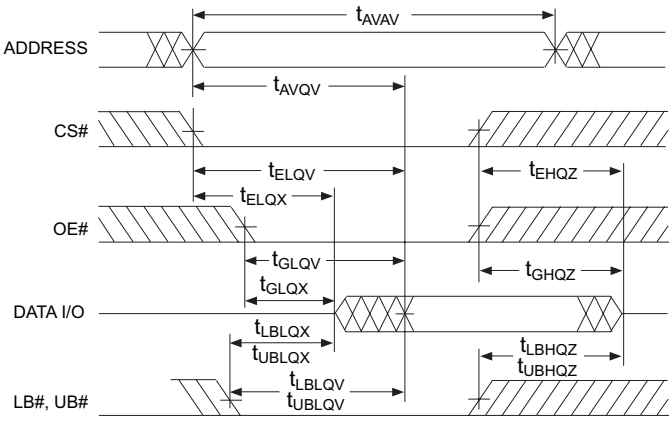
NOTE:

1. This parameter is guaranteed by design but not tested.

## TIMING WAVEFORM – READ CYCLE

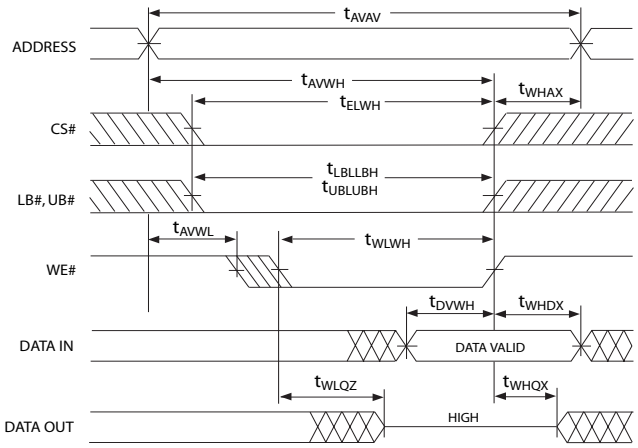



READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



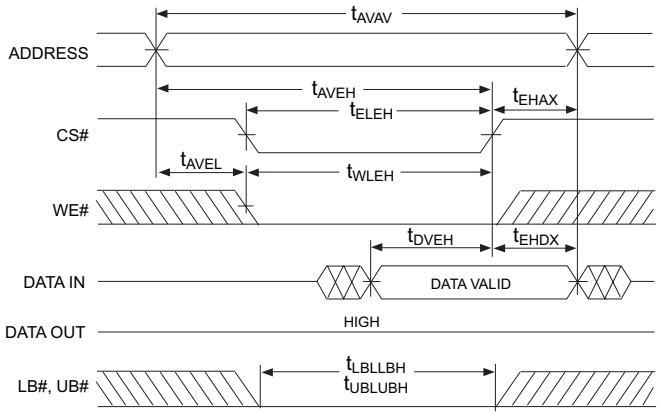

READ CYCLE 2 (WE# HIGH)

## WRITE CYCLE – WE# CONTROLLED



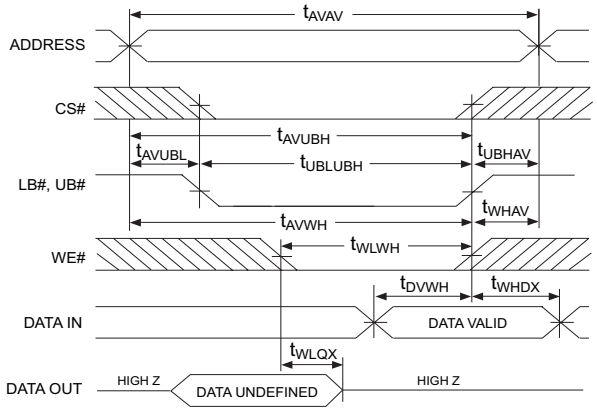

WRITE CYCLE 1, WE# CONTROLLED

## WRITE CYCLE - CS# CONTROLLED




WRITE CYCLE 2, CS# CONTROLLED

## WRITE CYCLE - LB#, UB# CONTROLLED




WRITE CYCLE 3, LB#, UB# CONTROLLED

## DATA RETENTION CHARACTERISTICS (EDI816256LPA ONLY)

-55°C ≤ $T_A$ ≤ +125°C

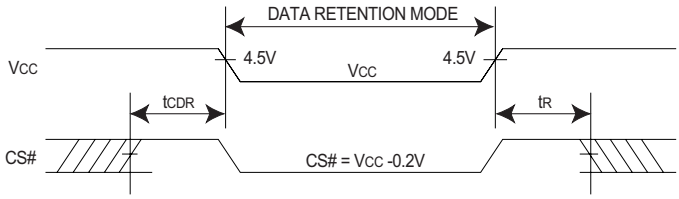
| Characteristic Low Power Version only | Sym | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Data Retention Voltage | $V_{CC}$ | $V_{CC}$ = 2.0V | 2 | – | – | V |
| Data Retention Quiescent Current | $I_{CCDR}$ | CS# ≥ $V_{CC}$ -0.2V | – | – | 2.2 | mA |
| Chip Disable to Data Retention Time (1) | $T_{CDR}$ | $V_{IN}$ ≥ $V_{CC}$ -0.2V | 0 | – | – | ns |
| Operation Recovery Time (1) | $T_R$ | or $V_{IN}$ ≤ 0.2V | $T_{AVAV}$ | – | – | ns |

**NOTE:**

1. This parameter is guaranteed by design but not tested.

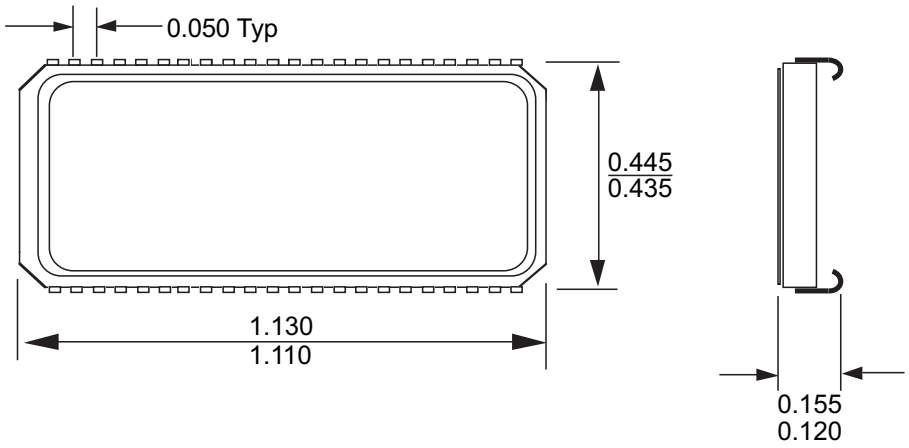
* Read Cycle Time

## DATA RETENTION – CS# CONTROLLED



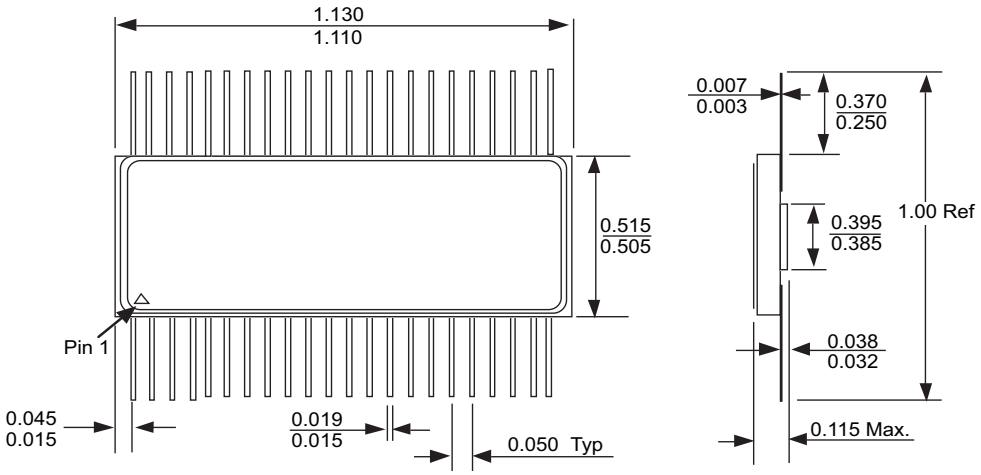

DATA RETENTION, CS# CONTROLLED

## PACKAGE 322: 44 LEAD, CERAMIC SOJ




DIMENSIONS ARE IN INCHES

## PACKAGE 323: 44 PIN, CERAMIC FLATPACK




DIMENSIONS ARE IN INCHES

## ORDERING INFORMATION

**EDI 8 16256 CA X X X**

**WHITE ELECTRONIC DESIGNS**

**SRAM**

**ORGANIZATION, 256Kx16**

**TECHNOLOGY:**

CA = CMOS Standard Power

LPA = Low Power

**ACCESS TIME (ns)**

**PACKAGE TYPE:**

F44 = 44 pin Ceramic Flatpack (Package 323)

N44 = 44 lead Ceramic SOJ (Package 322)

**DEVICE GRADE:**

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C