HYS64D64300[G/H]U–[5/6]–B
HYS72D64300[G/H]U–[5/6]–B
HYS64D128320[G/H]U–[5/6]–B
HYS72D128320[G/H]U–[5/6]–B

184-Pin Unbuffered Dual-In-Line Memory Modules
UDIMM
DDR SDRAM

Memory Products

Infineon technologies

Never stop thinking.

Edition 2004-05

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HYS64D64300[G/H]U–[5/6]–B
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Revision History:	**Rev. 1.0**	**2004-05**
Previous Version:	Rev. 0.5	
Page	Subjects (major changes since last revision)	
7	Added Non-Green Modules DDR400 & DDR333 and removed DDR266	
8,12ff	editorial changes	
22,23	Updated I_{DD} currents to final	
24,27,30,33	Update SPD Codes	

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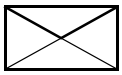

Table of Contents

1 Overview

1.1 Features

- 184-Pin Unbuffered Dual-In-Line Memory Modules (ECC and non-parity) for PC and Workstation main memory applications
- One rank 64M x 64, 64M ×72 and two ranks 128M × 64, 128M ×72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single +2.5V (±0.2V) power supply
- Built with 512 Mbit DDR SDRAM in P-TSOPII-66-1 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts
- DDR400 speed grade supported
- Lead-free

Table 1 Performance

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333B	—
	Module		PC3200–3033	PC2700–2533	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	166	MHz
	@CL2	f_{CK2}	133	133	MHz

1.2 Description

The HYS64D64300[G/H]U–[5/6]–B, HYS72D64300[G/H]U–[5/6]–B, HYS64D128320[G/H]U–[5/6]–B, and HYS72D128320[G/H]U–[5/6]–B are industry standard 184-Pin Unbuffered Dual-In-Line Memory Modules (UDIMM) organized as 64M ×64, 128M ×64 for non-parity and 64M ×72,128M ×72 for ECC main memory applications. The memory array is designed with 512Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer

Table 2 Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL=3.0)			
HYS64D64300GU–5–B	PC3200U–30330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300GU–5–B	PC3200U–30330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320GU–5–B	PC3200U–30330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320GU–5–B	PC3200U–30330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D64300GU–6–B	PC2700U–25330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300GU–6–B	PC2700U–25330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320GU–6–B	PC2700U–25330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320GU–6–B	PC2700U–25330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC3200 (CL=3.0)			
HYS64D64300HU–5–B	PC3200U–30330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU–5–B	PC3200U–30330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU–5–B	PC3200U–30330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU–5–B	PC3200U–30330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D64300HU–6–B	PC2700U–25330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU–6–B	PC2700U–25330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU–6–B	PC2700U–25330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU–6–B	PC2700U–25330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)

Note: All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D64300HU-6-B, indicating rev. B dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example “PC2700”), the latencies and SPD code definition (for example “20330” means CAS latency of 2.0 clocks, RCD[1] latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.

1) RCD: Row-Column-Delay

2 Pin Configuration

The pin configuration of the Unbuffered DDR SDRAM DIMM is listed by function in **Table 3** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 4** and **Table 5** respectively. The pin numbering is depicted in **Figure 1**.

Table 3 Pin Configuration of UDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
137	CK0	I	SSTL	**Clock Signals 2:0**
	NC	NC	–	*Note: For clock net loading see block diagram, CK0 is NC on 1R ×16*
16	CK1	I	SSTL	
76	CK2	I	SSTL	
138	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 2:0**
	NC	NC	–	
17	$\overline{CK1}$	I	SSTL	*Note: For clock net loading see block diagram, CK0 is NC on 1R ×16*
75	$\overline{CK2}$	I	SSTL	
21	CKE0	I	SSTL	**Clock Enable Rank 0**
111	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
Control Signals				
157	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
158	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
154	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
65	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
63	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
59	BA0	I	SSTL	**Bank Address Bus 2:0**
52	BA1	I	SSTL	
48	A0	I	SSTL	**Address Bus 11:0**
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	
32	A5	I	SSTL	
125	A6	I	SSTL	
29	A7	I	SSTL	

Table 3 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
122	A8	I	SSTL	**Address Bus 11:0**
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	
118	A11	I	SSTL	
115	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
	NC	NC	–	*Note: 128 Mbit based module*
167	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	–	*Note: Module based on 512 Mbit or smaller dies*
Data Signals				
2	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	
106	DQ13	I/O	SSTL	
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
114	DQ20	I/O	SSTL	
117	DQ21	I/O	SSTL	

Table 3 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
121	DQ22	I/O	SSTL	**Data Bus 63:0**
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	
150	DQ38	I/O	SSTL	
151	DQ39	I/O	SSTL	
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	
166	DQ53	I/O	SSTL	
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	
174	DQ60	I/O	SSTL	
175	DQ61	I/O	SSTL	
178	DQ62	I/O	SSTL	
179	DQ63	I/O	SSTL	
44	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
45	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
49	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
51	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
134	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
135	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
142	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
144	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
5	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
14	DQS1	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	
78	DQS6	I/O	SSTL	
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	**Data Strobe 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*

Table 3 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
97	DM0	I	SSTL	**Data Mask Bus 7:0**
107	DM1	I	SSTL	
119	DM2	I	SSTL	
129	DM3	I	SSTL	
149	DM4	I	SSTL	
159	DM5	I	SSTL	
169	DM6	I	SSTL	
177	DM7	I	SSTL	
140	DM8	I	SSTL	**Data Mask 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
EEPROM				
92	SCL	I	CMOS	**Serial Bus Clock**
91	SDA	I/O	OD	**Serial Bus Data**
181	SA0	I	CMOS	**Slave Address Select Bus 2:0**
182	SA1	I	CMOS	
183	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
184	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	PWR	–	**Power Supply**

Table 3 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	GND	–	**Ground Plane**
Other Pins				
82	V_{DDID}	O	OD	**V_{DD} Identification** *Note: Pin in tristate, indicating V_{DD} and V_{DDQ} nets connected on PCB*
9, 10, 71, 90, 101, 102, 103, 113, 163, 173	NC	NC	–	**Not connected** Pins not connected on Infineon UDIMMs

Table 4 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 5 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

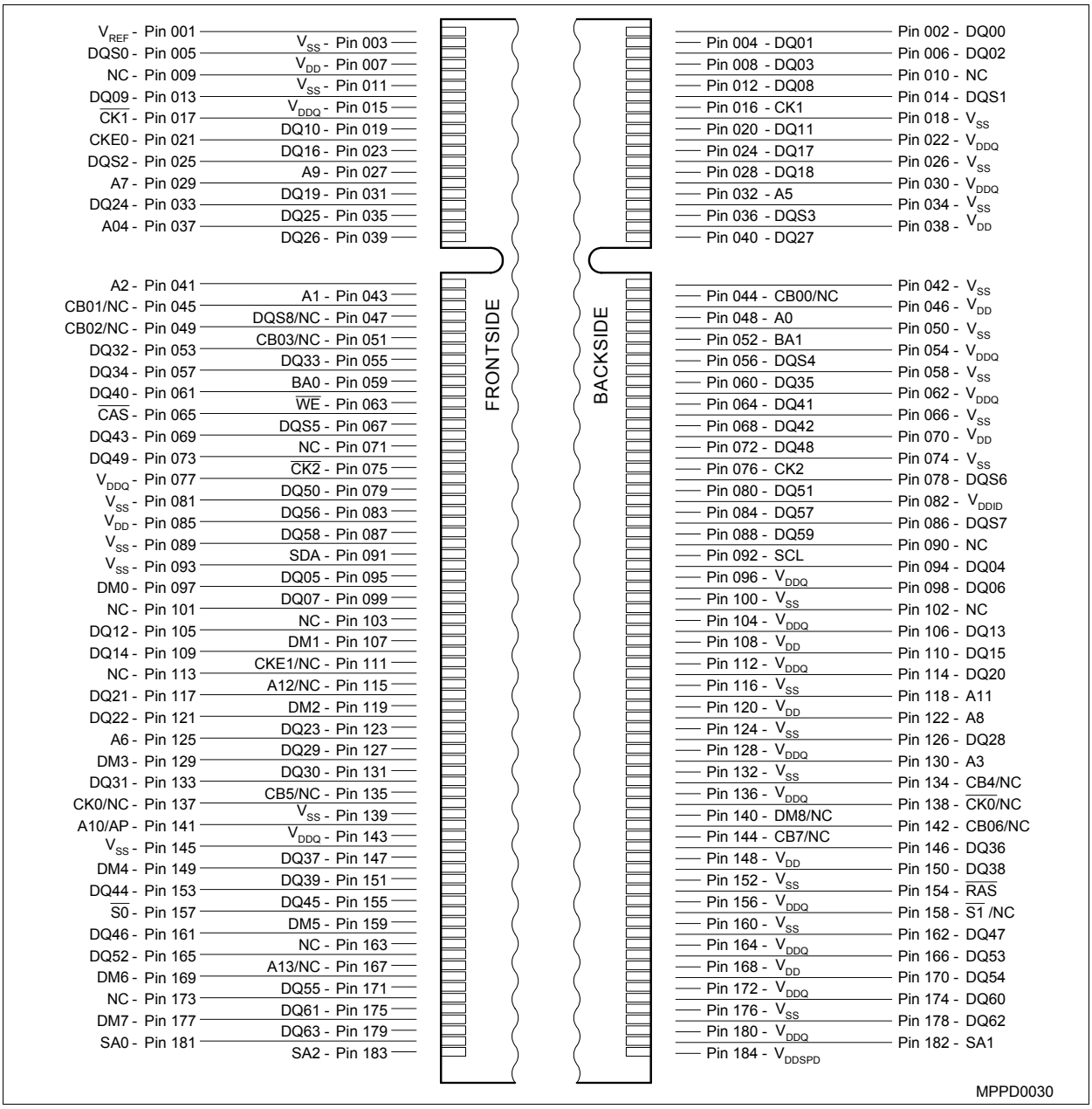

Figure 1 Pin Configuration 184-Pin, UDIMM

Table 6 Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
512 MB	64M ×64	1	64M ×8	8	13/2/11	8K	64 ms	7.8 µs
512 MB	64M ×72	1	64M ×8	8	13/2/11	8K	64 ms	7.8 µs
1 GB	128M ×64	2	64M ×8	16	13/2/12	8K	64 ms	7.8 µs
1 GB	128M ×72	2	64M ×8	18	13/2/12	8K	64 ms	7.8 µs

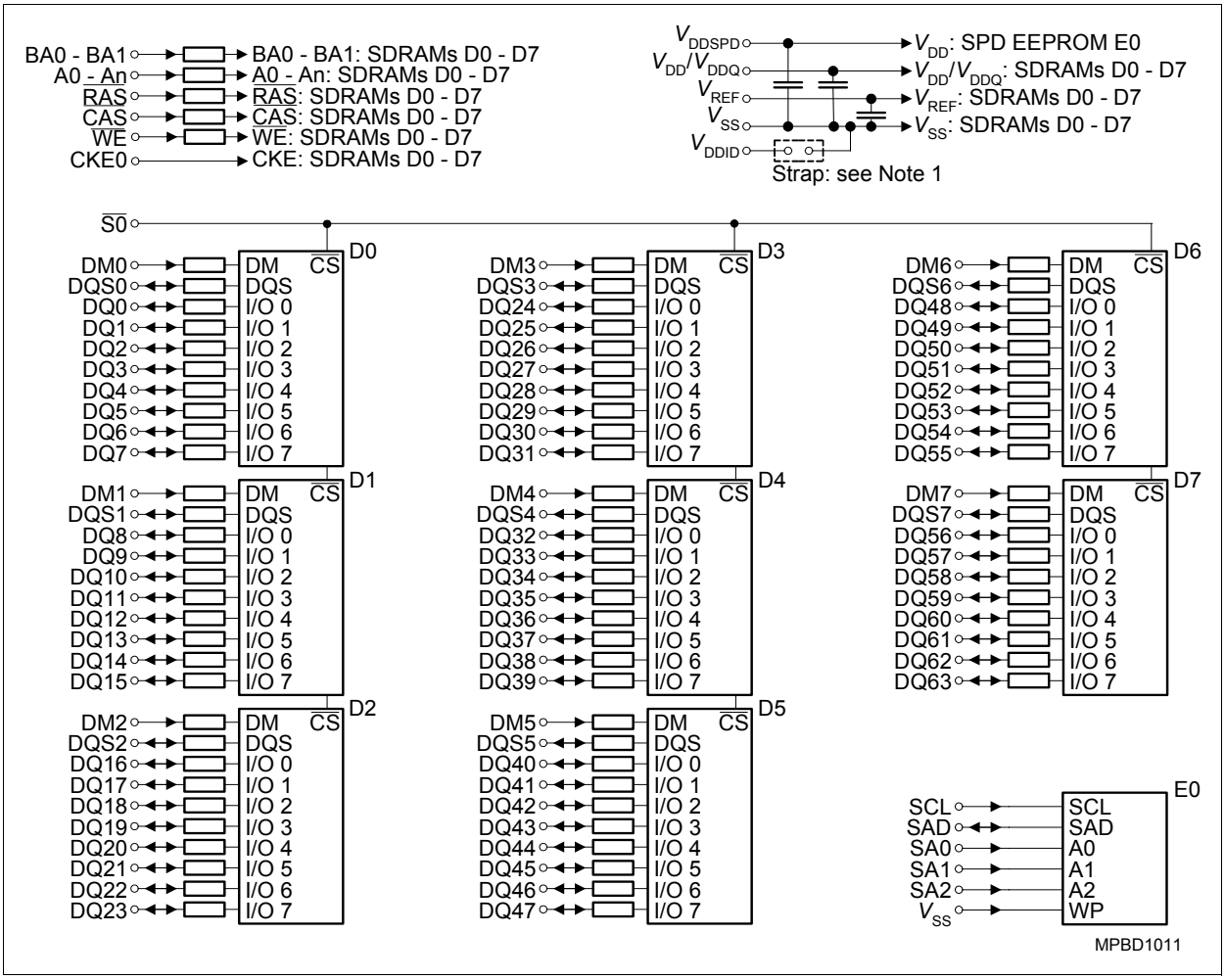

Figure 2 Block Diagram UDIMM Raw Card A ×64, 1 Rank, ×8

Note:

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 Ω ±5 %*
3. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ±5 %*

Table 7 Clock Signal Loads

Clock Input	Number of SDRAMs	Note
CK0, $\overline{CK0}$	2 SDRAMs	—
CK1, $\overline{CK1}$	3 SDRAMs	—
CK2, $\overline{CK2}$	3 SDRAMs	—

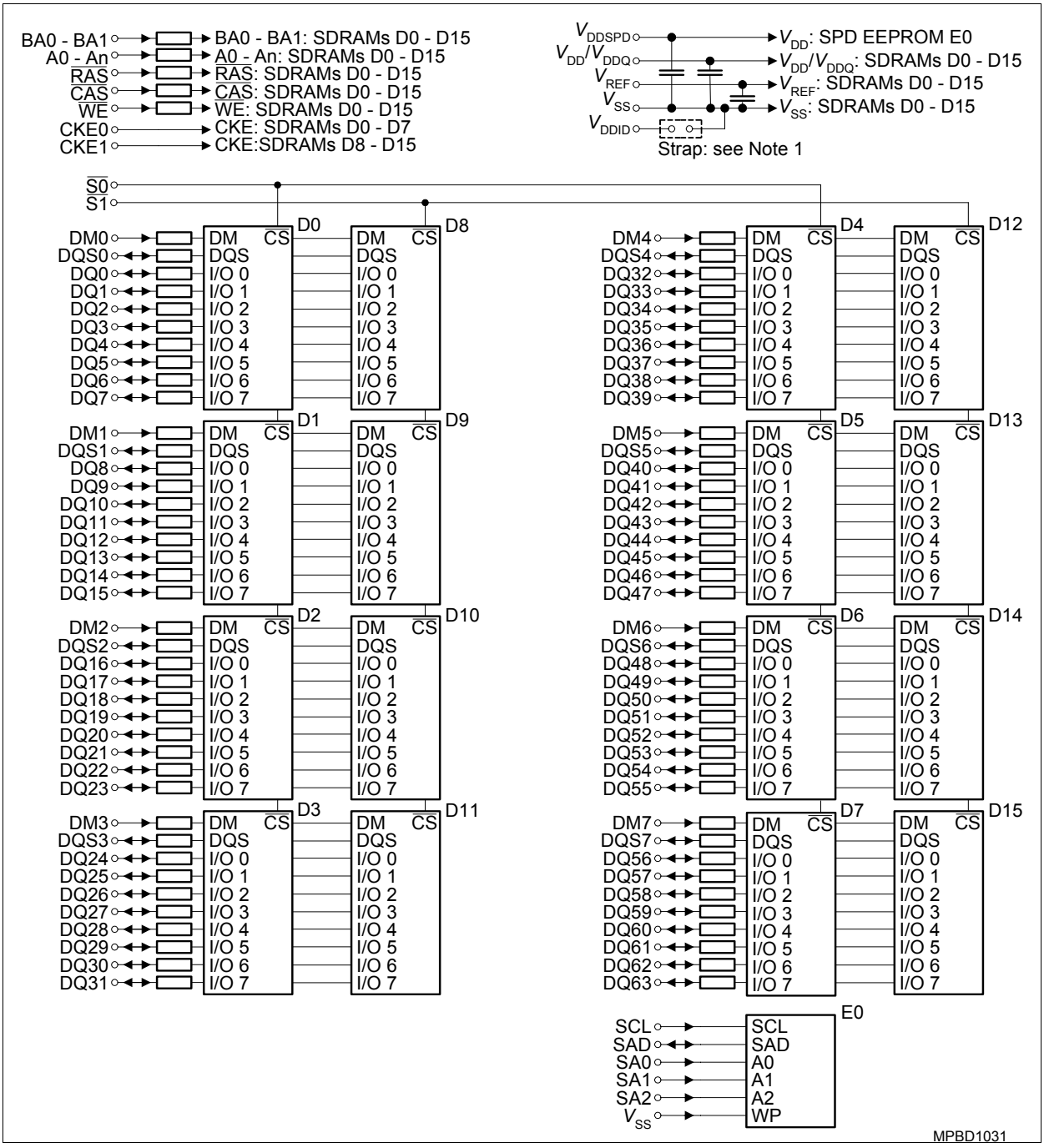

Figure 3 Block Diagram UDIMM Raw Card B (x64, 2 Ranks, x8)

Note:

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 Ω ±5 %*
3. *BAn, An, RAS, CAS, WE resistors are 3 Ω ±5 %*

Table 8 Clock Signal Loads

Clock Input	Number of SDRAMs	Note
CK0, CK0	4 SDRAMs	—
CK1, CK1	6 SDRAMs	—
CK2, CK2	6 SDRAMs	—

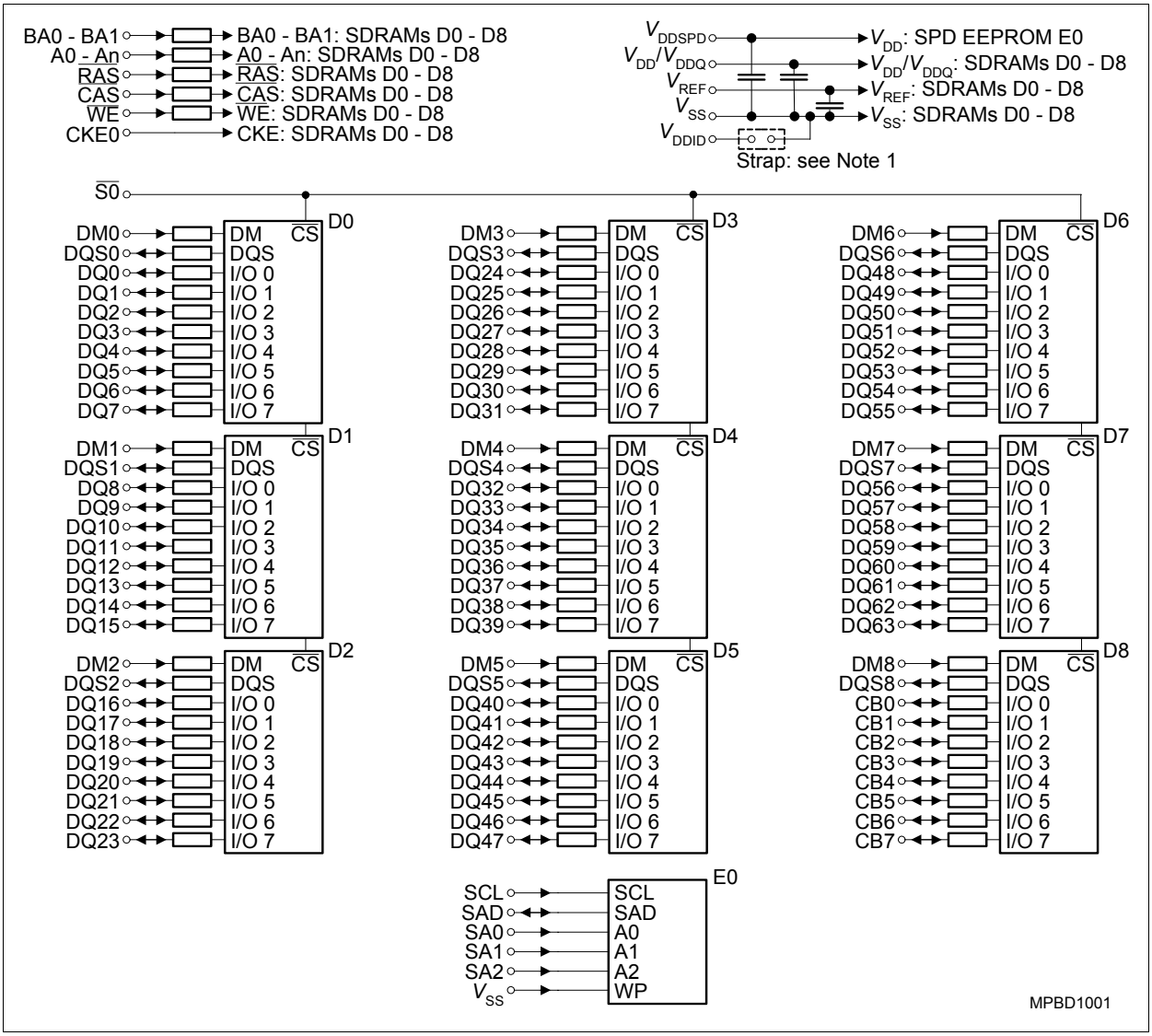

Figure 4 Block Diagram UDIMM Raw Card A ×72, 1Rank, ×8, ECC

Note:

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 Ω ±5 %*
3. *BAn, An, RAS, CAS, WE resistors are 5.1 Ω ±5 %*

Table 9 Clock Signal Loads

Clock Input	Number of SDRAMs	Note
CK0, CK0	3 SDRAMs	—
CK1, CK1	3 SDRAMs	—
CK2, CK2	3 SDRAMs	—

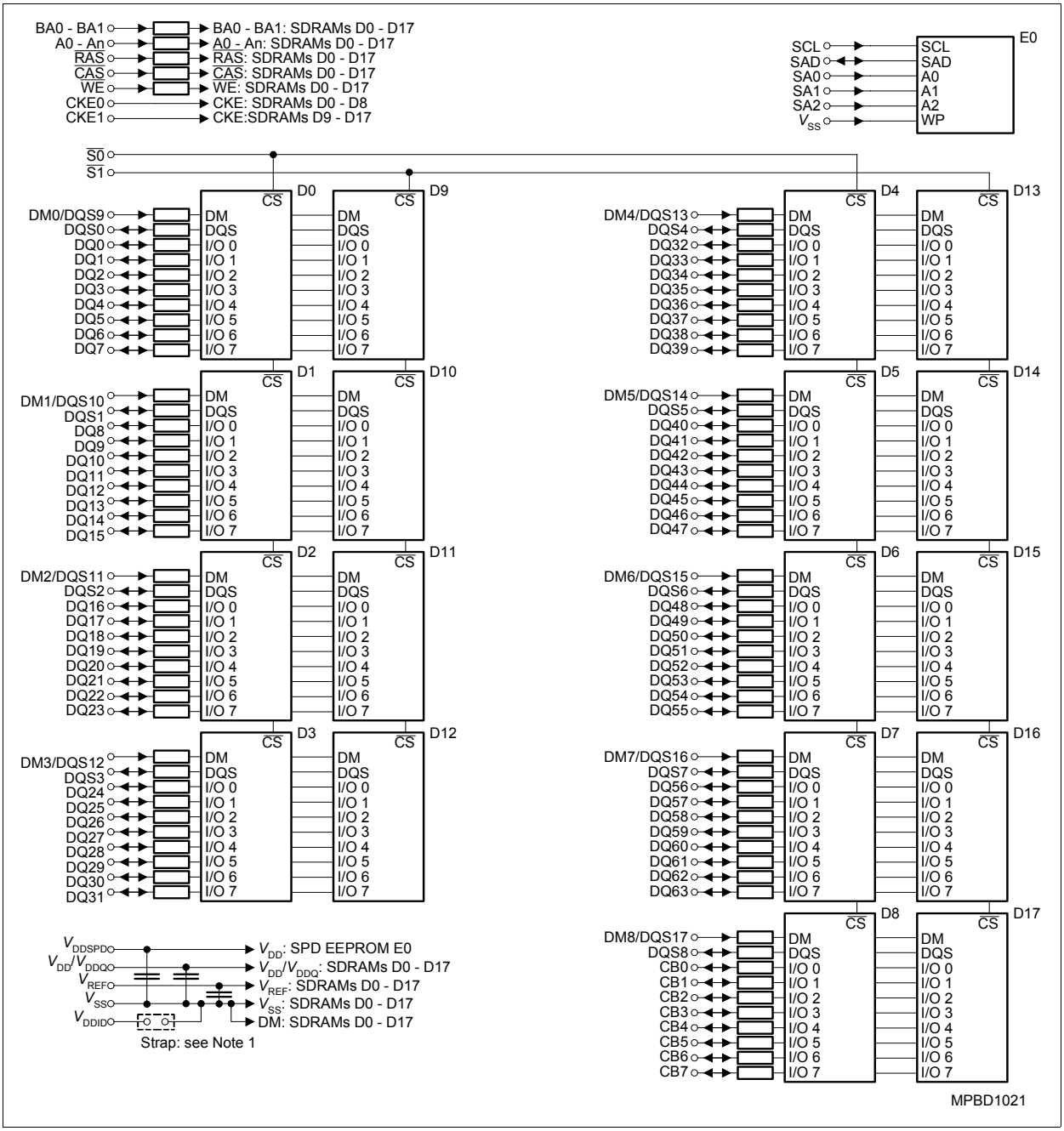

Figure 5 Block Diagram UDIMM Raw Card B ×72, 2Ranks, ×8, ECC

Note:

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 Ω ±5 %*
3. *BAn, An, RAS, CAS, WE resistors are 3 Ω ±5 %*

Table 10 Clock Signal Loads

Clock Input	Number of SDRAMs	Note
CK0, CK0	6 SDRAMs	—
CK1, CK1	6 SDRAMs	—
CK2, CK2	6 SDRAMs	—

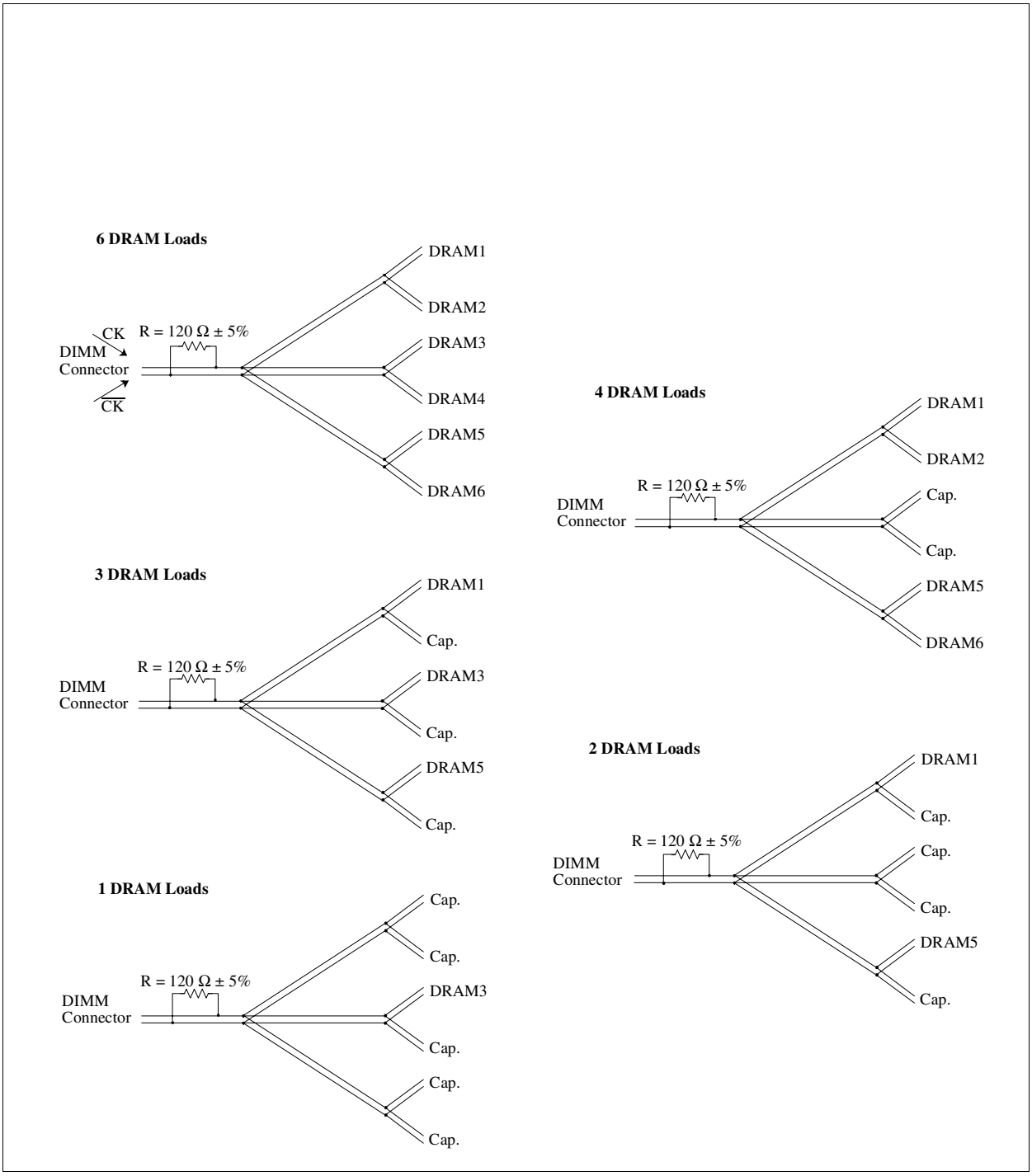

Figure 6 Clock Net Wiring

3 Electrical Characteristics

3.1 Operating Conditions

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 12 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]

Table 12 Electrical Characteristics and DC Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Input Leakage Current	I_I	–2		2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$ [8)]
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V [8)]
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V [8)]

1) 0 °C $\leq T_A \leq$ 70 °C
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Inputs are not recognized as valid until V_{REF} stabilizes.
9) Values are shown per DDR SDRAM component

Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	5	8	—	—	ns	CL = 3.0 2)3)4)5)
		6	12	7.5	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)

Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	70	—	72	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	$t_{RCD} - t_{RASmin}$				ns	2)3)4)5)

Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}					t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

3.2 Current Conditions and Specification

I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 14 I_{DD} Specification for HYS[64/72]D[64/128][300/320]HU–5–B

Product Type	HYS64D64300HU–5–B HYS64D64300GU–5–B		HYS72D64300HU–5–B HYS72D64300GU–5–B		HYS64D128320HU–5–B HYS64D128320GU–5–B		HYS72D128320HU–5–B HYS72D128320GU–5–B		Unit	Note [1)2)]
Organization	**512MB**		**512MB**		**1GB**		**1GB**			
	×64		**×64**		**×64**		**×72**			
	1 Rank		**1 Rank**		**2 Ranks**		**2 Ranks**			
	–5		**–5**		**–5**		**–5**			
Symbol	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{DD0}	800	920	900	1040	1110	1300	1250	1460	mA	3)
I_{DD1}	880	1040	990	1170	1190	1420	1340	1590	mA	3)4)
I_{DD2P}	20	40	30	40	50	70	50	80	mA	5)
I_{DD2F}	240	290	270	320	480	580	540	650	mA	3)
I_{DD2Q}	150	210	170	230	300	420	340	470	mA	5)
I_{DD3P}	100	130	110	140	190	260	220	290	mA	5)
I_{DD3N}	310	380	350	420	620	750	700	850	mA	5)
I_{DD4R}	800	960	900	1080	1110	1340	1250	1500	mA	3)4)
I_{DD4W}	840	1000	950	1130	1150	1380	1300	1550	mA	3)
I_{DD5}	1920	2320	2160	2610	2230	2700	2510	3030	mA	3)
I_{DD6}	23	46	26	51	46	91	52	103	mA	5)
I_{DD7}	2480	2920	2790	3290	2790	3300	3140	3710	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

Table 15 I_{DD} Specification for HYS[64/72]D[64/128][300/320]HU–6–B

Product Type	HYS64D64300HU–6–B HYS64D64300GU–6–B		HYS72D64300HU—6–B HYS72D64300GU–6–B		HYS64D128320HU–6–B HYS64D128320GU–6–B		HYS72D128320HU–6–B HYS72D128320GU–6–B		Unit	Note [1)2)]
Organization	**512MB**		**512MB**		**1 GB**		**1 GB**			
	×64		**×72**		**×64**		**×72**			
	1 Rank		**1 Rank**		**2 Ranks**		**2 Ranks**			
	–6		**–6**		**–6**		**–6**			
Symbol	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{DD0}	720	840	810	950	1000	1170	1130	1310	mA	3)
I_{DD1}	760	920	860	1040	1040	1250	1170	1400	mA	3)4)
I_{DD2P}	20	30	30	40	50	60	50	70	mA	5)
I_{DD2F}	200	240	230	270	400	480	450	540	mA	5)
I_{DD2Q}	140	190	150	220	270	380	310	430	mA	5)
I_{DD3P}	90	120	100	140	180	240	200	270	mA	5)
I_{DD3N}	280	330	320	370	560	660	630	740	mA	5)
I_{DD4R}	680	840	770	950	960	1170	1080	1310	mA	3)4)
I_{DD4W}	720	880	810	990	1000	1210	1130	1360	mA	3)
I_{DD5}	1720	2040	1940	2300	2000	2370	2250	2660	mA	3)
I_{DD6}	23	46	26	51	46	91	52	103	mA	5)
I_{DD7}	2200	2600	2480	2930	2480	2930	2790	3290	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

4 SPD Contents

Table 16 SPD Codes for HYS[64/72]D[64/128][300/320]GU–5–B

Product Type		HYS64D64300GU–5–B	HYS72D64300GU–5–B	HYS64D128320GU–5–B	HYS72D128320GU–5–B
Organization		512 MB	512 MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U–30330			
	JEDEC SPD Revision	Rev 0.0	Rev 0.0	Rev 0.0	Rev 0.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	50	50	50	50
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	75	75	75

Table 16 SPD Codes for HYS[64/72]D[64/128][300/320]GU–5–B (cont'd)

Product Type		**HYS64D64300GU–5–B**	**HYS72D64300GU–5–B**	**HYS64D128320GU–5–B**	**HYS72D128320GU–5–B**
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50
27	t_{RPmin} [ns]	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28
31	Module Density per Rank	80	80	80	80
32	$t_{AS,}$ tCS [ns]	60	60	60	60
33	$t_{AH,}$ tCH [ns]	60	60	60	60
34	t_{DS} [ns]	40	40	40	40
35	t_{DH} [ns]	40	40	40	40
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37
42	t_{RFCmin} [ns]	41	41	41	41
43	t_{CKmax} [ns]	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	3E	50	3F	51
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 -8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31

Table 16 SPD Codes for HYS[64/72]D[64/128][300/320]GU–5–B (cont'd)

Product Type		**HYS64D64300GU–5–B**	**HYS72D64300GU–5–B**	**HYS64D128320GU–5–B**	**HYS72D128320GU–5–B**
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	47	47	30	30
82	Part Number, Char 10	55	55	47	47
83	Part Number, Char 11	35	35	55	55
84	Part Number, Char 12	42	42	35	35
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

Table 17 SPD Codes for HYS[64/72]D[64/128][300/320]HU–5–B

Product Type		HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	50	50	50	50
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	75	75	75
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50

Table 17 SPD Codes for HYS[64/72]D[64/128][300/320]HU–5–B (cont'd)

Product Type		**HYS64D64300HU–5–B**	**HYS72D64300HU–5–B**	**HYS64D128320HU–5–B**	**HYS72D128320HU–5–B**
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
27	t_{RPmin} [ns]	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28
31	Module Density per Rank	80	80	80	80
32	$t_{AS,}$ tCS [ns]	60	60	60	60
33	$t_{AH,}$ tCH [ns]	60	60	60	60
34	t_{DS} [ns]	40	40	40	40
35	t_{DH} [ns]	40	40	40	40
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37
42	t_{RFCmin} [ns]	41	41	41	41
43	t_{CKmax} [ns]	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	3E	50	3F	51
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32

Table 17 SPD Codes for HYS[64/72]D[64/128][300/320]HU–5–B (cont'd)

Product Type		**HYS64D64300HU–5–B**	**HYS72D64300HU–5–B**	**HYS64D128320HU–5–B**	**HYS72D128320HU–5–B**
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	35	35	55	55
84	Part Number, Char 12	42	42	35	35
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

Table 18 SPD Codes for HYS[64/72]D[64/128][300/320]GU–6–B

Product Type		HYS64D64300GU–6–B	HYS72D64300GU–6–B	HYS64D128320GU–6–B	HYS72D128320GU–6–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00

Table 18 SPD Codes for HYS[64/72]D[64/128][300/320]GU–6–B (cont'd)

Product Type		HYS64D64300GU–6–B	HYS72D64300GU–6–B	HYS64D128320GU–6–B	HYS72D128320GU–6–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	80	80
32	t_{AS}, t_{CS} [ns]	75	75	75	75
33	t_{AH}, t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D
45	t_{QHSmax} [ns]	55	55	55	55
46	not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	42	54	43	55
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32

Table 18 SPD Codes for HYS[64/72]D[64/128][300/320]GU–6–B (cont'd)

Product Type		**HYS64D64300GU–6–B**	**HYS72D64300GU–6–B**	**HYS64D128320GU–6–B**	**HYS72D128320GU–6–B**
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	47	47	30	30
82	Part Number, Char 10	55	55	47	47
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	42	42	36	36
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

Table 19 SPD Codes for HYS[64/72]D[64/128][300/320]HU–6–B

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00

Table 19 SPD Codes for HYS[64/72]D[64/128][300/320]HU–6–B

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	80	80
32	t_{AS}, t_{CS} [ns]	75	75	75	75
33	t_{AH}, t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D
45	t_{QHSmax} [ns]	55	55	55	55
46	not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	42	54	43	55
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32

Table 19 SPD Codes for HYS[64/72]D[64/128][300/320]HU–6–B

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		**512 MB**	**512 MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**			
	JEDEC SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	42	42	36	36
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

5 Package Outlines

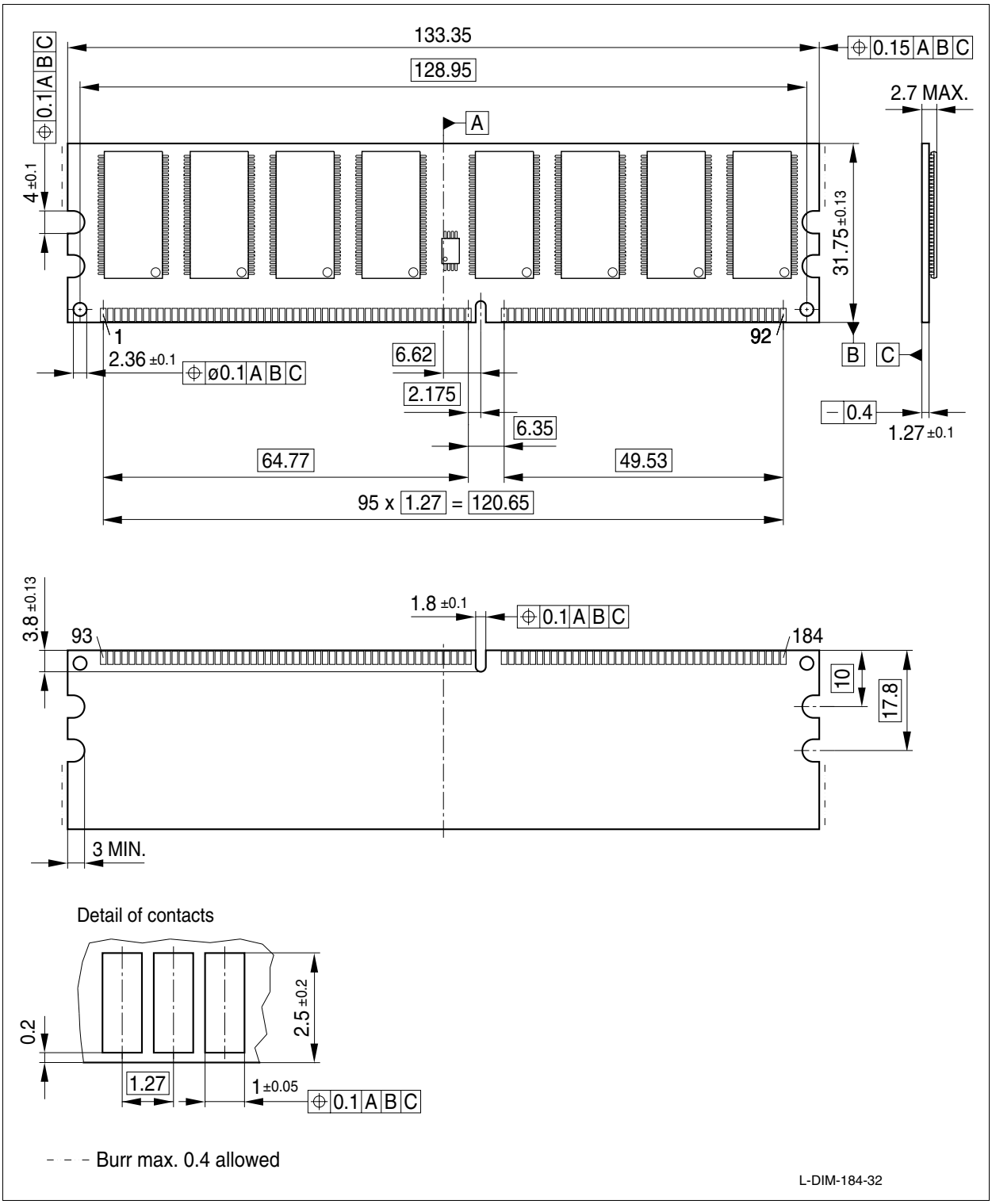

Figure 7 Raw Card A DDR UDIMM HYS64D64300HU-[5/6/7]-B (1 Rank Module)

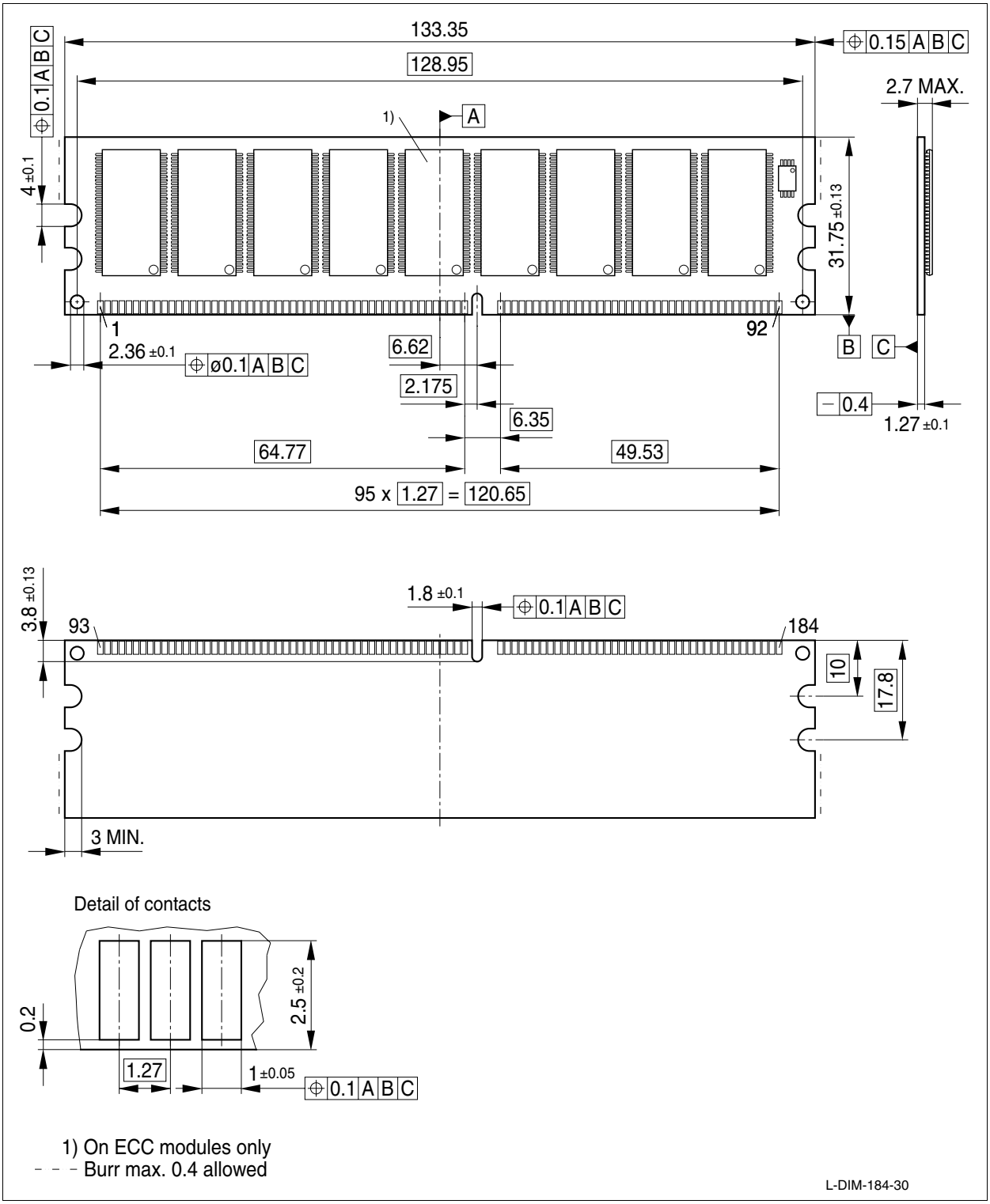

Figure 8 Raw Card A DDR UDIMM HYS72D64300HU-[5/6/7F]-B (1 Rank Module)

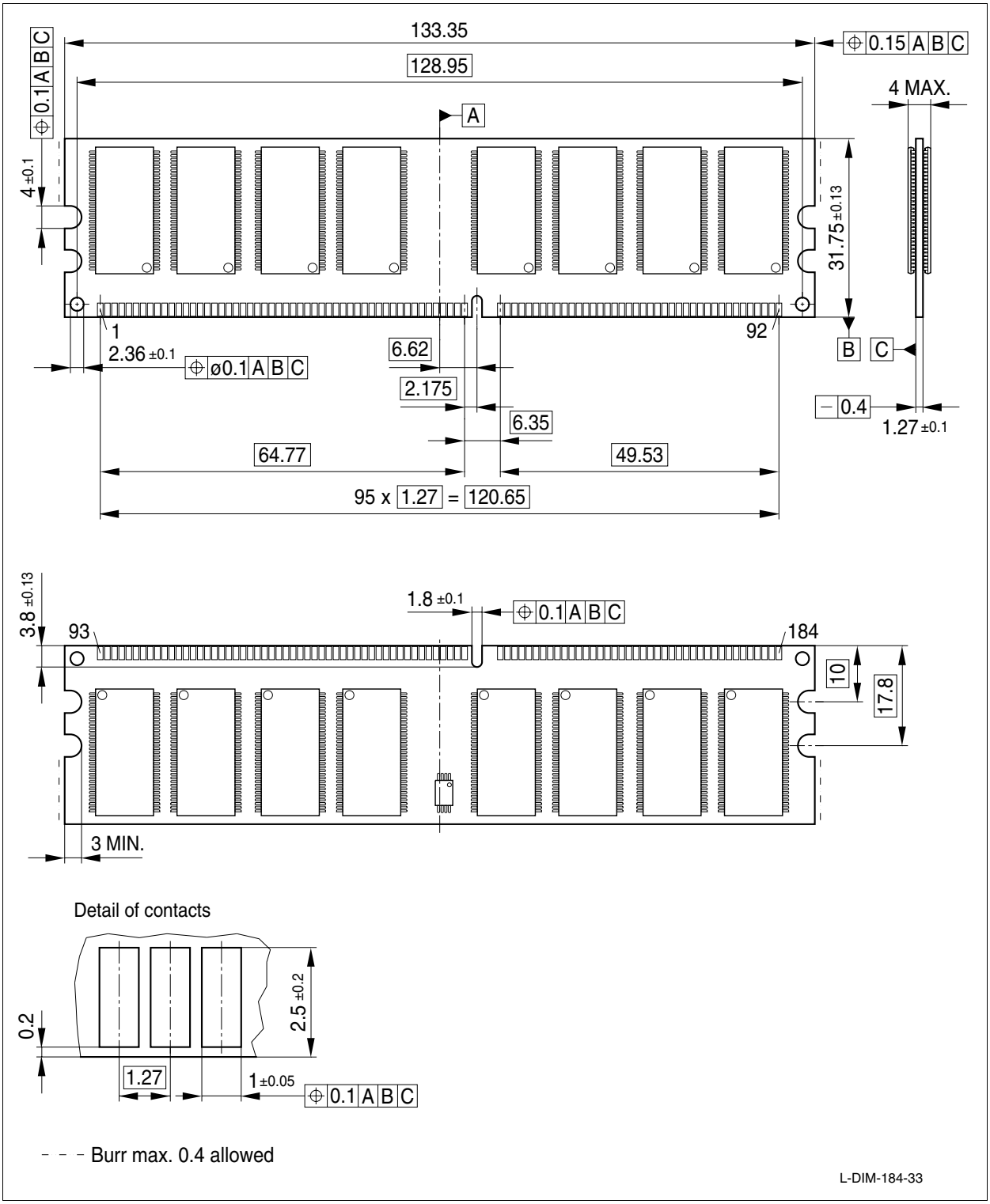

Figure 9 Raw Card B DDR UDIMM HYS64D128320HU-[5/6/7]-B (2 Ranks Module)

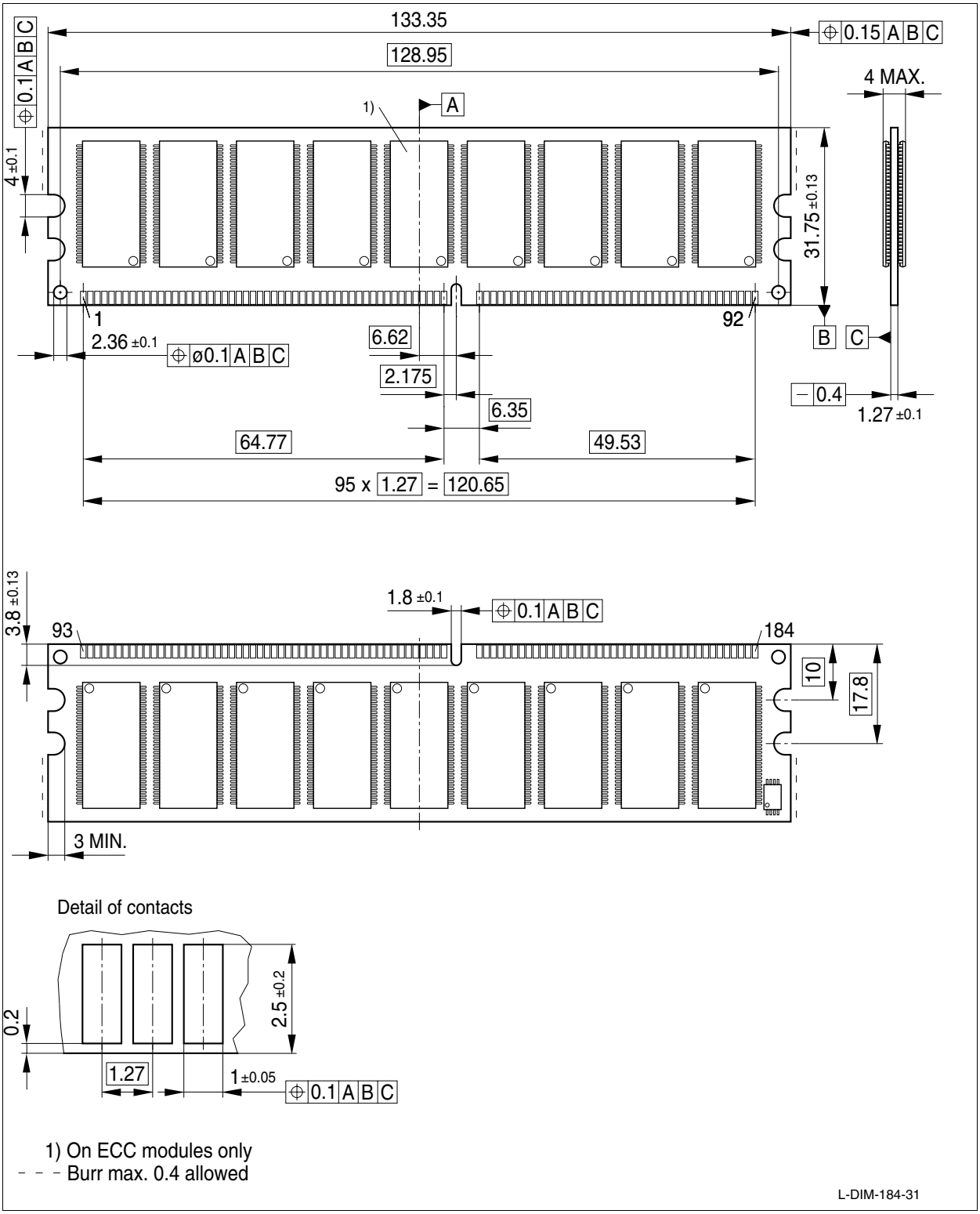

Figure 10 Raw Card B DDR UDIMM HYS72D128320HU-[5/6/7/-B (2 Rank Module)

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