SIEMENS

3.3 V 16M × 64/72-Bit SDRAM Modules — HYS 64/72V16200GU
3.3 V 32M × 64/72-Bit SDRAM Modules — HYS 64/72V32220GU
3.3 V 64M × 64/72-Bit SDRAM Modules — HYS 64/72V32200GU
HYS 64/72V64220GU

PC100-168 pin unbuffered DIMM Modules

Preliminary Information

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- One bank 16M × 64, 16M × 72, 32M × 64 and 32M × 72 organization
- Two bank 32M × 64, 32M × 72, 64M × 64 and 64M × 72 organization
- Optimized for byte-write non-parity or ECC applications
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- JEDEC standard Synchronous DRAMs (SDRAM)
- SDRAM Performance:

		-8	-8B	Units
f_{CK}	Clock frequency (max.)	100	100	MHz
t_{AC}	Clock access time	6	6	ns

- Programmed Latencies:

Product Speed		CL	t_{RCD}	t_{RP}
-8	PC100	2	2	2
-8B	PC100	3	2	3

- Single + 3.3 V (± 0.3 V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes 32M × 8 SDRAMs in TSOPII-54 packages
- Uses SIEMENS 128Mbit and 256Mbit SDRAM components
- Gold contact pad
- Card Size: 133.35 mm × 31.75 mm × 4.00 mm

The HYS 64/72V1600, HYS 64/72V32220, HYS 64/72V32200 and HYS 64/72V64220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 16M × 64, 16M × 72, 32M × 64 and 32M × 72 in 1 bank and 32M × 64, 32M × 72, 64M × 64 and 64M × 72 in two banks high speed memory arrays designed with 128M and 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -8 and -8B speed sort for 16M × 8 and 32M × 8 SDRAM devices in TSOP-54 packages to meet the PC100 requirement. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC 100 module specification.

The DIMMs have a serial presence detect, implemented with a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25“ (31.75 mm) height.

Ordering Information

Type	Ordering Code	Package	Descriptions	Module Height
HYS 64V16200GU-8	PC100-222-620	L-DIM-168-30	PC100 16M × 64 1 bank SDRAM module	1.25“
HYS 72V16200GU-8	PC100-222-620	L-DIM-168-30	PC100 16M × 72 1 bank SDRAM module	1.25“
HYS 64V32220GU-8	PC100-222-620	L-DIM-168-30	PC100 32M × 64 2 bank SDRAM module	1.25“
HYS 72V32220GU-8	PC100-222-620	L-DIM-168-30	PC100 32M × 72 2 bank SDRAM module	1.25“
HYS 64V16200GU-8B	PC100-323-620	L-DIM-168-30	PC100 16M × 64 1 bank SDRAM module	1.25“
HYS 72V16200GU-8B	PC100-323-620	L-DIM-168-30	PC100 16M × 72 1 bank SDRAM module	1.25“
HYS 64V32220GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M × 64 2 bank SDRAM module	1.25“
HYS 72V32220GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M × 72 2 bank SDRAM module	1.25“
HYS 64V32200GU-8	PC100-222-620	L-DIM-168-30	PC100 32M × 64 1 bank SDRAM module	1.25“
HYS 72V32200GU-8	PC100-222-620	L-DIM-168-30	PC100 32M × 72 1 bank SDRAM module	1.25“
HYS 64V64220GU-8	PC100-222-620	L-DIM-168-30	PC100 64M × 64 2 bank SDRAM module	1.25“
HYS 72V64220GU-8	PC100-222-620	L-DIM-168-30	PC100 64M × 72 2 bank SDRAM module	1.25“

Ordering Information (cont'd)

Type	Ordering Code	Package	Descriptions	Module Height
HYS 64V32200GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M × 64 1 bank SDRAM module	1.25"
HYS 72V32200GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M × 72 1 bank SDRAM module	1.25"
HYS 64V64220GU-8B	PC100-323-620	L-DIM-168-30	PC100 64M × 64 2 bank SDRAM module	1.25"
HYS 72V64220GU-8B	PC100-323-620	L-DIM-168-30	PC100 64M × 72 2 bank SDRAM module	1.25"

Pin Names

A0-A12	Address Inputs (RA0 ~ RA10/CA0 ~ CA9)	CLK0 - CLK3	Clock Input
BA0, BA1	Bank Selects	DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output	$\overline{CS0}$ - $\overline{CS3}$	Chip Select
CB0-CB7	Check Bits (× 72 organization only)	V_{CC}	Power (+ 3.3 Volt)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out for Presence Detect
$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable	N.C. / DU	No Connection

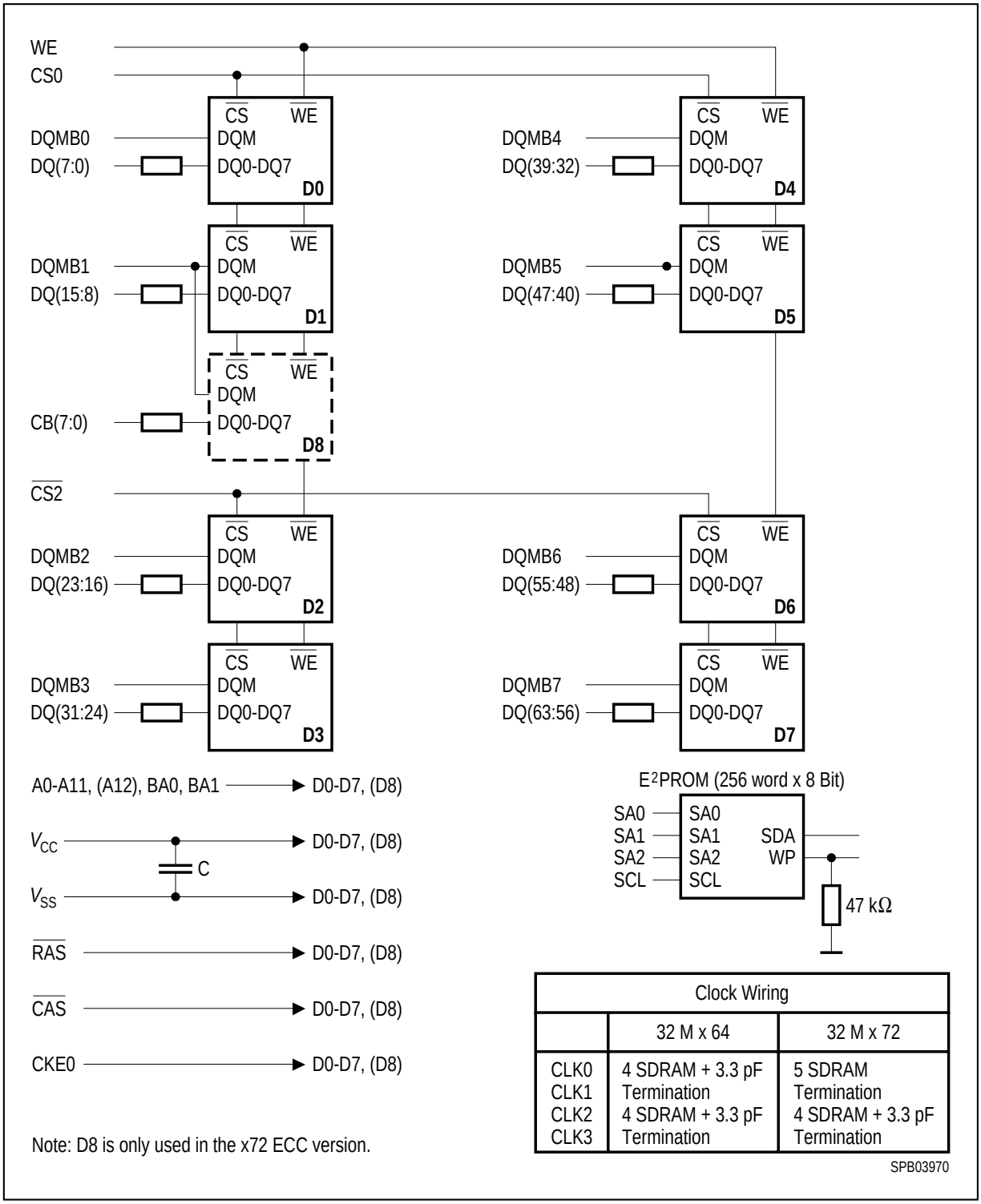
Address Format

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
16M × 64/72	HYS 64/72V16200GU	12	10	2	4k	64ms	15.6 µ
32M × 64/72	HYS 64/72V32220GU	12	10	2	4k	64ms	15.6 µ
32M × 64/72	HYS 64/72V32220GU	13	10	2	8k	64ms	7.8 µ
64M × 64/72	HYS 64/72V64220GU	13	10	2	8k	64ms	7.8 µ

Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	$\overline{CKE0}$
3	DQ1	45	$\overline{CS2}$	87	DQ33	129	$\overline{CS3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{CC}	48	DU	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC (CB2)	94	DQ39	136	CB6
11	DQ8	53	NC (CB3)	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC (CB0)	63	$\overline{CKE1}$	105	NC (CB4)	147	NC
22	NC (CB1)	64	V_{SS}	106	NC (CB5)	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{CS0}$	72	DQ27	114	$\overline{CS1}$	156	DQ59
31	DU	73	V_{CC}	115	$\overline{RAS}$	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{CC}	126	A12	168	V_{CC}

Note: Pinnames in brackets are for the x72 ECC versions

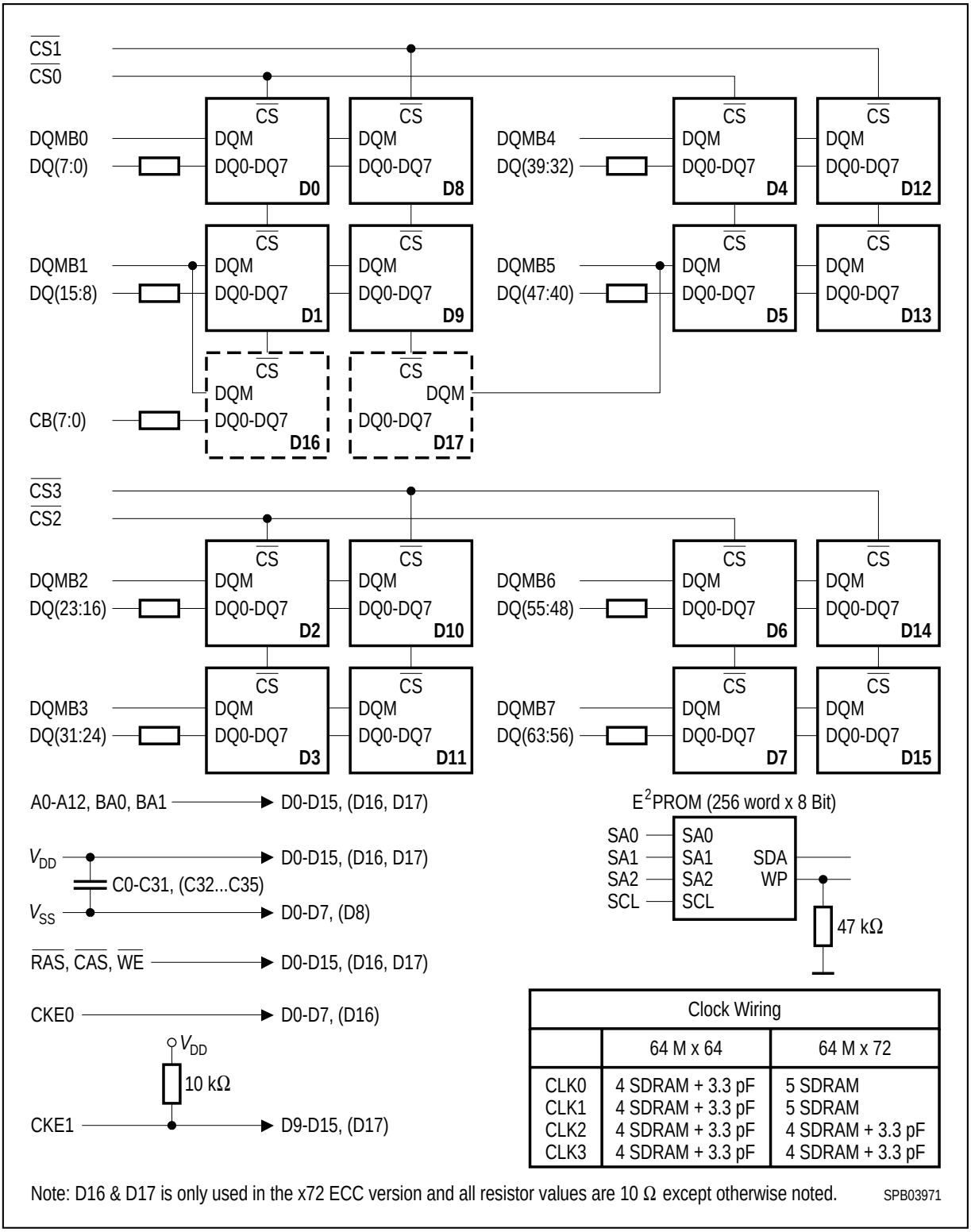


Note: D8 is only used in the x72 ECC version.

Clock Wiring		
	32 M x 64	32 M x 72
CLK0 CLK1 CLK2 CLK3	4 SDRAM + 3.3 pF Termination 4 SDRAM + 3.3 pF Termination	5 SDRAM Termination 4 SDRAM + 3.3 pF Termination

SPB03970

Block Diagram for 16M × 64/72 & 32M × 64/72 one bank SDRAM DIMM Modules (HYS 64/72V16200GU & HYS 64/72V32200GU)



Clock Wiring		
	64 M x 64	64 M x 72
CLK0	4 SDRAM + 3.3 pF	5 SDRAM
CLK1	4 SDRAM + 3.3 pF	5 SDRAM
CLK2	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF
CLK3	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF

Note: D16 & D17 is only used in the x72 ECC version and all resistor values are 10 Ω except otherwise noted. SPB03971

Block Diagram for 32M × 64/72 & 64M × 64/72 two bank SDRAM DIMM Modules

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 40	40	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		max. 32M×64	max. 32M×72	max. 32M×64	max. 32M×72	
Input capacitance (A0 to A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	45	55	80	90	pF
Input capacitance ($\overline{CS0}$ - $\overline{CS3}$)	C_{I2}	20	25	30	35	pF
Input capacitance (CLK0 - CLK3)	C_{ICL}	22	38	22	38	pF
Input capacitance ($\overline{CKE0}$, $\overline{CKE1}$)	C_{I3}	22	38	50	55	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	13	13	20	20	pF
Input/Output capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	13	12	20	20	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	8	8	pF
Input/Output Capacitance	C_{SD}	10	10	10	10	pF

Operating Currents

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V [1]

Recommended Operating Conditions unless otherwise noted

Parameter & Test Condition		Symb.	-8/-8B	-10	Unit	Note
			max.			
Operating current $t_{RC} \geq t_{RC(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access		I_{CC1} × 4 × 8 × 16	 210 210 210	 165 165 165	 mA mA mA	2
Precharged Standby Current in Power Down Mode $\overline{CS}$ = $V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	2	2	mA	2
Precharged Standby Current in Non-power Down Mode $\overline{CS}$ = $V_{IH(MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	19	16	mA	2
No operating current t_{CK} = min., $\overline{CS}$ = $V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	45	40	mA	2
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	10	10	mA	2
Burst operating current t_{CK} = min., Read command cycling	–	I_{CC4} × 4 × 8 × 16	 210 210 210	 165 165 165	 mA mA mA	2, 3
Auto refresh current t_{CK} = min., Auto Refresh command cycling	–	I_{CC5}	240	195	mA	2
Self refresh current Self Refresh Mode, CKE = 0.2 V	standard version	I_{CC6}	2.5	2.5	mA	2

Notes

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 100 MHz for -8 and at 66 MHz for -10 parts. Input signals are changed once during t_{CK}, excepts for I_{CC6} and for standby currents when t_{CK} = infinity.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 is assumed and the V_{DDQ} current is excluded.

AC Characteristics [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8 PC100-222		-8B PC100-323			
		min.	max.	min.	max.		
Clock and Clock Enable							
Clock Cycle Time	t_{CK}						
$\overline{CAS}$ Latency = 3		10	–	10	–	ns	
$\overline{CAS}$ Latency = 2		10	–	12	–	ns	
System Frequency	f_{CK}						
$\overline{CAS}$ Latency = 3		–	100	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	100	–	83	MHz	
Clock Access Time	t_{AC}						
$\overline{CAS}$ Latency = 3		–	6	–	6	ns	3, 4
$\overline{CAS}$ Latency = 2		–	6	–	7	ns	
Clock High Pulse Width	t_{CH}	3	–	3	–	ns	4
Clock Low Pulse Width	t_{CL}	3	–	3	–	ns	4
Input Setup Time	t_{CS}	2	–	2	–	ns	5
Input Hold Time	t_{CH}	1	–	1	–	ns	5
CKE Setup Time (Power down mode)	t_{CKSP}	2	–	2	–	ns	6
CKE Setup Time (Self Refresh Exit)	t_{CKSR}	10	–	–	–	ns	7
Transition Time (rise and fall)	t_T	1	–	–	–	ns	
Common Parameters							
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}	20	–	20	–	ns	
Cycle Time	t_{RC}	70	–	70	–	ns	
Active Command Period	t_{RAS}	48	–	48	–	ns	
Precharge Time	t_{RP}	20	–	30	–	ns	
Bank to Bank Delay Time	t_{RRD}	16	–	20	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (same bank)	t_{CCD}	1	–	1	–	CLK	

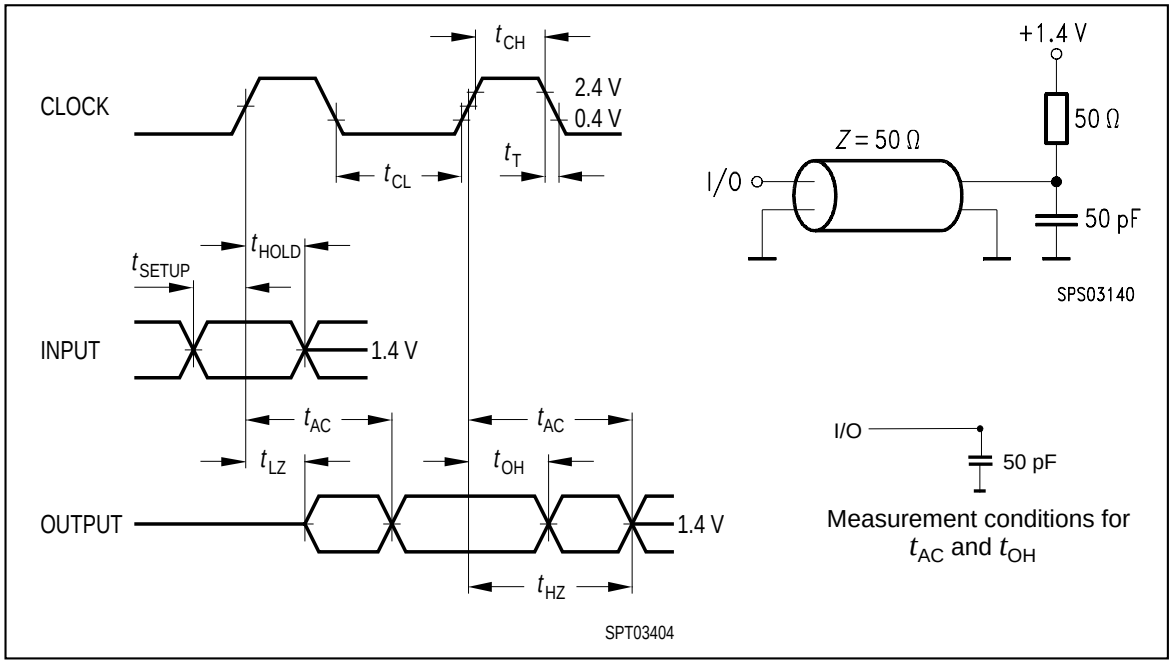
AC Characteristics (cont'd) [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8 PC100-222		-8B PC100-323			
		min.	max.	min.	max.		
Refresh Cycle							
Self Refresh Exit Time	t_{SREX}	10	–	10	–	ns	[9]
Refresh Period	t_{REF}	64	–	64	–	ms	[6]
Refresh Interval 128Mbit SDRAM based modules 256Mbit SDRAM based modules		 – –	 15.6 7.8	 – –	 15.6 7.8	 µs µs	
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	[2]
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	3	10	ns	[8]
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	
Write Cycle							
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	
Data In to Active/Refresh	t_{DAL}	5	–	5	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Notes

1. An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit show. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resisitve termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.



3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
4. Rated at 1.5 V
5. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
6. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
7. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
8. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus).

SPD-Table for 256MBit SDRAM based PC100 Modules

Byte#	Description	SPD Entry Value	Hex			
			32M×64 one bank -8	32M×64 one bank -8B	32M×72 one bank -8	32M×72 one bank -8B
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D	0D
4	Number of Column Addresses (for 32M×8 SDRAMs)	10	0A	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	64/72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL = 3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL = 3	6.0 ns	60	60	60	60
11	Dimm Configuration	none / ECC	00	00	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82	82	82	82
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a/x8	00	00	08	08
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	4	04	04	04	04

SPD-Table for 256MBit SDRAM based PC100 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			32M×64 one bank -8	32M×64 one bank -8B	32M×72 one bank -8	32M×72 one bank -8B
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	$\overline{WE}$ Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/ non re.	00	00	00	00
22	SDRAM Device Attributes: General	V_{CC} tol ± 10%	06	06	06	06
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 / 12.0 ns	A0	C0	A0	C0
24	Max. data access time from Clock for CL = 2	6.0 / 7.0 ns	60	70	60	70
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 / 30 ns	14	1E	14	1E
28	Minimum Row Active to Row Active delay t_{RRD}	16 / 20 ns	10	14	10	14
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay t_{RCD}	20 ns	14	14	14	14
30	Minimum RAS pulse width t_{RAS}	50 / 60 ns	32	3C	32	3C
31	Module Bank Density (per bank)	256 MByte	40	40	40	40
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input hold time	2 ns	20	20	20	20
35	SDRAM data input setup time	1 ns	10	10	10	10

SPD-Table for 256MBit SDRAM based PC100 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			32M×64 one bank -8	32M×64 one bank -8B	32M×72 one bank -8	32M×72 one bank -8B
62-61	Superset information (may be used in future)	–	FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62	–	–	–	–	–
64-125	Manufacturers information (optional) (FF_H if not used)	–	XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz support details	–	AF	AD	AF	AD
128+	Unused storage locations	–	FF	FF	FF	FF

SPD-Table for 256MBit SDRAM based PC100 Modules

Byte#	Description	SPD Entry Value	Hex			
			64M×64 two bank -8	64M×64 two bank -8B	64M×72 two bank -8	64M×72 two bank -8B
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D	0D
4	Number of Column Addresses (for 32M × 8 SDRAMs)	10	0A	0A	0A	0A
5	Number of DIMM Banks	2	02	02	02	02
6	Module Data Width	64/72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL = 3	10.0 ns	A0	A0	A0	A0

SPD-Table for 256MBit SDRAM based PC100 Modules (cont'd)

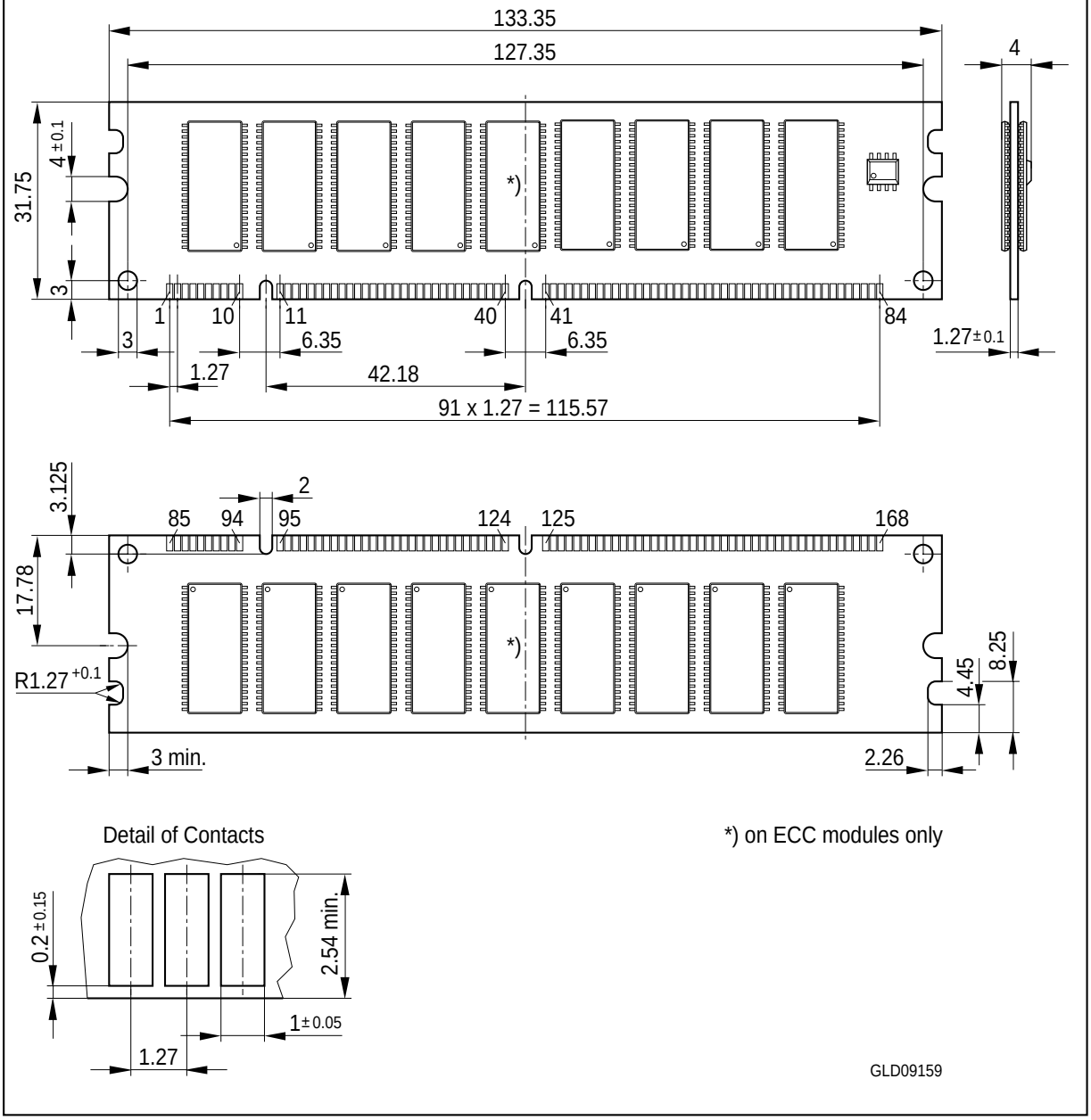
Byte#	Description	SPD Entry Value	Hex			
			64M×64 two bank -8	64M×64 two bank -8B	64M×72 two bank -8	64M×72 two bank -8B
10	SDRAM Access time from Clock at CL = 3	6.0 ns	60	60	60	60
11	Dimm Configuration	none/ECC	00	00	02	02
12	Refresh Rate/Type	Self Refresh, 7.8 µs	82	82	82	82
13	SDRAMwidth,Primary	× 8	08	08	08	08
14	Error Checking SDRAM data width	n/a/× 8	00	00	08	08
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	4	04	04	04	04
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	$\overline{WE}$ Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/ non re.	00	00	00	00
22	SDRAM Device Attributes: General	V_{CC} tol ± 10%	06	06	06	06
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0/12.0 ns	A0	C0	A0	C0
24	Max. data access time from Clock for CL = 2	6.0/7.0 ns	60	70	60	70
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20/30 ns	14	1E	14	1E

SPD-Table for 256MBit SDRAM based PC100 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			64M×64 two bank -8	64M×64 two bank -8B	64M×72 two bank -8	64M×72 two bank -8B
28	Minimum Row Active to Row Active delay t_{RRD}	16/20 ns	10	14	10	14
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay t_{RCD}	20 ns	14	14	14	14
30	Minimum $\overline{RAS}$ pulse width t_{RAS}	50/60 ns	32	3C	32	3C
31	Module Bank Density (per bank)	256 MByte	40	40	40	40
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input hold time	2 ns	20	20	20	20
35	SDRAM data input setup time	1 ns	10	10	10	10
62-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		10	65	22	77
64-125	Manufacturers information (optional) (FF_H if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz support details		FF	FD	FF	FD
128+	Unused storage locations		FF	FF	FF	FF

Package Outlines

L-DIM-168-30
SDRAM DIMM Module Package



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm