

# DDR2 Registered SDRAM MODULE

**240pin Registered Module based on 1Gb A-die**

**72-bit ECC**

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## Revision History

Revision	Month	Year	History
1.0	July	2005	- Initial Release
1.1	Aug.	2005	- Revised IDD Current Values
1.2	Sep.	2005	- Revised the Ordering Information

## DDR2 Registered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Parity Register	Height
M393T2863AZ3-CD5/CC	1GB	128Mx72	128Mx8(K4T1G084QA)*9EA	1	X	30mm
M393T2863AZA-CE6/D5/CC	1GB	128Mx72	128Mx8(K4T1G084QA)*9EA	1	O	30mm
M393T5663AZ3-CD5/CC	2GB	256Mx72	128Mx8(K4T1G084QA)*18EA	2	X	30mm
M393T5663AZA-CE6/D5/CC	2GB	256Mx72	128Mx8(K4T1G084QA)*18EA	2	O	30mm
M393T5660AZ3-CD5/CC	2GB	256Mx72	256Mx4(K4T1G044QA)*18EA	1	X	30mm
M393T5660AZA-CE6/D5/CC	2GB	256Mx72	256Mx4(K4T1G044QA)*18EA	1	O	30mm
M393T5168AZ0-CD5/CC	4GB	512Mx72	st.512Mx4(K4T2G064QA)*18EA	2	X	30mm
M393T5166AZA-CE6/D5/CC	4GB	512Mx72	st.512Mx4(K4T2G264QA)*18EA	2	O	30mm

Note: "Z" of Part number(11th digit) stand for Lead-free products.

Note: "3" of Part number(12th digit) stand for Dummy Pad PCB products.

Note: "A" of Part number(12th digit) stand for Parity Register products.

## Features

- Performance range

	E6(DDR2-667)	D5(DDR2-533)	CC(DDR2-400)	Unit
Speed@CL3	400	400	400	Mbps
Speed@CL4	533	533	400	Mbps
Speed@CL5	667	533	-	Mbps
CL-tRCD-tRP	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- $V_{DDQ} = 1.8V \pm 0.1V$
- 200 MHz  $f_{CK}$  for 400Mb/sec/pin, 267MHz  $f_{CK}$  for 533Mb/sec/pin, 333MHz  $f_{CK}$  for 667Mb/sec/pin
- 8 Banks
- Posted  $\overline{CAS}$
- Programmable  $\overline{CAS}$  Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- PASR(Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a  $T_{CASE} 85^{\circ}C$ , 3.9us at  $85^{\circ}C < T_{CASE} \leq 95^{\circ}C$   
- support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 68ball FBGA - 256Mx4/128Mx8, 56ball BGA - st.512Mbx4
- All of Lead-free products are compliant for RoHS

Note: For detailed DDR2 SDRAM operation, please refer to Samsung's Device operation & Timing diagram..

## Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
256Mx4(1Gb) based Module	A0-A13	A0-A9, A11	BA0-BA2	A10
128Mx8(1Gb) based Module	A0-A13	A0-A9	BA0-BA2	A10

Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V <sub>REF</sub>	121	V <sub>SS</sub>	31	DQ19	151	V <sub>SS</sub>	61	A4	181	V <sub>DDQ</sub>	91	V <sub>SS</sub>	211	DM5/DQS14
2	V <sub>SS</sub>	122	DQ4	32	V <sub>SS</sub>	152	DQ28	62	V <sub>DDQ</sub>	182	A3	92	$\overline{\text{DQS5}}$	212	NC/ $\overline{\text{DQS14}}$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V <sub>SS</sub>
4	DQ1	124	V <sub>SS</sub>	34	DQ25	154	V <sub>SS</sub>	64	V <sub>DD</sub>	184	V <sub>DD</sub>	94	V <sub>SS</sub>	214	DQ46
5	V <sub>SS</sub>	125	DM0/DQS9	35	V <sub>SS</sub>	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{\text{DQS0}}$	126	NC/ $\overline{\text{DQS9}}$	36	$\overline{\text{DQS3}}$	156	NC/ $\overline{\text{DQS12}}$	65	V <sub>SS</sub>	185	CK0	96	DQ43	216	V <sub>SS</sub>
7	DQS0	127	V <sub>SS</sub>	37	DQS3	157	V <sub>SS</sub>	66	V <sub>SS</sub>	186	$\overline{\text{CK0}}$	97	V <sub>SS</sub>	217	DQ52
8	V <sub>SS</sub>	128	DQ6	38	V <sub>SS</sub>	158	DQ30	67	V <sub>DD</sub>	187	V <sub>DD</sub>	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC/Par_In	188	A0	99	DQ49	219	V <sub>SS</sub>
10	DQ3	130	V <sub>SS</sub>	40	DQ27	160	V <sub>SS</sub>	69	V <sub>DD</sub>	189	V <sub>DD</sub>	100	V <sub>SS</sub>	220	RFU
11	V <sub>SS</sub>	131	DQ12	41	V <sub>SS</sub>	161	CB4	70	A10/AP	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V <sub>DDQ</sub>	102	NC(TEST)	222	V <sub>SS</sub>
13	DQ9	133	V <sub>SS</sub>	43	CB1	163	V <sub>SS</sub>	72	V <sub>DDQ</sub>	192	RAS	103	V <sub>SS</sub>	223	DM6/DQS15
14	V <sub>SS</sub>	134	DM1/DQS10	44	V <sub>SS</sub>	164	DM8/DQS17	73	WE	193	$\overline{\text{S0}}$	104	$\overline{\text{DQS6}}$	224	NC/ $\overline{\text{DQS15}}$
15	$\overline{\text{DQS1}}$	135	NC/ $\overline{\text{DQS10}}$	45	$\overline{\text{DQS8}}$	165	NC/ $\overline{\text{DQS17}}$	74	CAS	194	V <sub>DDQ</sub>	105	DQS6	225	V <sub>SS</sub>
16	DQS1	136	V <sub>SS</sub>	46	DQS8	166	V <sub>SS</sub>	75	V <sub>DDQ</sub>	195	ODT0	106	V <sub>SS</sub>	226	DQ54
17	V <sub>SS</sub>	137	RFU	47	V <sub>SS</sub>	167	CB6	76	$\overline{\text{S1}}^4$	196	A13	107	DQ50	227	DQ55
18	RESET	138	RFU	48	CB2	168	CB7	77	ODT1	197	V <sub>DD</sub>	108	DQ51	228	V <sub>SS</sub>
19	NC	139	V <sub>SS</sub>	49	CB3	169	V <sub>SS</sub>	78	V <sub>DDQ</sub>	198	V <sub>SS</sub>	109	V <sub>SS</sub>	229	DQ60
20	V <sub>SS</sub>	140	DQ14	50	V <sub>SS</sub>	170	V <sub>DDQ</sub>	79	V <sub>SS</sub>	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V <sub>DDQ</sub>	171	CKE1 <sup>4</sup>	80	DQ32	200	DQ37	111	DQ57	231	V <sub>SS</sub>
22	DQ11	142	V <sub>SS</sub>	52	CKE0	172	V <sub>DD</sub>	81	DQ33	201	V <sub>SS</sub>	112	V <sub>SS</sub>	232	DM7/DQS16
23	V <sub>SS</sub>	143	DQ20	53	V <sub>DD</sub>	173	NC	82	V <sub>SS</sub>	202	DM4/DQS13	113	$\overline{\text{DQS7}}$	233	NC/ $\overline{\text{DQS16}}$
24	DQ16	144	DQ21	54	BA2	174	NC	83	$\overline{\text{DQS4}}$	203	NC/ $\overline{\text{DQS13}}$	114	DQS7	234	V <sub>SS</sub>
25	DQ17	145	V <sub>SS</sub>	55	NC/Err_Out	175	V <sub>DDQ</sub>	84	DQS4	204	V <sub>SS</sub>	115	V <sub>SS</sub>	235	DQ62
26	V <sub>SS</sub>	146	DM2/DQS11	56	V <sub>DDQ</sub>	176	A12	85	V <sub>SS</sub>	205	DQ38	116	DQ58	236	DQ63
27	$\overline{\text{DQS2}}$	147	NC/ $\overline{\text{DQS11}}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V <sub>SS</sub>
28	DQS2	148	V <sub>SS</sub>	58	A7	178	V <sub>DD</sub>	87	DQ35	207	V <sub>SS</sub>	118	V <sub>SS</sub>	238	VDDSPD
29	V <sub>SS</sub>	149	DQ22	59	V <sub>DD</sub>	179	A8	88	V <sub>SS</sub>	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V <sub>SS</sub>				

NC = No Connect, RFU = Reserved for Future Use

1. RESET (Pin 18) is connected to both OE of PLL and Reset of register.
2. The Test pin (Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)
3. NC/Err\_Out ( Pin 55) and NC/Par\_In (Pin 68) are for optional function to check address and command parity.
4. CKE1, $\overline{\text{S1}}$  Pin is used for double side Registered DIMM.

Pin Description

Pin Name	Description	Pin Name	Description
CK0	Clock Inputs, positive line	ODT0~ODT1	On die termination
$\overline{\text{CK0}}$	Clock inputs, negative line	DQ0~DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	CB0~CB7	Data check bits Input/Output
RAS	Row Address Strobe	DQS0~DQS8	Data strobes
CAS	Column Address Strobe	$\overline{\text{DQS0}}\sim\overline{\text{DQS8}}$	Data strobes, negative line
$\overline{\text{WE}}$	Write Enable	DM(0~8), DQS(9~17)	Data Masks / Data strobes (Read)
$\overline{\text{S0}}, \overline{\text{S1}}$	Chip Selects	$\overline{\text{DQS9}}\sim\overline{\text{DQS17}}$	Data strobes (Read), negative line
A0~A9, A11~A13	Address Inputs	RFU	Reserved for Future Use
A10/AP	Address Input/Autoprecharge	NC	No Connect
BA0~BA2	DDR2 SDRAM Bank Address	TEST	Memory bus test tool (Not Connect and Not Useable on DIMMs)
SCL	Serial Presence Detect (SPD) Clock Input	V <sub>DD</sub>	Core Power
SDA	SPD Data Input/Output	V <sub>DDQ</sub>	I/O Power
SA0~SA2	SPD address	V <sub>SS</sub>	Ground
Par_In	Parity bit for the Address and Control bus	V <sub>REF</sub>	Input/Output Reference
Err_Out	Parity error found in the Address and Control bus	V <sub>DDSPD</sub>	SPD Power
RESET	Register and PLL control pin		

\* The VDD and VDDQ pins are tied to the single power-plane on PCB.

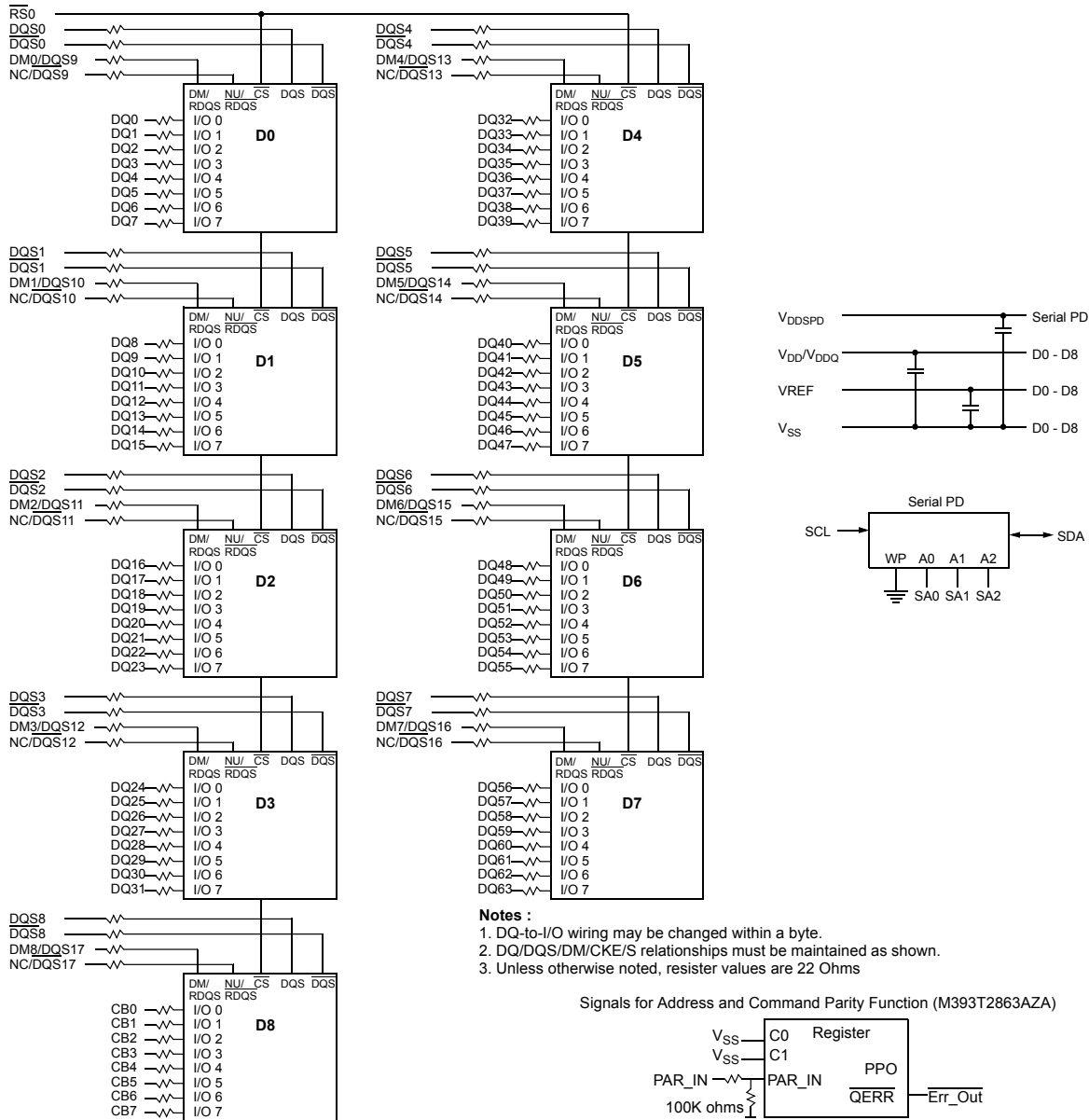
## Input/Output Function Description

Symbol	Type	Description
CK0	Input	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	Input	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0~CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$ ~ $\overline{S1}$	Input	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high.
ODT0~ODT1	Input	I/O bus impedance control signals.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	When sampled at the positive rising edge of the clock, $\overline{CAS}$ , $\overline{RAS}$ , and $\overline{WE}$ define the operation to be executed by the SDRAM.
V <sub>REF</sub>	Supply	Reference voltage for SSTL_18 inputs
V <sub>DDQ</sub>	Supply	Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0~BA2	Input	Selects which SDRAM bank of eight is activated.
A0~A9,A10/AP A11~A13	Input	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ0~63, CB0~CB7	In/Out	Data and Check Bit Input/Output pins
DM0~DM8	Input	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V <sub>DD</sub> , V <sub>SS</sub>	Supply	Power and ground for the DDR SDRAM input buffers and core logic
DQS0~DQS17	In/Out	Positive line of the differential data strobe for input and output data.
$\overline{DQS0}$ ~ $\overline{DQS17}$	In/Out	Negative line of the differential data strobe for input and output data.
SA0~SA2	Input	These signals are tied at the system planar to either V <sub>SS</sub> or V <sub>DDSPD</sub> to configure the serial SPD EEPROM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V <sub>DDSPD</sub> to act as a pullup.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V <sub>DDSPD</sub> to act as a pullup.
V <sub>DDSPD</sub>	Supply	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt operation).
$\overline{RESET}$	Input	The $\overline{RESET}$ pin is connected to the $\overline{RST}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (The PLL will remain synchronized with the input clock )
Par_In	Input	Parity bit for the Address and Control bus. ( "1 " : Odd, "0 " : Even)
$\overline{Err\_Out}$	Input	Parity error found in the Address and Control bus
TEST	In/Out	Used by memory bus analysis tools (unused on memory DIMMs)

## Functional Block Diagram

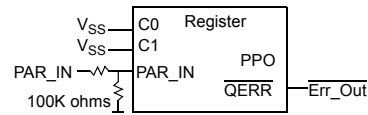
### 1GB, 128Mx72 Module (M393T2863AZ3/M393T2863AZA)

(populated as 1 rank of x8 DDR2 SDRAMs)

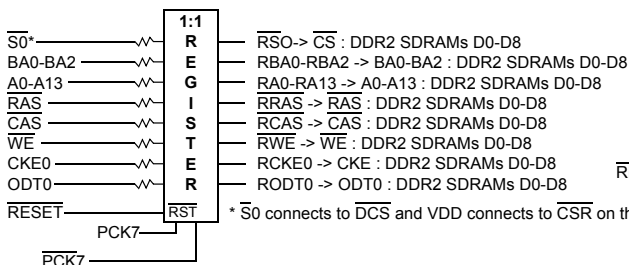


- Notes :**
1. DQ-to-I/O wiring may be changed within a byte.
  2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
  3. Unless otherwise noted, resistor values are 22 Ohms

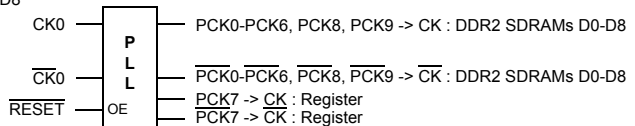
#### Signals for Address and Command Parity Function (M393T2863AZA)



The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address inputs"



\* S0 connects to  $\overline{DCS}$  and VDD connects to  $\overline{CSR}$  on the register.

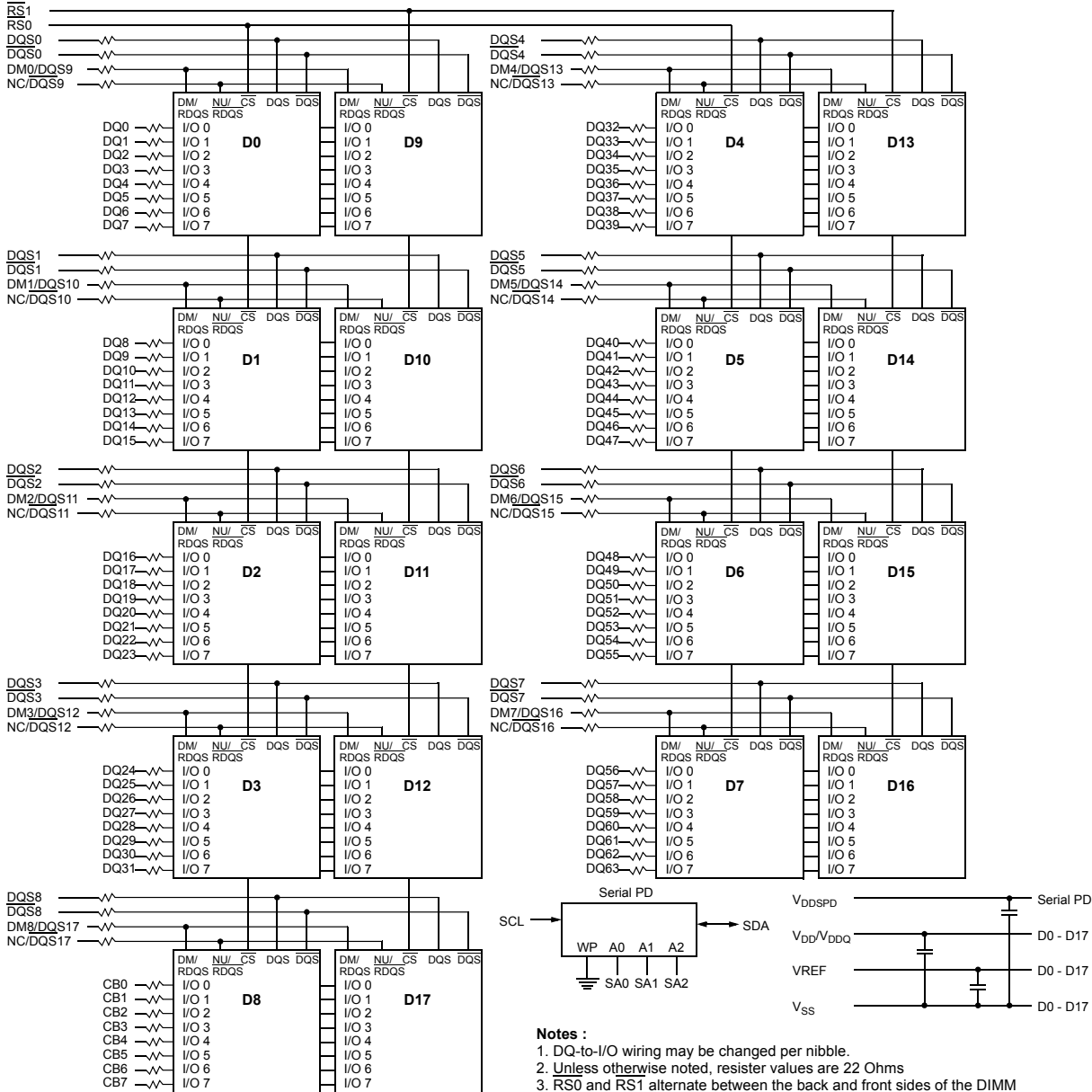


# 1GB, 2GB, 4GB Registered DIMMs

# DDR2 SDRAM

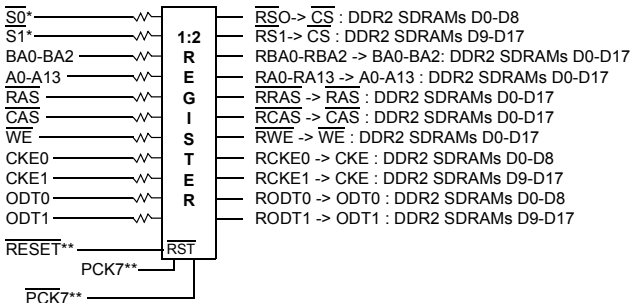
## 2GB, 256Mx72 Module (M393T5663AZ3/M393T5663AZA)

(populated as 2 rank of x8 DDR2 SDRAMs)



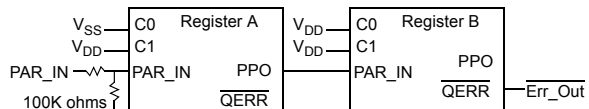
**Notes :**

1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resistor values are 22 Ohms
3. RS0 and RS1 alternate between the back and front sides of the DIMM

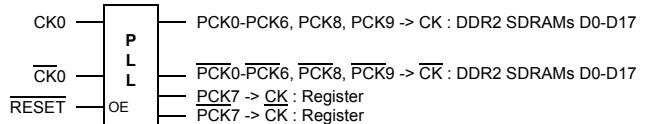


\* S0 connects to DCS and S0 connects to CSR on a Register,  
 S1 connects to DCS and S0 connects to CSR on another Register.  
 \*\* RESET, PCK7 and PCK7 connects to both Registers.  
 Other signals connect to one of two Registers.

Signals for Address and Command Parity Function (M393T5663AZA)



The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address inputs"



Rev. 1.2 Sep. 2005

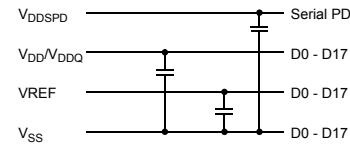
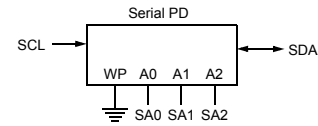
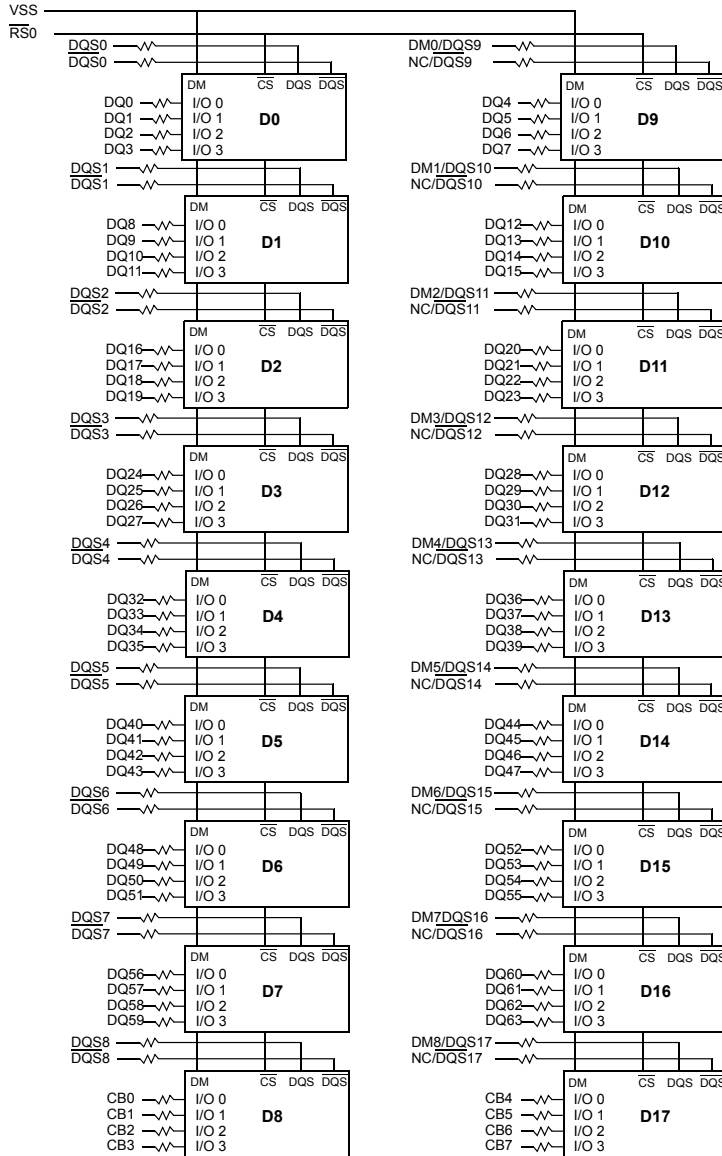


# 1GB, 2GB, 4GB Registered DIMMs

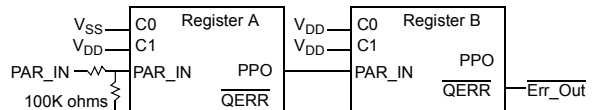
# DDR2 SDRAM

## 2GB, 256Mx72 Module (M393T5660AZ3/M393T5660AZA)

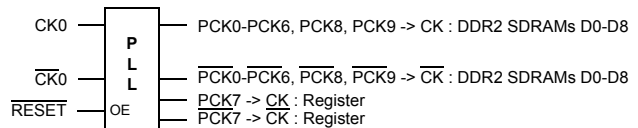
(populated as 1 rank of x4 DDR2 SDRAMs)



### Signals for Address and Command Parity Function (M393T5660AZA)

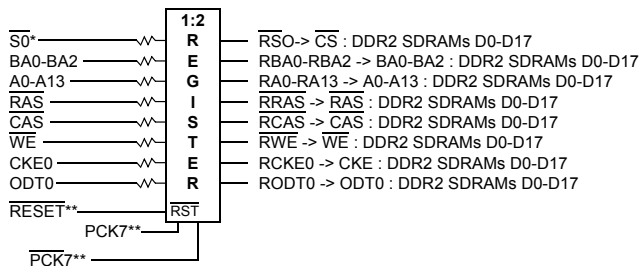


The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address inputs"



### Notes :

1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resistor values are 22 Ohms



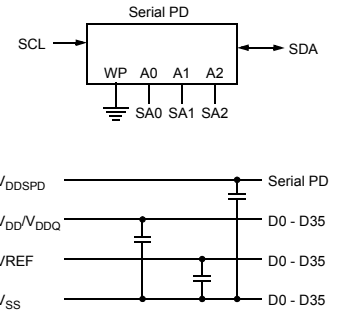
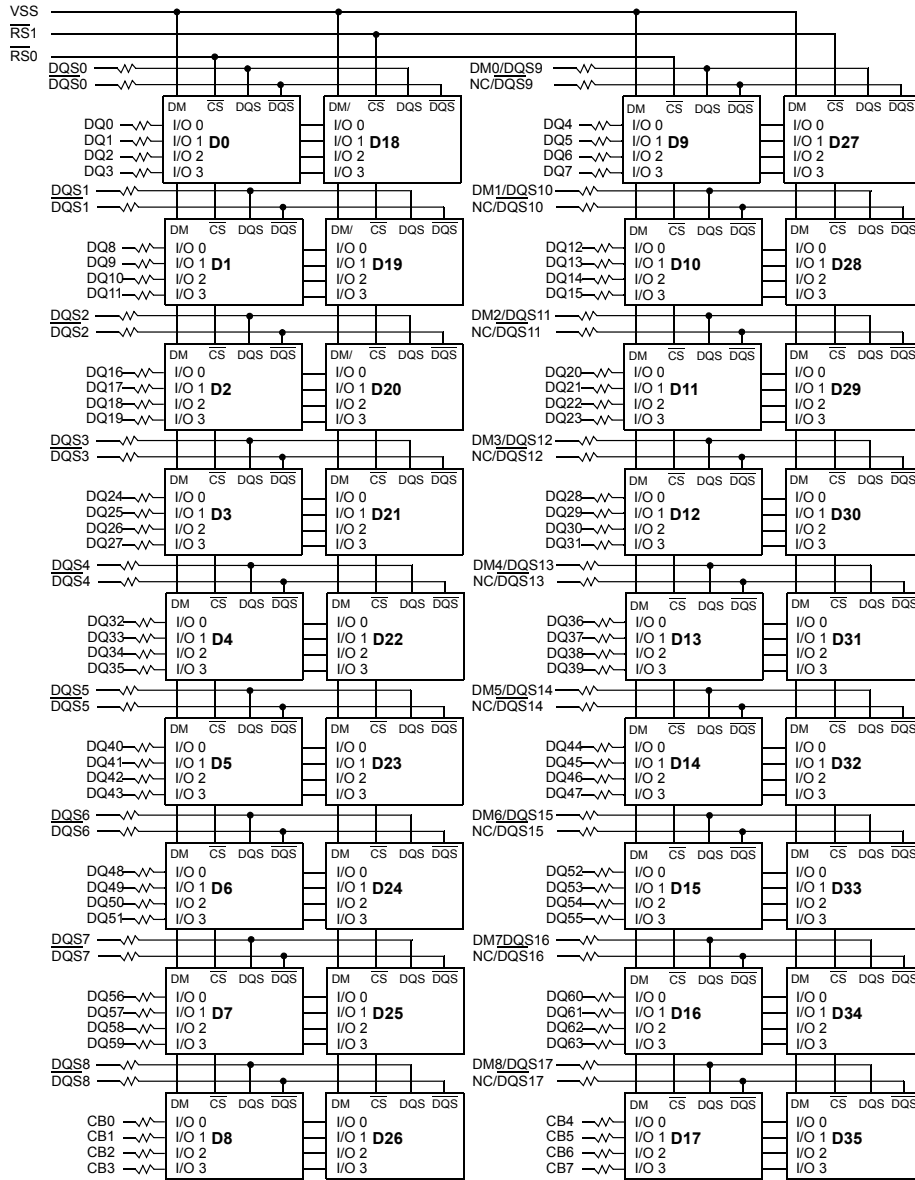
\*  $\overline{S0}$  connects to  $\overline{DCS}$  of Register1,  $\overline{CSR}$  of Register2.  $\overline{CSR}$  of register 1 and  $\overline{DCS}$  of register 2 connects to VDD.

\*\* RESET, PCK7 and PCK7 connects to both Registers. Other signals connect to one of two Registers.

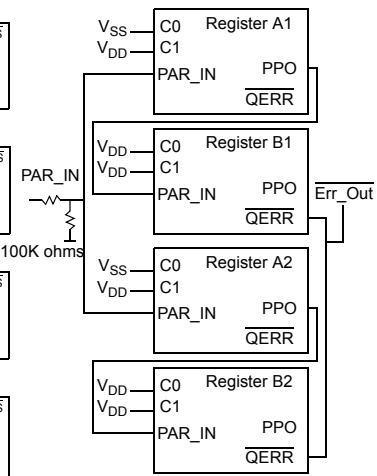
# 1GB, 2GB, 4GB Registered DIMMs

# DDR2 SDRAM

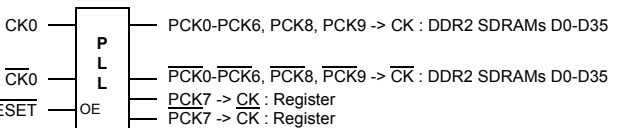
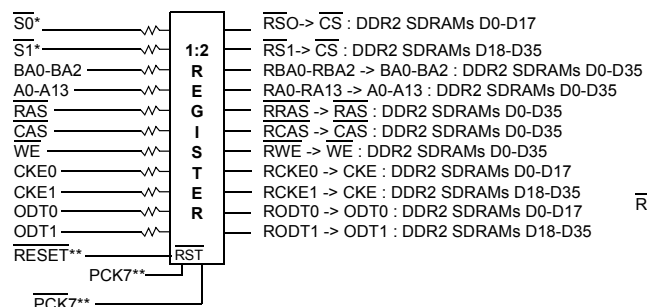
## 4GB, 512Mx72 Module (M393T5168AZ0/M393T5166AZA) (populated as 2 rank of x4 DDR2 SDRAMs)



Signals for Address and Command Parity Function (M393T5166AZA)



Register A1 and A2 share the a part of Add/ Cmd input signal set.  
 Register B1 and B2 share the rest part of Add/ Cmd input signal set.  
 The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address inputs"



\* S0 connects to DCS and S1 connects to CSR on a Register,  
 S1 connects to DCS and S0 connects to CSR on another Register.  
 \*\* RESET, PCK7 and PCK7 connects to both Registers.  
 Other signals connect to one of two Registers.



**Absolute Maximum DC Ratings**

Symbol	Parameter	Rating	Units	Notes
$V_{DD}$	Voltage on $V_{DD}$ pin relative to $V_{SS}$	- 1.0 V ~ 2.3 V	V	1
$V_{DDQ}$	Voltage on $V_{DDQ}$ pin relative to $V_{SS}$	- 0.5 V ~ 2.3 V	V	1
$V_{DDL}$	Voltage on $V_{DDL}$ pin relative to $V_{SS}$	- 0.5 V ~ 2.3 V	V	1
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	- 0.5 V ~ 2.3 V	V	1
$T_{STG}$	Storage Temperature	-55 to +100	°C	1, 2

Note :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

**AC & DC Operating Conditions**

Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
$V_{DD}$	Supply Voltage	1.7	1.8	1.9	V	
$V_{DDL}$	Supply Voltage for DLL	1.7	1.8	1.9	V	4
$V_{DDQ}$	Supply Voltage for Output	1.7	1.8	1.9	V	4
$V_{REF}$	Input Reference Voltage	$0.49 \cdot V_{DDQ}$	$0.50 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	mV	1,2
$V_{TT}$	Termination Voltage	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	3

Note : There is no specific device  $V_{DD}$  supply voltage requirement for SSTL-1.8 compliance. However under all conditions  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .

- The value of  $V_{REF}$  may be selected by the user to provide optimum noise margin in the system. Typically the value of  $V_{REF}$  is expected to be about  $0.5 \times V_{DDQ}$  of the transmitting device and  $V_{REF}$  is expected to track variations in  $V_{DDQ}$ .
- Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF}(DC)$ .
- $V_{TT}$  of transmitting device must track  $V_{REF}$  of receiving device.
- AC parameters are measured with  $V_{DD}$ ,  $V_{DDQ}$  and  $V_{DDL}$  tied together.

## Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature	0 to 95	°C	1, 2, 3

Note :

- Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
- At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period ( tREFI=3.9 us ) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

## Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V <sub>IH</sub> (DC)	DC input logic high	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V	
V <sub>IL</sub> (DC)	DC input logic low	- 0.3	V <sub>REF</sub> - 0.125	V	

## Input AC Logic Level

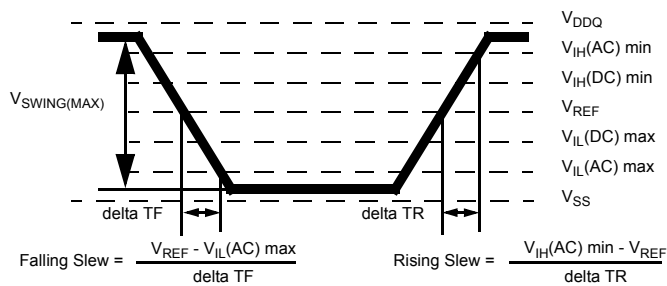
Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667		Units
		Min.	Max.	Min.	Max.	
V <sub>IH</sub> (AC)	AC input logic high	V <sub>REF</sub> + 0.250	-	V <sub>REF</sub> + 0.200	-	V
V <sub>IL</sub> (AC)	AC input logic low	-	V <sub>REF</sub> - 0.250	-	V <sub>REF</sub> - 0.200	V

## AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V <sub>REF</sub>	Input reference voltage	0.5 * V <sub>DDQ</sub>	V	1
V <sub>SWING(MAX)</sub>	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:

- Input waveform timing is referenced to the input signal crossing through the V<sub>IH/IL</sub>(AC) level applied to the device under test.
- The input signal minimum slew rate is to be maintained over the range from V<sub>REF</sub> to V<sub>IH</sub>(AC) min for rising edges and the range from V<sub>REF</sub> to V<sub>IL</sub>(AC) max for falling edges as shown in the below figure.
- AC timings are referenced with input waveforms switching from V<sub>IL</sub>(AC) to V<sub>IH</sub>(AC) on the positive transitions and V<sub>IH</sub>(AC) to V<sub>IL</sub>(AC) on the negative transitions.



< AC Input Test Signal Waveform >

## IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Units	Note
IDD0	<b>Operating one bank active-precharge current;</b> t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmin</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD1	<b>Operating one bank active-read-precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmin</sub> (IDD), t <sub>RCD</sub> = t <sub>RCD</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD2P	<b>Precharge power-down current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2N	<b>Precharge standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD3P	<b>Active power-down current;</b> All banks open; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA
		Slow PDN Exit MRS(12) = 1mA	mA
IDD3N	<b>Active standby current;</b> All banks open; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD5B	<b>Burst auto refresh current;</b> t <sub>CK</sub> = t <sub>CK</sub> (IDD); Refresh command at every t <sub>RFC</sub> (IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD6	<b>Self refresh current;</b> CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA
		Low Power	mA
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = t <sub>RCD</sub> (IDD) - 1 * t <sub>CK</sub> (IDD); t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RRD</sub> = t <sub>RRD</sub> (IDD), t <sub>FAW</sub> = t <sub>FAW</sub> (IDD), t <sub>RCD</sub> = 1 * t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	mA	

# 1GB, 2GB, 4GB Registered DIMMs

# DDR2 SDRAM

## Operating Current Table(1-1)

### M393T2863AZ3/M393T2863AZA : 1GB(128Mx8 \*9) Module

(TA=0°C, VDD= 1.9V)

Symbol	E6 (DDR2-667@CL=5)	D5 (DDR2-533@CL=4)	CC (DDR2-400@CL=3)	Unit	Notes
IDD0	TBD	1,285	1,175	mA	
IDD1	TBD	1,405	1,285	mA	
IDD2P	TBD	625	585	mA	
IDD2Q	TBD	895	800	mA	
IDD2N	TBD	865	760	mA	
IDD3P-F	TBD	795	765	mA	
IDD3P-S	TBD	402	392	mA	
IDD3N	TBD	1,090	975	mA	
IDD4W	TBD	1,710	1,455	mA	
IDD4R	TBD	1,570	1,385	mA	
IDD5B	TBD	2,455	2,350	mA	
IDD6*	Normal	TBD	135	mA	
IDD7	TBD	3,200	2,930	mA	

\* IDD6 = DRAM current + standby current of PLL and Register

\*\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

### M393T5663AZ3/M393T5663AZA : 2GB(128Mx8 \*18) Module

(TA=0°C, VDD= 1.9V)

Symbol	E6 (DDR2-667@CL=5)	D5 (DDR2-533@CL=4)	CC (DDR2-400@CL=3)	Unit	Notes
IDD0	TBD	1,790	1,665	mA	
IDD1	TBD	1,920	1,815	mA	
IDD2P	TBD	910	850	mA	
IDD2Q	TBD	1,470	1,310	mA	
IDD2N	TBD	1,360	1,240	mA	
IDD3P-F	TBD	1,280	1,220	mA	
IDD3P-S	TBD	654	624	mA	
IDD3N	TBD	1,525	1,415	mA	
IDD4W	TBD	2,245	1,955	mA	
IDD4R	TBD	2,105	1,875	mA	
IDD5B	TBD	2,980	2,800	mA	
IDD6*	Normal	TBD	270	mA	
IDD7	TBD	3,965	3,500	mA	

\* IDD6 = DRAM current + standby current of PLL and Register

\*\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## M393T5660AZ3/M393T5660AZA : 2GB(256Mx4 \*18) Module

(TA=0°C, VDD= 1.9V)

Symbol	E6 (DDR2-667@CL=5)	D5 (DDR2-533@CL=4)	CC (DDR2-400@CL=3)	Unit	Notes
IDD0	TBD	2,150	2,070	mA	
IDD1	TBD	2,370	2,310	mA	
IDD2P	TBD	910	850	mA	
IDD2Q	TBD	1,470	1,310	mA	
IDD2N	TBD	1,360	1,240	mA	
IDD3P-F	TBD	1,280	1,220	mA	
IDD3P-S	TBD	654	624	mA	
IDD3N	TBD	1,660	1,550	mA	
IDD4W	TBD	2,830	2,360	mA	
IDD4R	TBD	2,690	2,280	mA	
IDD5B	TBD	4,510	4,330	mA	
IDD6*	Normal	TBD	270	mA	
IDD7	TBD	6,080	5,480	mA	

\* IDD6 = DRAM current + standby current of PLL and Register

\*\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## M393T5168AZ0/M393T5166AZA : 4GB(st.512Mx4 \*18) Module

(TA=0°C, VDD= 1.9V)

Symbol	E6 (DDR2-667@CL=5)	D5 (DDR2-533@CL=4)	CC (DDR2-400@CL=3)	Unit	Notes
IDD0	TBD	3,170	3,040	mA	
IDD1	TBD	3,420	3,370	mA	
IDD2P	TBD	1,480	1,380	mA	
IDD2Q	TBD	2,600	2,320	mA	
IDD2N	TBD	2,360	2,210	mA	
IDD3P-F	TBD	2,240	2,140	mA	
IDD3P-S	TBD	1,138	1,088	mA	
IDD3N	TBD	2,590	2,330	mA	
IDD4W	TBD	3,920	3,360	mA	
IDD4R	TBD	3,770	3,260	mA	
IDD5B	TBD	5,550	5,230	mA	
IDD6*	Normal	TBD	540	mA	
IDD7	TBD	7,610	6,630	mA	

\* IDD6 = DRAM current + standby current of PLL and Register

\*\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## Input/Output Capacitance

(V<sub>DD</sub>=1.8V, V<sub>DDQ</sub>=1.8V, T<sub>A</sub>=25°C)

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Part-Number		M393T2863AZ3 M393T2863AZA	M393T5663AZ3 M393T5663AZA	M393T5660AZ3 M393T5660AZA	M393T5168AZ0 M393T5166AZA					
Input capacitance, CK and $\overline{\text{CK}}$	CCK	-	11	-	11	-	11	-	11	pF
Input capacitance, CKE and $\overline{\text{CS}}$	CI1	-	12	-	12	-	12	-	12	
Input capacitance, Addr, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	CI2	-	12	-	12	-	12	-	12	
Input/output capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$	CIO	-	10	-	10	-	10	-	10	

\* DM is internally loaded to match DQ and DQS identically.



## Electrical Characteristics & AC Timing for DDR2-667/533/400

(0 °C ≤ T<sub>OPER</sub> ≤ 95 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V)

### Refresh Parameters by Device Density

Parameter	Symbol	256Mb	512Mb	1Gb	2Gb	4Gb	Units	
Refresh to active/Refresh command time	tRFC	75	105	127.5	195	327.5	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T <sub>CASE</sub> ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T <sub>CASE</sub> ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

### Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-667(E6)		DDR2-533(D5)		DDR2-400(CC)		Units
Bin(CL - tRCD - tRP)	5 - 5 - 5		4 - 4 - 4		3 - 3 - 3		
Parameter	min	max	min	max	min	max	
tCK, CL=3	5	8	5	8	5	8	ns
tCK, CL=4	3.75	8	3.75	8	5	8	ns
tCK, CL=5	3	8	-	-	-	-	ns
tRCD	15	-	15	-	15	-	ns
tRP	15	-	15	-	15	-	ns
tRC	54	-	55	-	55	-	ns
tRAS	39	70000	40	70000	40	70000	ns

### Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

Parameter	Symbol	DDR2-667		DDR2-533		DDR2-400		Units	Notes
		min	max	min	max	min	max		
DQ output access time from CK/CK̄	tAC	-450	+450	-500	+500	-600	+600	ps	
DQS output access time from CK/CK̄	tDQSCK	-400	+400	-450	+450	-500	+500	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)	x	min(tCL, tCH)	x	min(tCL, tCH)	x	ps	
Clock cycle time, CL=x	tCK	3000	8000	3750	8000	5000	8000	ps	
DQ and DM input hold time	tDH	175	x	225	x	275	x	ps	
DQ and DM input setup time	tDS	100	x	100	x	150	x	ps	
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/CK̄	tHZ	x	tAC max	x	tAC max	x	tAC max	ps	
DQS low-impedance time from CK/CK̄	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/CK̄	tLZ(DQ)	2*tAC min	tAC max	2* tACmin	tAC max	2* tACmin	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	240	x	300	x	350	ps	
DQ hold skew factor	tQHS	x	340	x	400	x	450	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK	

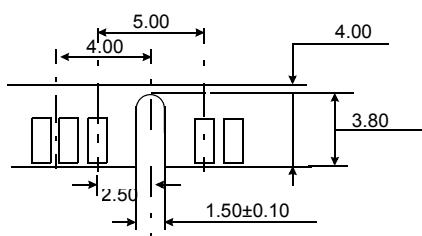
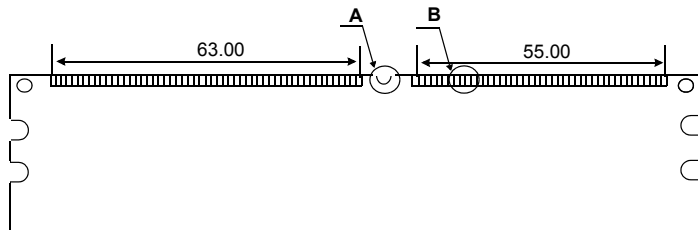
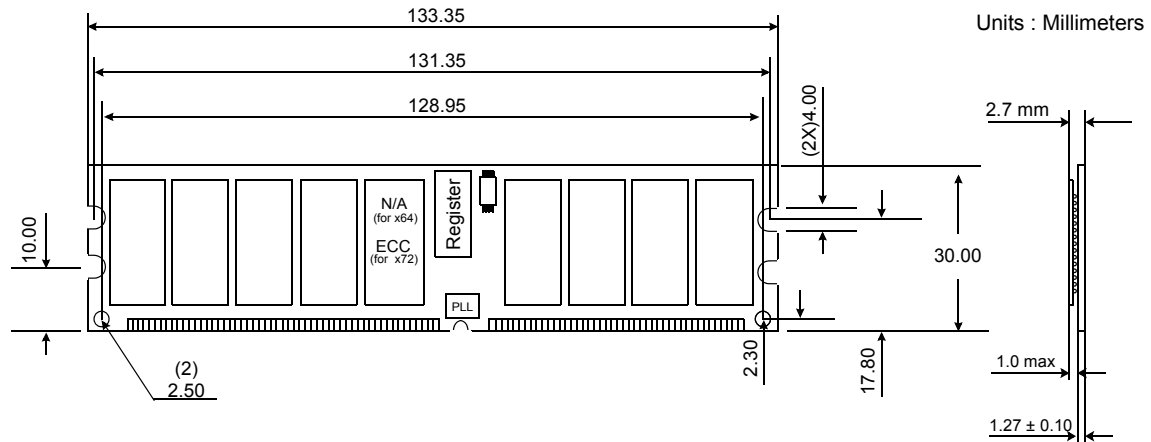
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# DDR2 SDRAM

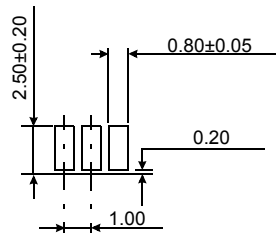
Parameter	Symbol	DDR2-667		DDR2-533		DDR2-400		Units	Notes
		min	max	min	max	min	max		
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	2	x	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	tCK	
Address and control input hold time	tIH	275	x	375	x	475	x	ps	
Address and control input setup time	tIS	200	x	250	x	350	x	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	ns	
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	ns	
Four Activate Window for 1KB page size products	tFAW	37.5		37.5		37.5		ns	
Four Activate Window for 2KB page size products	tFAW	50		50		50		ns	
CAS to CAS command delay	tCCD	2		2		2		tCK	
Write recovery time	tWR	15	x	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	tWR+tRP	x	tWR+tRP	x	tCK	
Internal write to read command delay	tWTR	7.5	x	7.5	x	10	x	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	2	x	tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		6 - AL		6 - AL		tCK	
CKE minimum pulse width(high and low pulse width)	tCKE	3		3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		3		tCK	
ODT power down exit latency	tAXPD	8		8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		tIS+tCK+tIH		ns	

## Physical Dimensions

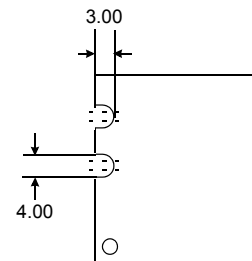
128Mbx8 based 128Mx72 Module(1 Rank) (M393T2863AZ3/M393T2863AZA)



Detail A



Detail B



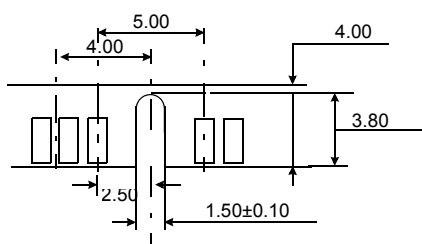
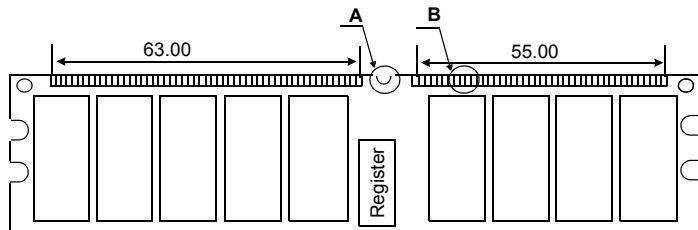
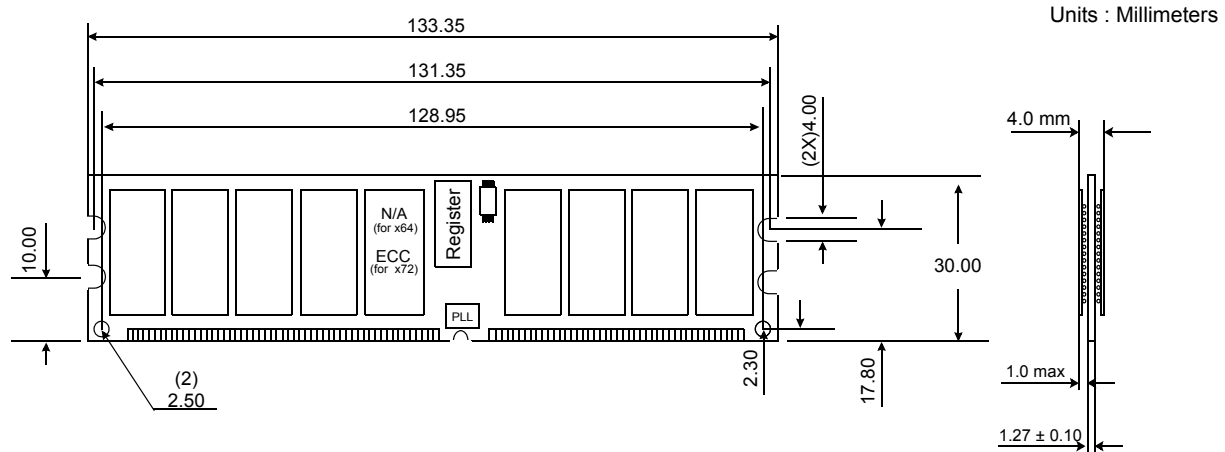
The used device is 128M x8 DDR2 SDRAM, FBGA.  
DDR2 SDRAM Part NO : K4T1G084QA

# 1GB, 2GB, 4GB Registered DIMMs

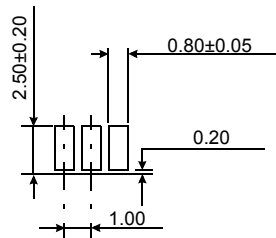
# DDR2 SDRAM

128Mbx8/256Mbx4 based 256Mx72 Module(2/1 Ranks)

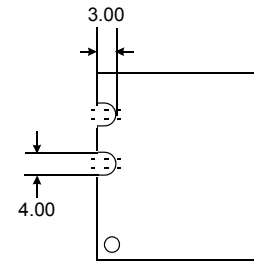
(M393T5663AZ3 / M393T5663AZA / M393T5660AZ3 / M393T5660AZA)



Detail A

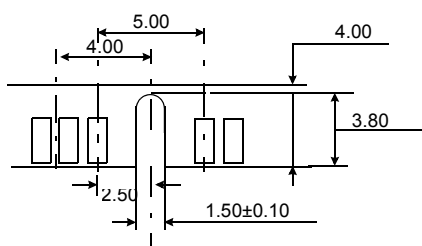
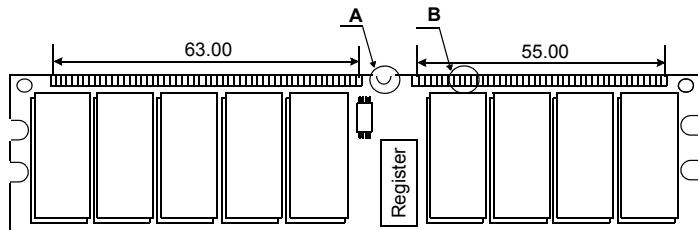
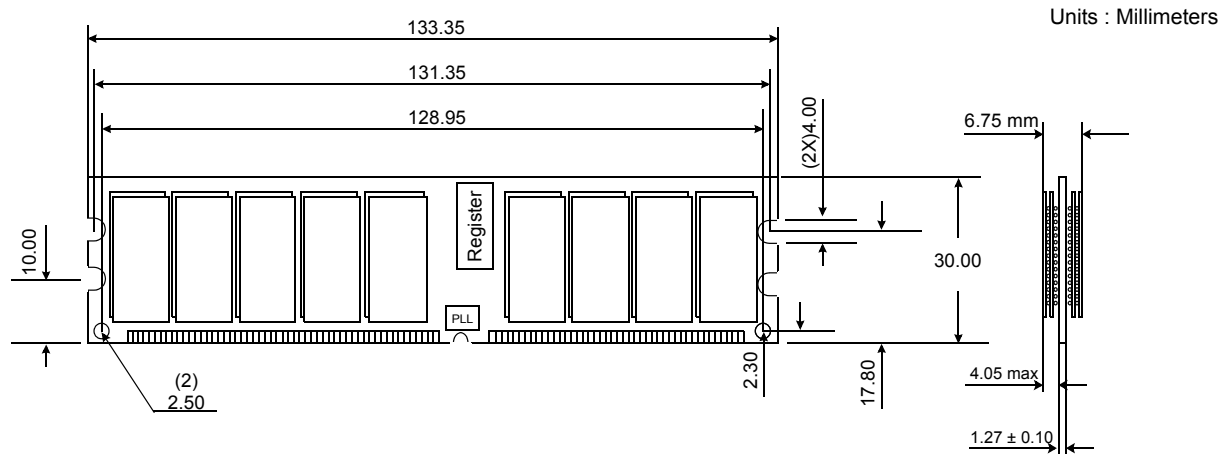


Detail B

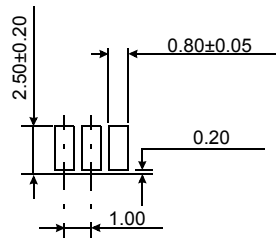


The used device is 128M x8 / 256M x4 DDR2 SDRAM, FBGA.  
DDR2 SDRAM Part NO : K4T1G084QA / K4T1G044QA

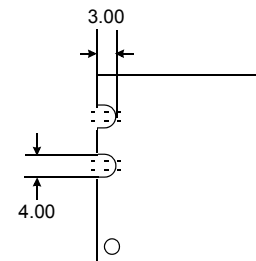
## St.512Mbx4 based 512Mx72 Module(2 Ranks) (M393T5168AZ0/M393T5166AZA)



Detail A

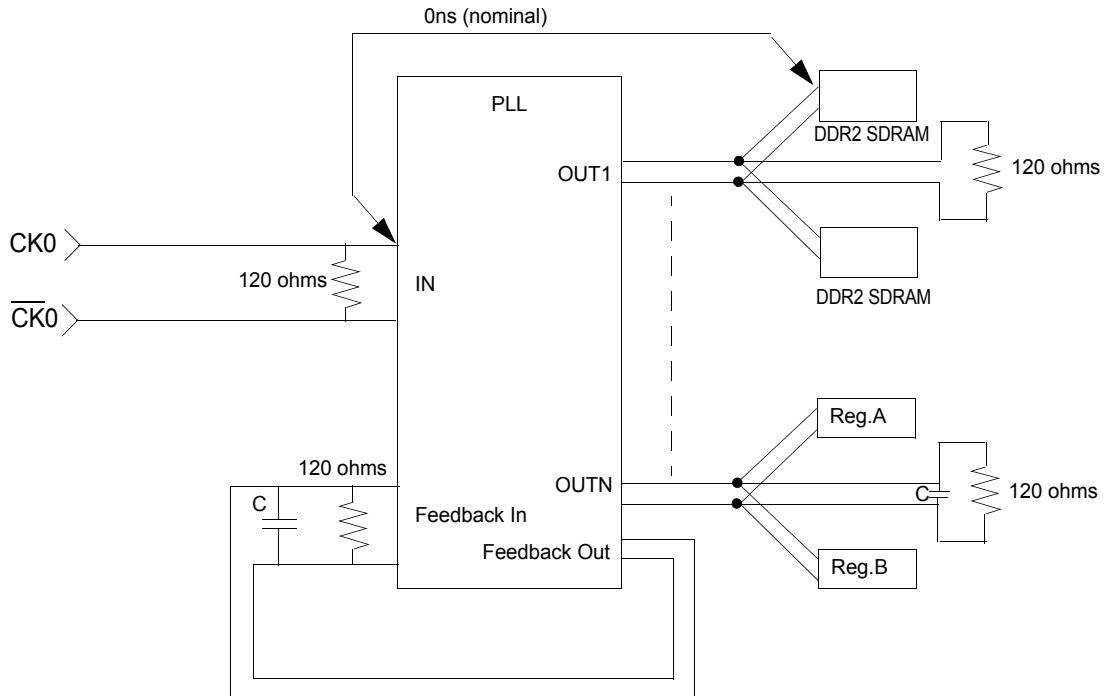


Detail B



The used device is st.512M x4 DDR2 SDRAM.  
 DDR2 SDRAM Part NO : K4T2G064QA / K4T2G264QA

240 Pin DDR2 Registered DIMM Clock Topology



Note :

1. The clock delay from the input of the PLL clock to the input of any DDR2 SDRAM or register will be set to 0ns (nominal).
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.