

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD95N03 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

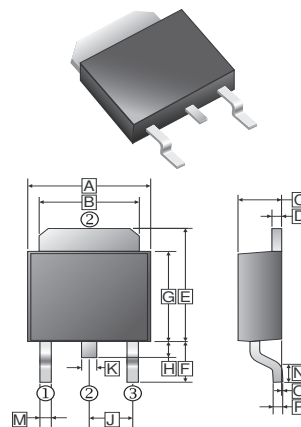
FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING



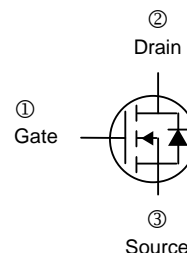
TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30	REF.
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	$V_{GS}=10V, T_C=25^\circ\text{C}$	96
		$V_{GS}=10V, T_C=100^\circ\text{C}$	88
Pulsed Drain Current ²	I_{DM}	192	A
Total Power Dissipation ⁴	P_D	62.5	W
Linear Derating Factor		0.42	W / $^\circ\text{C}$
Single Pulse Avalanche Energy ³	E_{AS}	317	mJ
Single Pulse Avalanche Current	I_{AS}	53.8	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	62	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	2.4	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	-	0.0213	-	V / $^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$	
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Forward Transconductance	g_{fs}	-	26.5	-	S	$V_{DS}=5\text{V}, I_D=30\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20\text{V}$	
Drain-Source Leakage Current	$T_J=25^\circ\text{C}$	I_{DSS}	-	-	1	μA	$V_{DS}=24\text{V}, V_{GS}=0$
	$T_J=55^\circ\text{C}$		-	-	5		$V_{DS}=24\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	3.4	4	m Ω	$V_{GS}=10\text{V}, I_D=30\text{A}$	
		-	5.2	6		$V_{GS}=4.5\text{V}, I_D=15\text{A}$	
Total Gate Charge	Q_g	-	31.6	-	nC	$I_D=15\text{A}$ $V_{DS}=15\text{V}$ $V_{GS}=4.5\text{V}$	
Gate-Source Charge	Q_{gs}	-	8.6	-			
Gate-Drain ("Miller") Change	Q_{gd}	-	11.7	-			
Turn-on Delay Time	$T_{d(on)}$	-	9	-	nS	$V_{DD}=15\text{V}$ $I_D=15\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$	
Rise Time	T_r	-	19	-			
Turn-off Delay Time	$T_{d(off)}$	-	58	-			
Fall Time	T_f	-	15.2	-			
Input Capacitance	C_{iss}	-	3075	4000	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1.0\text{MHz}$	
Output Capacitance	C_{oss}	-	400	530			
Reverse Transfer Capacitance	C_{rss}	-	315	-			
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy ⁵	EAS	98	-	-	mJ	$V_{DD}=25\text{V}, L=0.1\text{mH}, I_{AS}=30\text{A}$	
Source-Drain Diode							
Diode Forward Voltage ²	V_{SD}	-	-	1.2	V	$I_S=30\text{A}, V_{GS}=0$	
Continuous Source Current ^{1,6}	I_S	-	-	96	A	$V_D=V_G=0$, Force Current	
Pulsed Source Current ^{2,6}	I_{SM}	-	-	192	A		

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=53.8\text{A}$
- The power dissipation is limited by 175°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

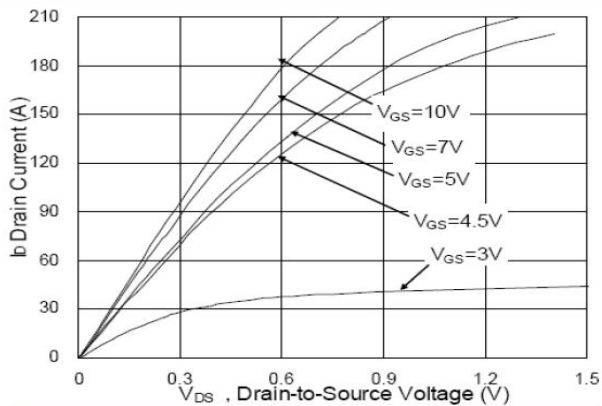


Fig.1 Typical Output Characteristics

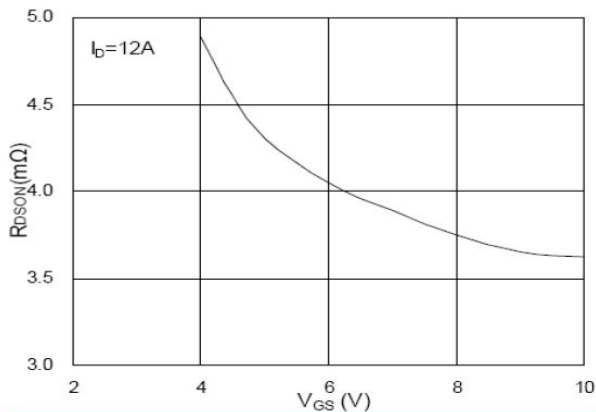


Fig.2 On-Resistance vs. G-S Voltage

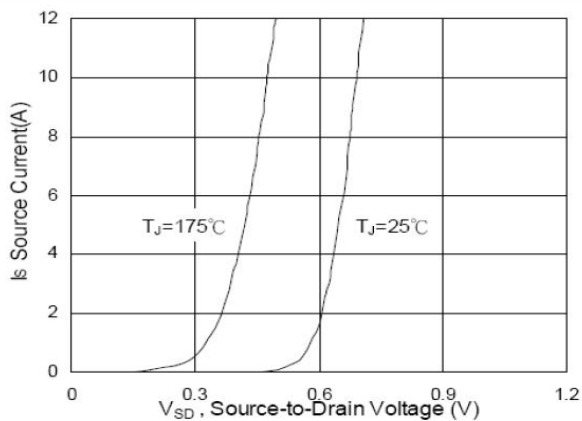


Fig.3 Forward Characteristics of Reverse

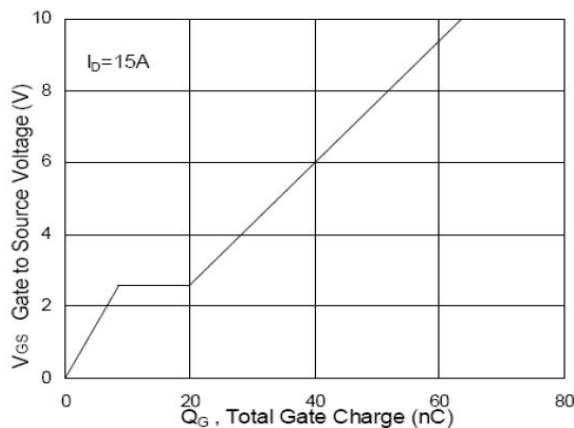


Fig.4 Gate-Charge Characteristics

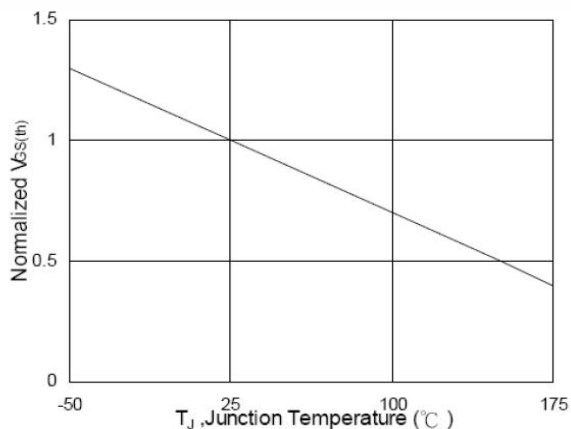


Fig.5 Normalized V_{GS(th)} vs. T_J

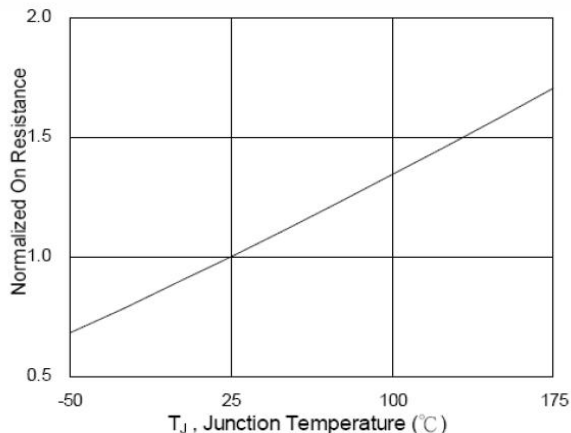


Fig.6 Normalized R_{DS(ON)} vs. T_J

CHARACTERISTIC CURVES

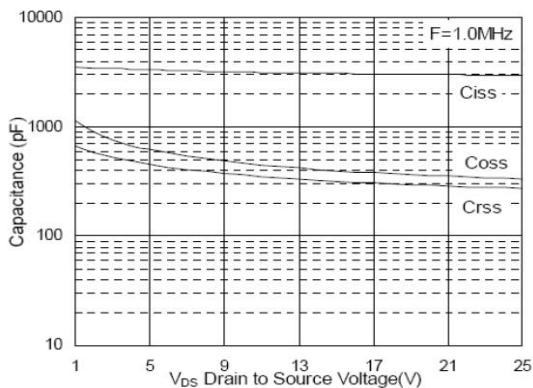


Fig.7 Capacitance

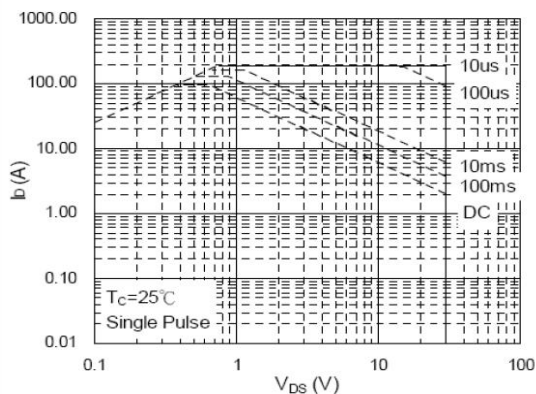


Fig.8 Safe Operating Area

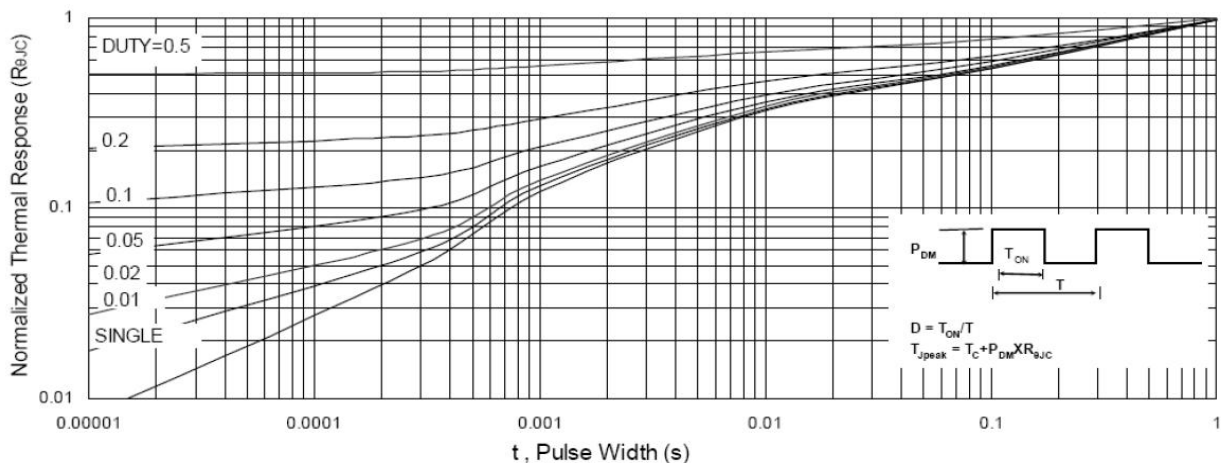


Fig.9 Normalized Maximum Transient Thermal Impedance

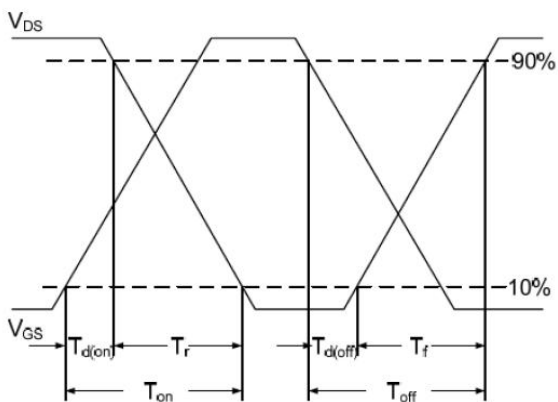


Fig.10 Switching Time Waveform

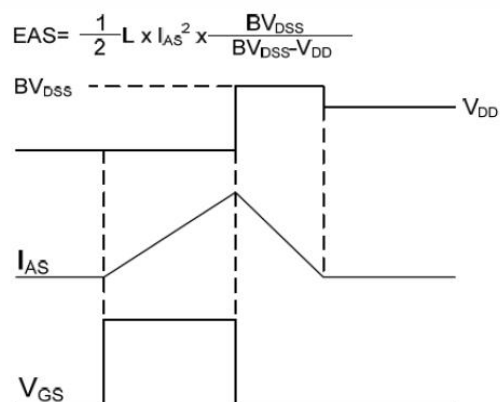


Fig.11 Unclamped Inductive Switching Wave