

54F/74F410 Register Stack—16 x 4 RAM TRI-STATE® Output Register

General Description

The 'F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. TRI-STATE outputs are provided for maximum versatility. The 'F410 is fully compatible with all TTL families.

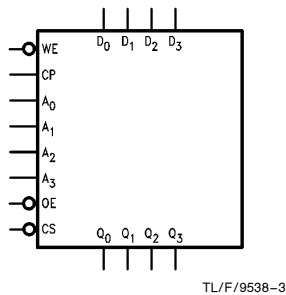
Features

- Edge-triggered output register
- Typical access time of 35 ns
- TRI-STATE outputs
- Optimized for register stack operation
- 18-pin package
- 9410 replacement

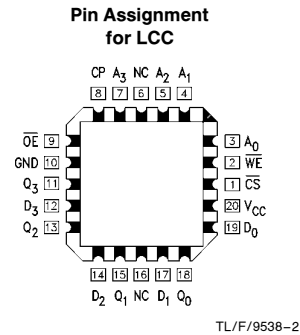
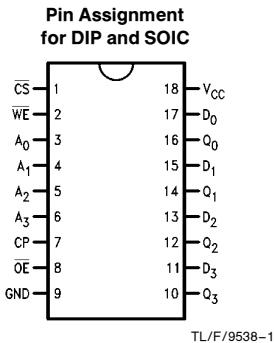
| Commercial | Military | Package Number | Package Description |
|------------|-------------------|----------------|---|
| 74F410PC | | N18A | 18-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F410DM (Note 1) | J18A | 18-Lead Ceramic Dual-In-Line |
| 74F410SC | | M20B | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 54F410LM | | W20A | 20-Lead Cerpak |

Note 1: Military grade device with environmental and burn-in processing. Use suffix = DMOB, LMQB

Logic Symbol



Connection Diagrams



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|-----------------|--|------------------|---|
| | | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| A_0-A_3 | Address Inputs | 1.0/1.0 | 20 μA / -0.6 mA |
| D_0-D_3 | Data Inputs | 1.0/1.0 | 20 μA / -0.6 mA |
| \overline{CS} | Chip Select Input (Active LOW) | 1.0/2.0 | 20 μA / -1.2 mA |
| \overline{OE} | Output Enable Input (Active LOW) | 1.0/1.0 | 20 μA / -0.6 mA |
| \overline{WE} | Write Enable Input (Active LOW) | 1.0/1.0 | 20 μA / -0.6 mA |
| CP | Clock Input (Outputs Change on LOW-to-HIGH Transition) | 1.0/2.0 | 20 μA / -1.2 mA |
| Q_0-Q_3 | TRI-STATE Outputs | 150/40 (33.3) | -3 mA/24 mA (20 mA) |

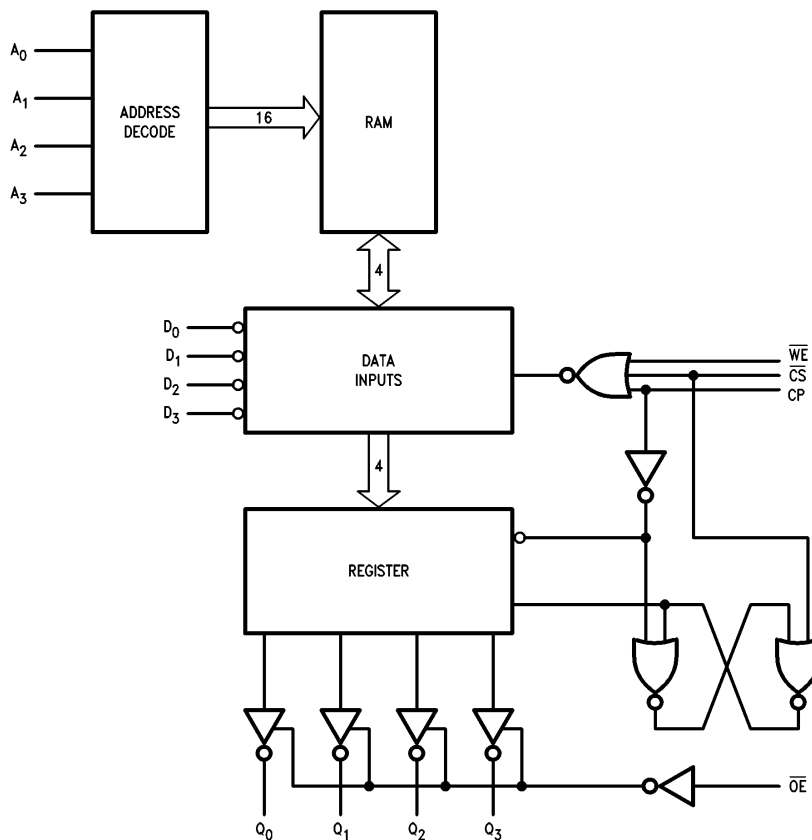
Functional Description

Write Operation—When the three control inputs, Write Enable (\overline{WE}), Chip Select (\overline{CS}), and Clock (CP), are LOW the information on the data inputs (D_0-D_3) is written into the memory location selected by the address inputs (A_0-A_3). If the input data changes while \overline{WE} , \overline{CS} , and CP are LOW, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation—Whenever \overline{CS} is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs (A_0-A_3) are edge-triggered into the Output Register.

The (\overline{OE}) input controls the output buffers. When \overline{OE} is HIGH the four outputs (Q_0-Q_3) are in a high impedance or OFF state; when \overline{OE} is LOW, the outputs are determined by the state of the Output Register.

Block Diagram



TL/F/9538-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------|-----------------|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +175°C |
| Plastic | −55°C to +150°C |

| | |
|---|----------------|
| V _{CC} Pin Potential to Ground Pin | −0.5V to +7.0V |
|---|----------------|

| | |
|------------------------|----------------|
| Input Voltage (Note 2) | −0.5V to +7.0V |
|------------------------|----------------|

| | |
|------------------------|-------------------|
| Input Current (Note 2) | −30 mA to +5.0 mA |
|------------------------|-------------------|

| | |
|---|--------------------------|
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | −0.5V to V _{CC} |
| TRI-STATE Output | −0.5V to +5.5V |

| | |
|--|--------------------------------------|
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
|--|--------------------------------------|

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | −55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|---------------------------------|--------------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | −1.2 | V | Min | I _{IN} = −18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} | 2.5 2.4 2.5 2.4 2.7 | | V | Min | I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −3 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | 54F 74F | | 20.0 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | 100 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | | 250 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | −0.6 −1.2 | mA | Max | V _{IN} = 0.5V (A _n , D _n , \overline{OE} , \overline{WE}) V _{IN} = 0.5V (\overline{CS} , CP) |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | −50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | | −60 | −150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |

DC Electrical Characteristics (Continued)

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|----------------------|---------|-----|-----|-------|-----------------|-------------------------|
| | | Min | Typ | Max | | | |
| I _{CCH} | Power Supply Current | | 47 | 70 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | 47 | 70 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | | 47 | 70 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics

| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|------------------|----------------------|---|-----|--|------|--|------|-------|
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 3.0 | 8.5 | 2.5 | 11.0 | 2.5 | 9.5 | ns |
| t _{PHL} | CP to Q | 3.5 | 9.0 | 3.0 | 12.0 | 3.0 | 10.0 | |
| t _{PZH} | Enable Time | 3.0 | 8.0 | 2.5 | 10.5 | 2.5 | 9.0 | ns |
| t _{PZL} | \overline{OE} to Q | 3.5 | 9.0 | 3.0 | 13.0 | 3.0 | 10.0 | |
| t _{PHZ} | Disable Time | 2.5 | 6.5 | 2.0 | 8.5 | 2.0 | 7.5 | |
| t _{PLZ} | \overline{OE} to Q | 2.5 | 7.0 | 2.0 | 9.5 | 2.0 | 8.0 | |

AC Operating Requirements

| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|--------|-----------|---|-----|--|-----|--|-----|-------|
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Mil | | T _A , V _{CC} = Com | | |
| | | Min | Max | Min | Max | Min | Max | |

READ MODE

| | | | | | | | | |
|--------------------|-------------------------|------|--|----|--|------|--|----|
| t _S (H) | Setup Time, HIGH or LOW | 15.0 | | 23 | | 17.0 | | ns |
| t _S (L) | A _n to CP | 15.0 | | 23 | | 17.0 | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 0 | | 0 | | |
| t _H (L) | A _n to CP | 0 | | 0 | | 0 | | |

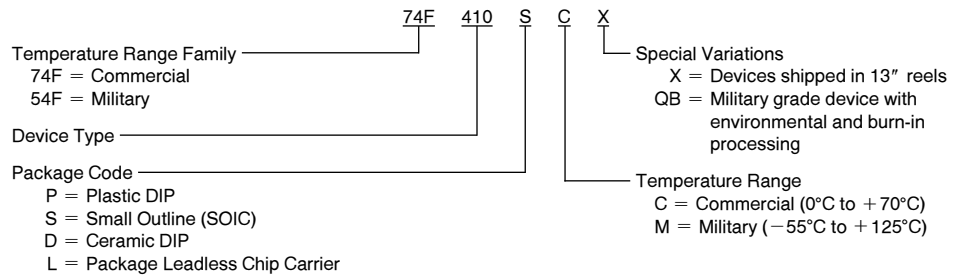
WRITE MODE

| | | | | | | | | |
|--------------------|--|-----|--|-----|--|-----|--|----|
| t _S (H) | Setup Time, HIGH or LOW | 0 | | 0 | | 0 | | ns |
| t _S (L) | A _n to \overline{WE} | 0 | | 0 | | 0 | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 0 | | 0 | | |
| t _H (L) | A _n to \overline{WE} | 0 | | 0 | | 0 | | |
| t _S (H) | Setup Time, HIGH or LOW | 5.0 | | 8.5 | | 6.0 | | ns |
| t _S (L) | D _n to \overline{WE} | 5.0 | | 8.5 | | 6.0 | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 2.5 | | 0 | | |
| t _H (L) | D _n to \overline{WE} | 0 | | 2.5 | | 0 | | |
| t _w | \overline{WE} Pulse Width Required to Write | 7.5 | | 9.5 | | 8.5 | | ns |
| t _w | \overline{CS} Pulse Width Required to Write | 7.5 | | 9.5 | | 8.5 | | ns |
| t _w | CP Pulse Width Required to Write | 7.5 | | 9.5 | | 8.5 | | ns |

Note: Military temperature range for this device is –40°C to +85°C.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

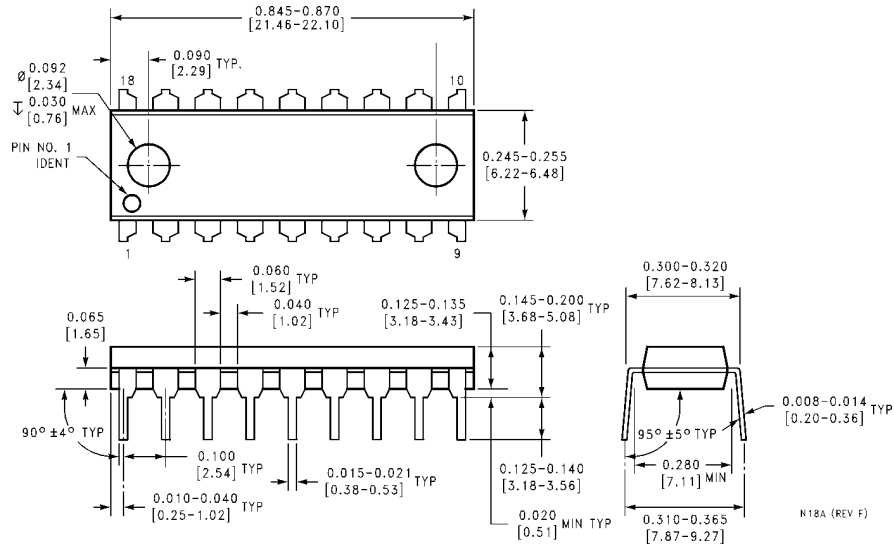


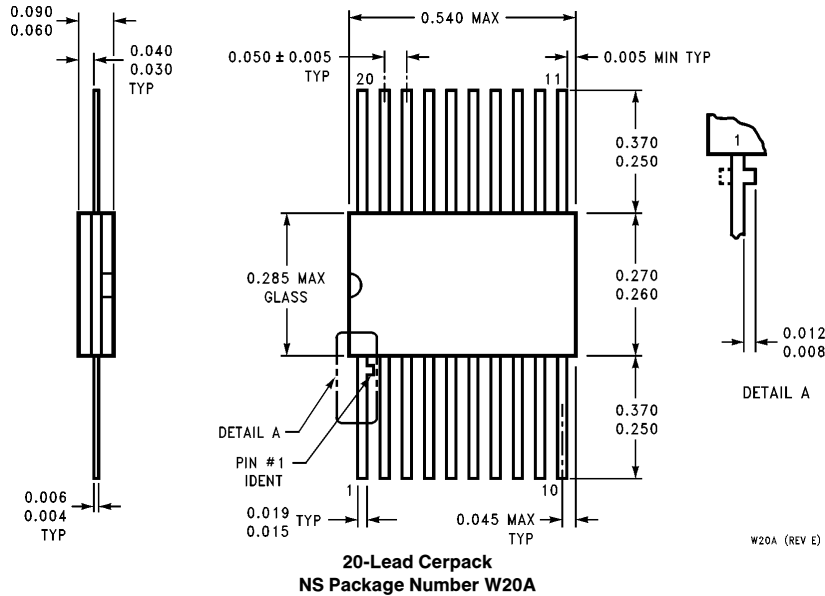
18-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J18A



**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B**

Physical Dimensions inches (millimeters) (Continued)



Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.