National Semiconductor

December 1994

54F407
Data Access Register

General Description

The ’F407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1), and Operand Address (R_2). The ’F407 implements 16 instructions which allow either pre- or post-decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 30 MHz microinstruction rate on a 16-bit word. The TRI-STATE® outputs are provided for bus-oriented applications. The ’F407 is fully compatible with all TTL families.

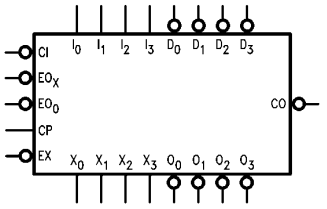
Features

- High-speed—greater than a 30 MHz microinstruction rate
- Three 4-bit registers
- 16 instructions for register manipulation
- Two separate output ports, one transparent
- Relative addressing capability
- TRI-STATE Outputs
- Optional pre- or post- arithmetic
- Expandable in multiples of four bits
- 24-pin slim package
- 9407 replacement

Military	Package Number	Package Description
54F407DM (Note 1)	J24A	24-Lead Ceramic Dual-In-Line
54F407SDM (Note 1)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
54F407FM (Note 1)	W24C	24-Lead Cerpack
54F407FM (Note 1)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbol



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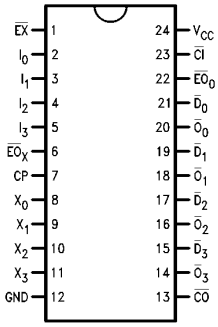
Connection Diagrams

Pin Assignment for DIP and Flatpak



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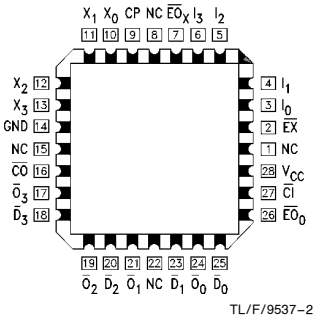
Pin Assignment for LCC



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RRD-B30M105/Printed in U. S. A.

Unit Loading/Fan Out

Pin Names	Description	54F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{D}_0-\overline{D}_3$	Data Inputs (Active LOW)	1.0/0.67	20 μA/−0.4 mA
I_0-I_3	Instruction Word Inputs	1.0/0.67	20 μA/−0.4 mA
$\overline{CI}$	Carry Input (Active LOW)	1.0/0.67	20 μA/−0.4 mA
$\overline{CO}$	Carry Output (Active LOW)	20/13.3 (0.67)	0.4 mA/8 mA (4 mA)
CP	Clock Input (L-H Edge-Triggered)	1.0/0.67	20 μA/−0.4 mA
$\overline{EX}$	Execute Input (Active LOW)	1.0/0.67	20 μA/−0.4 mA
$\overline{EO}_X$	Address Output Enable Input (Active LOW)	1.0/0.67	20 μA/−0.4 mA
$\overline{EO}_0$	Data Output Enable Input (Active LOW)	1.0/0.67	20 μA/−0.4 mA
X_0-X_3	Address Outputs	284 (100)/26.7 (13.3)	−5.7 mA (2 mA)/16 mA (8 mA)
$\overline{O}_0-\overline{O}_3$	Data Outputs (Active LOW)	284 (100)/26.7 (13.3)	−5.7 mA (2 mA)/16 mA (8 mA)

Functional Description

The ’F407 contains a 4-bit slice of three Registers (R_0-R_2), a 4-bit Adder, a TRI-STATE Address Output Buffer (X_0-X_3) and a separate Output Register with TRI-STATE buffers ($\overline{O}_0-\overline{O}_3$), allowing output of the register contents on the data bus (refer to the Block Diagram). The DAR performs sixteen instructions, selected by I_0-I_3, as listed in the Function Table.

The ’F407 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input, active LOW AND gate. For normal operation $\overline{EX}$ is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data inputs $\overline{D}_0-\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines ($I_1-I_2-I_3$) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH CP transition writes the result from the Adder into a register (R_0-R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the TRI-STATE Buffer controlling the address bus (X_0-X_3), independent of $\overline{EX}$ and CP. The ’F407 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

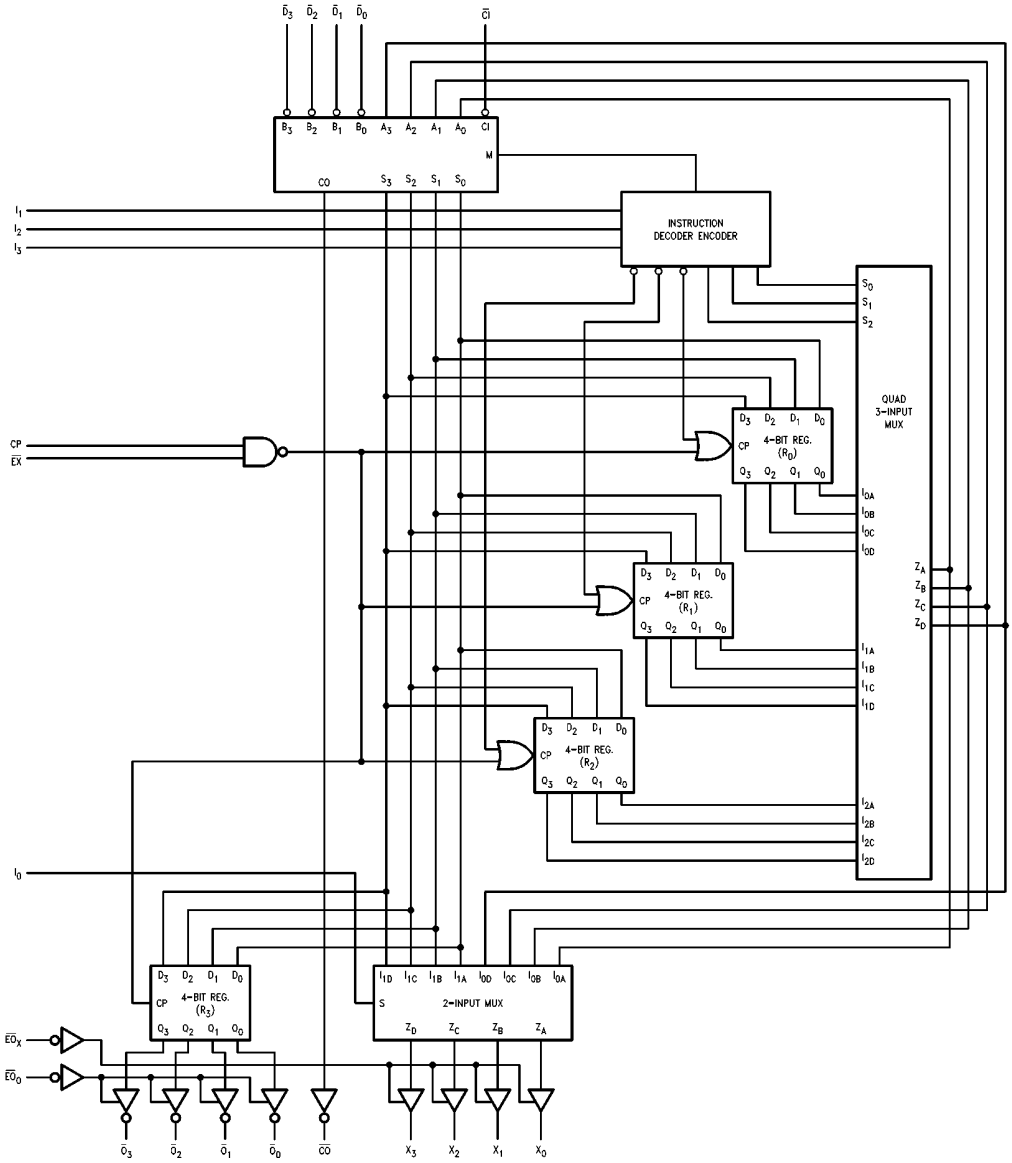
In a typical application, the register utilization in the DAR may be as follows: R_0 is the Program Counter (PC), R_1 is the Stack Pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction Fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

Function Table

Instruction				Combinatorial Function Available on the X-Bus	Sequential Function Occurring on the Next Rising CP Edge
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 Plus D Plus CI → R_0 and 0-Register
L	L	L	H	R_0 Plus D Plus CI	
L	L	H	L	R_0	R_0 Plus D Plus CI → R_1 and 0-Register
L	L	H	H	R_0 Plus D Plus CI	
L	H	L	L	R_0	R_0 Plus D Plus CI → R_2 and 0-Register
L	H	L	H	R_0 Plus D Plus CI	
L	H	H	L	R_1	R_1 Plus D Plus CI → R_1 and 0-Register
L	H	H	H	R_1 Plus D Plus CI	
H	L	L	L	R_2	D Plus CI → R_2 and 0-Register
H	L	L	H	D Plus CI	
H	L	H	L	R_0	D Plus CI → R_0 and 0-Register
H	L	H	H	D Plus CI	
H	H	L	L	R_2	R_2 Plus D Plus CI → R_2 and 0-Register
H	H	L	H	R_2 Plus D Plus CI	
H	H	H	L	R_1	D Plus CI → R_1 and 0-Register
H	H	H	H	D Plus CI	

H = HIGH Voltage Level
L = LOW Voltage Level

Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Timing Diagrams

$\overline{EO}_x$ = LOW

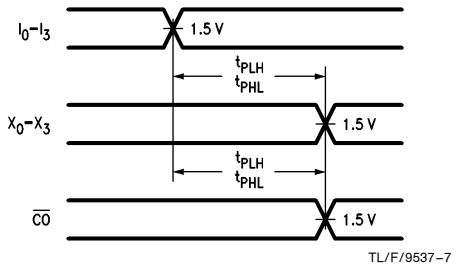

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FIGURE 407-a

$\overline{EO}_x$ = LOW

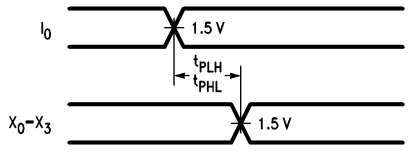

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FIGURE 407-b

$\overline{EO}_0$ = LOW

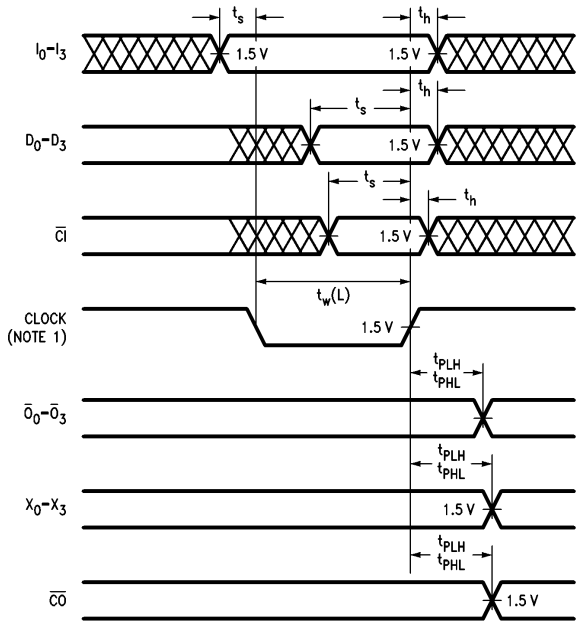

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FIGURE 407-c

$\overline{EO}_x$ = LOW, I_0 = HIGH

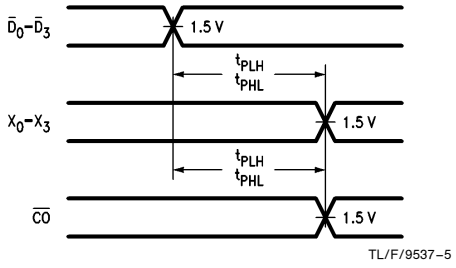

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FIGURE 407-d

$\overline{EO}_x$ = LOW, I_0 = HIGH

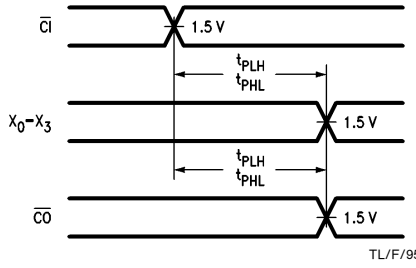

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FIGURE 407-e

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.5	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.4			V	Min	I_{OH} = −0.4 mA ($\overline{CO}$)
		54F 10% V_{CC}	2.4					I_{OH} = −2 mA (X_0–X_3, $\overline{O}_0$–$\overline{O}_3$)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}	0.5			V	Min	I_{OL} = 4 mA ($\overline{CO}$)
		54F 10% V_{CC}	0.5					I_{OL} = 8 mA (X_0–X_3, $\overline{O}_0$–$\overline{O}_3$)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
I_{IL}	Input LOW Current				−0.4	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V (X_0–X_3, $\overline{O}_0$–$\overline{O}_3$)
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V (X_0–X_3, $\overline{O}_0$–$\overline{O}_3$)
I_{OS}	Output Short-Circuit Current		−30		−100	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			90	145	mA	Max	

AC Electrical Characteristics

Symbol	Parameter	54F T_A, V_{CC} = Mil, C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$ (Note 1)	7.0 4.0	24.0 15.0	ns	407-c
t_{PLH} t_{PHL}	Propagation Delay, I_0 LOW I_1–I_3 to X_0–X_3	7.5 8.0	21.0 25.0	ns	407-a
t_{PLH} t_{PHL}	Propagation Delay, I_0 HIGH I_1–I_3 to X_0–X_3	8.5 6.5	50.0 35.0	ns	407-a
t_{PLH} t_{PHL}	Propagation Delay, I_0 LOW CP to X_n	7.0 8.5	24.0 28.0	ns	407-b
t_{PLH} t_{PHL}	Propagation Delay, I_0 HIGH CP to X_n	16.0 11.5	43.0 36.5	ns	407-b
t_{PLH} t_{PHL}	Propagation Delay $\overline{D}_n$ to X_n	6.5 3.0	29.0 20.5	ns	407-d
t_{PLH} t_{PHL}	Propagation Delay CI to X_n	4.0 4.5	22.0 14.0	ns	407-e
t_{PLH} t_{PHL}	Propagation Delay I_0 to X_n	4.0 3.0	14.5 19.5	ns	407-b
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CO}$	9.0 6.5	33.0 38.0	ns	407-a
t_{PLH} t_{PHL}	Propagation Delay $\overline{CI}$ to $\overline{CO}$	3.0 3.0	11.0 10.0	ns	407-e
t_{PLH} t_{PHL}	Propagation Delay $\overline{D}_n$ to $\overline{CO}$	3.0 3.5	10.0 10.0	ns	407-d
t_{PLH} t_{PHL}	Propagation Delay I_1–I_3 to $\overline{CO}$	8.0 6.0	23.0 32.5	ns	407-a
t_{PZH} t_{PZL}	Enable Time $\overline{EO}_0$ to $\overline{O}_n$ or $\overline{EO}_x$ to X_n	4.5 3.5	26.0 16.0	ns	
t_{PHZ} t_{PLZ}	Disable Time $\overline{EO}_0$ to $\overline{O}_n$ or $\overline{EO}_x$ to X_n	2.0 5.0	9.0 18.0	ns	

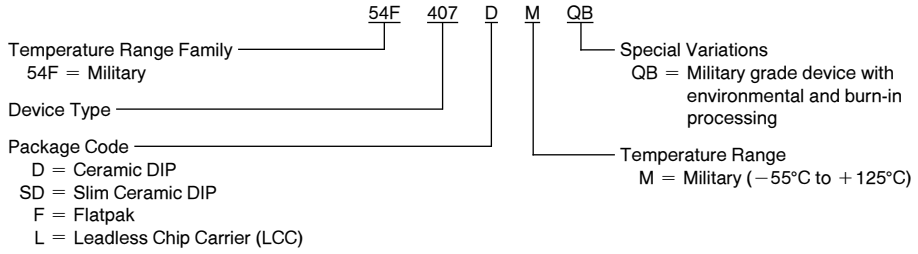
Note 1: The internal clock is generated from CP and $\overline{EX}$. The internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW.

AC Electrical Characteristics (Continued)

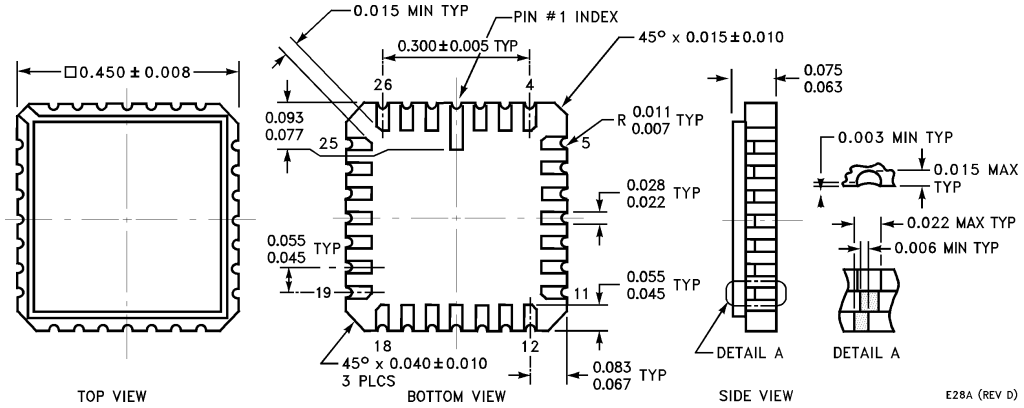
Symbol	Parameter	54F T_A, V_{CC} = Mil C_L = 50 pF Min	54F T_A, V_{CC} = Mil C_L = 50 pF Max	Units	Fig. No.
t_{cw}	Clock Period	36.0		ns	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I_1–I_3 to Negative-Going CP	4.5 4.5		ns	407-c
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I_1–I_3 to Positive-Going CP	0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{D}_n$ or $\overline{C}_1$ to Negative-Going CP	18.5 18.5		ns	407-c
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{D}_n$ or $\overline{CI}$ to Negative-Going Clock	0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CI}$ to Positive-Going CP	14.5 14.5		ns	407-c
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CI}$ to Positive-Going CP	0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	8.5 8.5		ns	407-c

Ordering Information

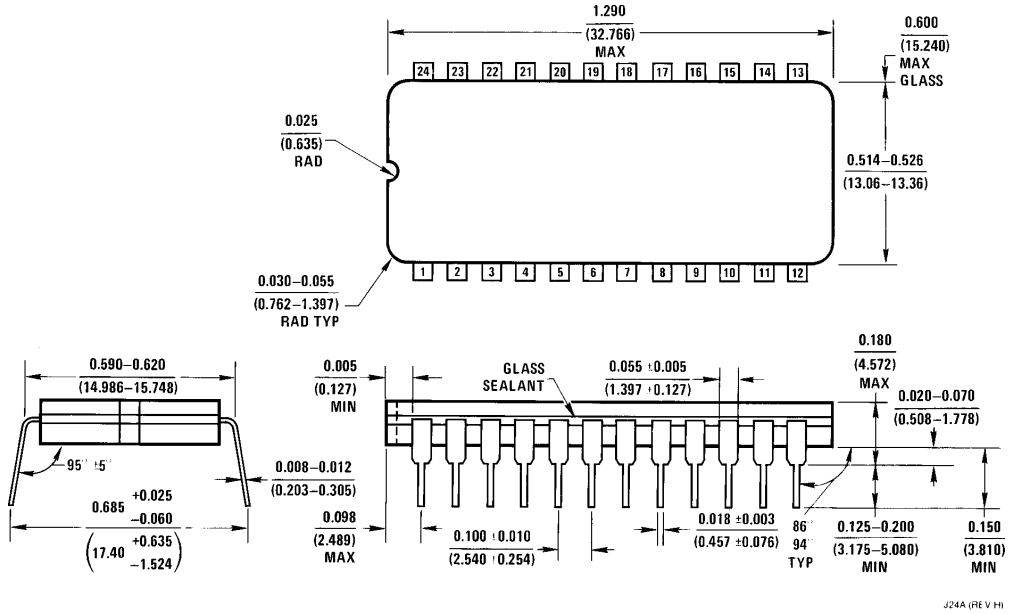
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

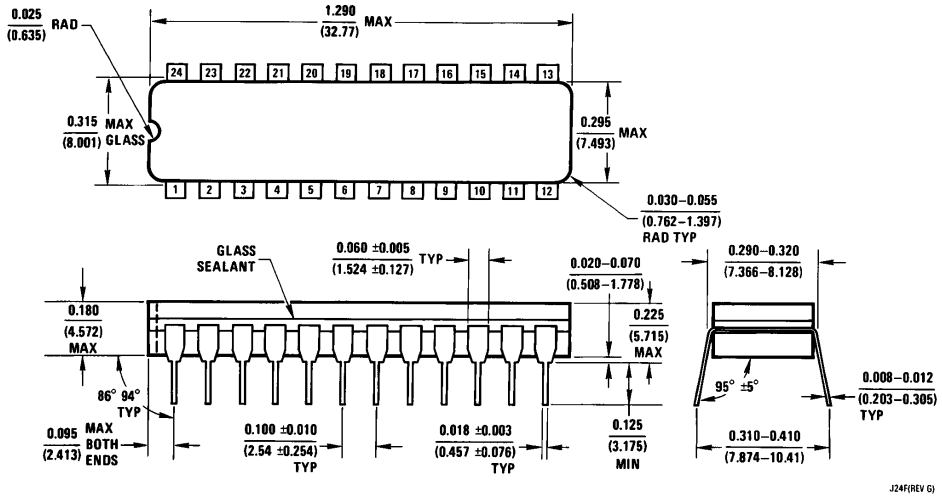


28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



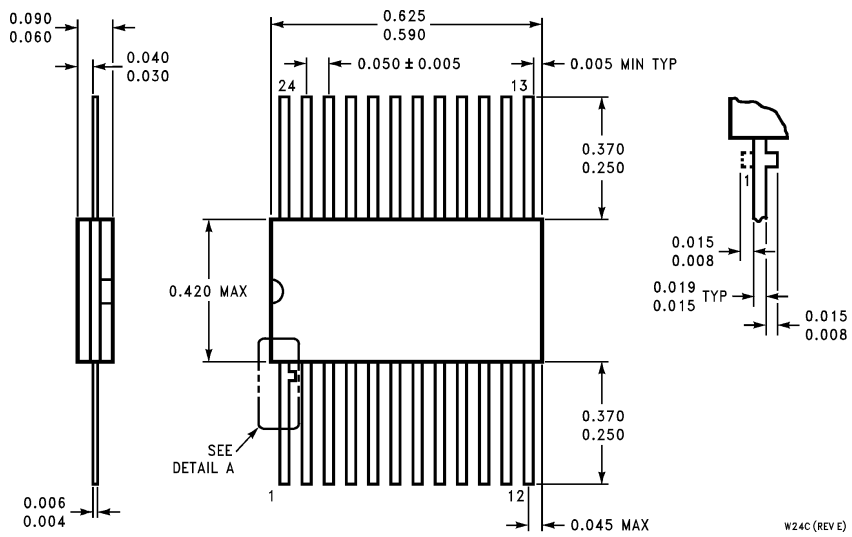
24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A

Physical Dimensions inches (millimeters) (Continued)



24-Lead Slim (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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